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Clock Gating Based Energy Efficient and Thermal Aware Design of Latin Unicode Reader for Natural Language Processing on FPGA

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Abstract

In this paper we have aimed to design an energy efficient and thermally aware Latin Unicode Reader. Our design is based on 28nm FPGA (Kintex-7) and 40nm FPGA (Artix-7). In order to test the portability of our design, we are operating our design with respective frequency of different mobile architecture. For thermal analysis of our energy efficient design, we have taken temperatures of four different regions from reference. Latin Unicode reader takes 16-bit hexadecimal code of alphabet and clock input. At the end we can conclude that the maximum power consumption is at 2.2GHz and minimum power consumption is at 1.2GHz. When we talk in terms of temperature we can see that maximum power is consumed at 329.85K and minimum power is consumed at 294.15K. And also the power dissipation is less in the case of 40nm (Artix-6) and is more in the case of 28nm (Kintex-7). Changing the parameter (Temperature) doesn't affect the clock power in both cases (Gated and Non-gated).

Keywords: *Clock Gating, Latin, Unicode, FPGA, Energy Efficient, VLSI, Thermal Aware*

1. Introduction

With of international standards (Unicode) it is now possible to develop and deploy online content in local languages across the globe [1]. Unicode is one of the fundamental technological building blocks for exchange of textual information across the globe with the help of computers [14]. Latin Unicode takes input as an alphabet and gives corresponding output like ASCII Digits, ASCII Punctuation, Control Character, C0 Control, Invalid Sign, Lowercase, and Uppercase. Range of Latin Script is 0000 to 007F. Ranges of outputs are shown in Table 1.

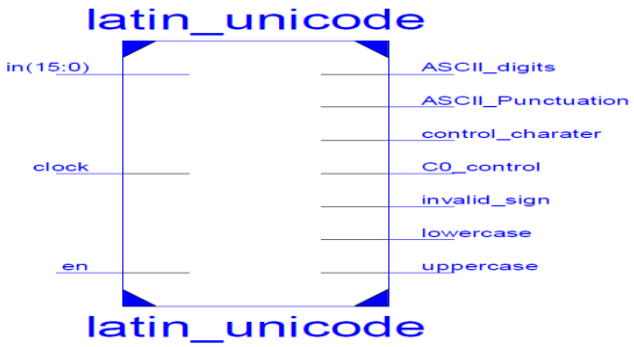

Figure 1. Symbol of Latin Unicode Reader

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Table 1. Range of Latin Unicode Scripts with O/P Port

Character Type (O/P Port)	Unicode Range
ASCII_Digits	0030-0039
ASCII_Punctuation	0020-002F, 003A-0040, 005B-0060, 007B-007E
Control_Character	007F
C0_control	0000-001F
Invalid Sign	-
Lowercase	0041-005A
Uppercase	0061-007A

Table 2. Set of Frequencies Taken In Consideration

Frequency	Mobile set
1400Mega Hz	Nokia Lumia 710
1.2Giga Hz	Samsung Galaxy Core
2100Mega Hz	iPhone6
1700Mega Hz	HTC/T
1800Mega Hz	Micromax X091
2.2Giga Hz	Sony Xperia Z1

Latch free, latch based, and flip-flop based clock gating are clock gating technique as illustrated in Figure 2. Our design is based on 28nm FPGA and 40nm FPGA and the code has been tested on Kintex-7 and Artix-7 FPGA. Clock gating technique is used to achieve energy efficiency in sequential circuit [3], 8-bit ALU [4] and 64-bit ALU [5], global reset ALU [6], and ITC'99-b01 Benchmark Circuit [7]. In [8], architecture of multiplier based on mathematics is discussed. Our design is based on 28nm FPGA (Kintex-7) and 40nm FPGA (Artix-7). For Kintex-7 device used is XC7K160T, package used is FBG676 and it is working on -3 speed grade. Same for Artix-7 the deviceused is XC7Q100T, package used is 2CSG324 and it is working on -2 speed grade.XPower Analyzer is used for power analysis.

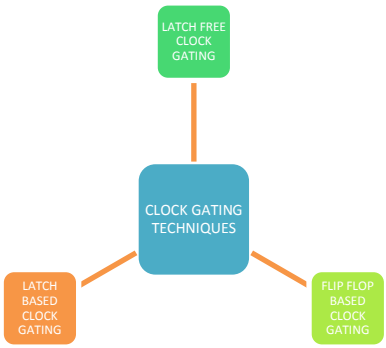

Figure 2. Clock Gating Techniques

We have taken different set of frequencies mentioned in Table 2, and have done power analysis by using Clock Gating Technique. The Clock Gating includes Gated and Non-Gated methods and by both methods we calculate Total power and Clock power. This can be shown in Figure 3. There are different techniques like capacitance scaling [8], thermal scaling [10], clock gating [11], various design goals [12], impedance matching, scalable scheme [9] and mapping. In this paper power analysis is our main concern and we have studied about the power analysis in this paper at different frequencies. Temperature is not kept constant it is varying and hence thermal analysis has also been done. For thermal

analysis of our energy efficient design, we have taken temperatures of four different regions from reference [13]. Median temperature of Delhi is 40^0C and standard normal temperature is 21^0C [13]. In order to test the portability of our design [15-16], we are operating our design with respective frequency of different mobile architecture as illustrated in Table 2. *e.g.*, Operating frequency of iPhone 6 is 2100MHz.

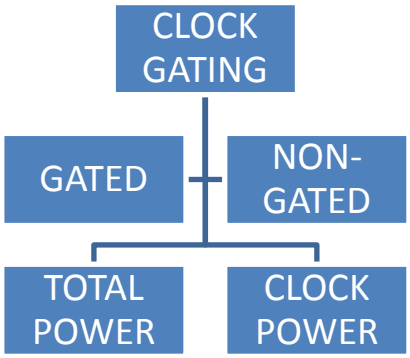

Figure 3. Clock Gating

2. Power Analysis

A. Power Analysis at 329.85 Kelvin Ambient Temperature

Table 3. Effect of Clock Gating and 28nm FPGA on Power Dissipation

Frequency	**Non-gated Total Power**	**Non-gated Clock Power**	**Gated Total Power**	**Gated Clock Power**
1400MHz	0.118	0.002	0.124	0.007
1.2GHz	0.117	0.002	0.121	0.006
2100MHz	0.123	0.004	0.131	0.010
1700MHz	0.120	0.003	0.127	0.008
1800MHz	0.120	0.003	0.128	0.009
2.2GHz	0.123	0.004	0.132	0.011

There is 4.83% for 1400MHz, 3.30% for 1.2GHz, 6.10% for 2100MHz, 5.51% for 1700MHz, 6.25% for 1800MHz, 6.81% for 2.2GHz saving in total power dissipation when we use non-gated clock instead of gated one on 28nm FPGA and temperature is 329.85K ambient temperature as illustrated in Table 3 and Figure 4.

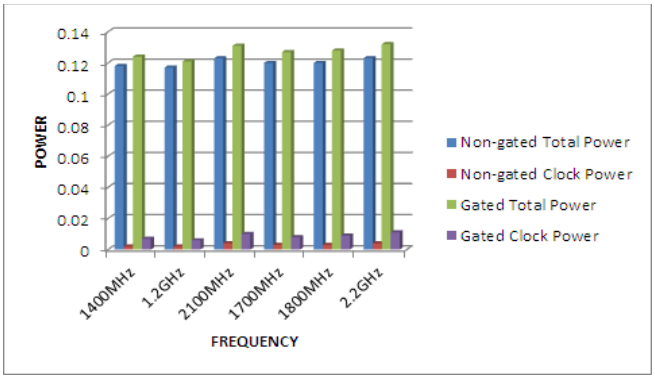

Figure 4. Power Analysis at 329.85Kon 28nm FPGA

Table 4. Effect of Clock Gating and 40nm FPGA on Power Dissipation

Frequency	Non-gated Total Power	Non-gated Clock Power	Gated Total Power	Gated Clock Power
1400MHz	0.100	0.003	0.105	0.007
1.2GHz	0.098	0.002	0.103	0.006
2100MHz	0.105	0.004	0.113	0.010
1700MHz	0.102	0.003	0.108	0.008
1800MHz	0.102	0.003	0.110	0.009
2.2GHz	0.105	0.004	0.114	0.011

There is 4.76% for 1400MHz, 4.85% for 1.2GHz, 7.07% for 2100MHz, 5.55% for 1700MHz, 7.27% for 1800MHz, 7.89% for 2.2GHz saving in total power dissipation when we usenon-gated clock instead of gated one on 40nm FPGA and temperature is 329.85K ambient temperature as illustrated in Table 4 and Figure 5.

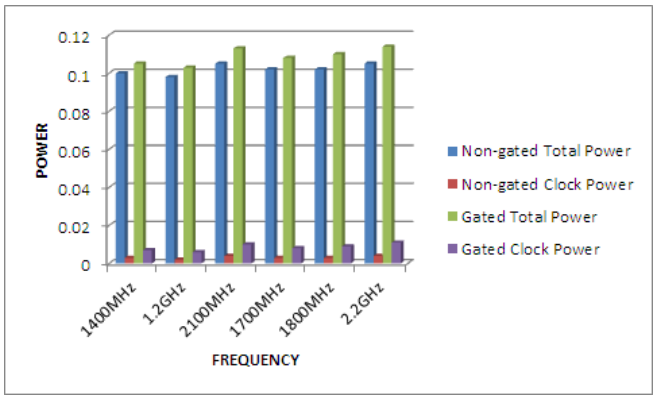

Figure 5. Total Power Analysis at 56.7°Celsius on 40nm FPGA

B. Power Analysis at 326.65K Ambient Temperature

Table 5. Effect of Clock Gating and 28nm FPGA on Power Dissipation

Frequency	Non-gated Total Power	Non-gated Clock Power	Gated Total Power	Gated Clock Power
1400MHz	0.107	0.002	0.113	0.007
1.2GHz	0.105	0.002	0.110	0.006
2100MHz	0.111	0.004	0.120	0.010
1700MHz	0.109	0.003	0.116	0.008
1800MHz	0.109	0.003	0.117	0.009
2.2GHz	0.112	0.004	0.121	0.011

There is 5.30% for 1400MHz, 4.54% for 1.2GHz, 7.5% for 2100MHz, 6.03% for 1700MHz, 6.83% for 1800MHz, 7.43% for 2.2GHz saving in total power dissipation when we use non-gated clock instead of gated one on 28nm FPGA and temperature is 326.65K ambient temperature as illustrated in Table 5 and Figure 6.

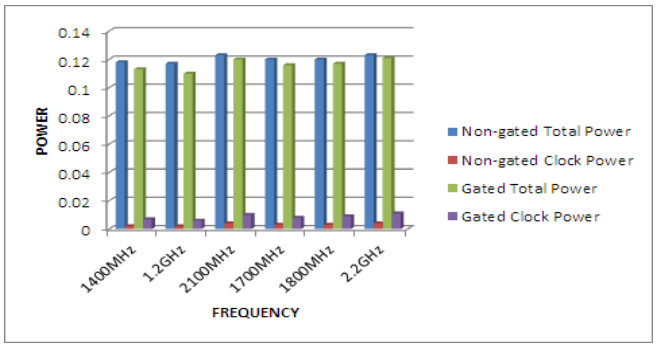

Figure 2. Power Analysis at 326.65Kon 28nm FPGA

Table 6. Effect of Clock Gating and 40nm FPGA on Power Dissipation

Frequency	Non-gated Total Power	Non-gated Clock Power	Gated Total Power	Gated Clock Power
1400MHz	0.091	0.003	0.097	0.007
1.2GHz	0.090	0.002	0.095	0.006
2100MHz	0.096	0.004	0.104	0.010
1700MHz	0.093	0.003	0.100	0.008
1800MHz	0.094	0.003	0.101	0.009
2.2GHz	0.097	0.004	0.106	0.011

There is 6.18% for 1400MHz, 5.26% for 1.2GHz, 7.69% for 2100MHz, 7% for 1700MHz, 7% for 1800MHz, 8.49% for 2.2GHz saving in total power dissipation when we use non-gated clock instead of gated one on 40nm FPGA and temperature is 326.65K ambient temperature as illustrated in Table 6 and Figure 7.

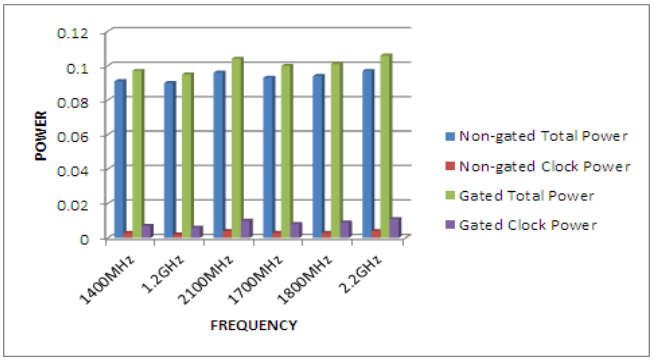

Figure 7. Power Analysis at 326.65K on 40nm FPGA

C. Power Analysis at 313.15K Ambient Temperature

Table 7. Effect of Clock Gating and 28nm FPGA on Power Dissipation

Frequency	Non-gated Total Power	Non-gated Clock Power	Gated Total Power	Gated Clock Power
1400MHz	0.073	0.002	0.079	0.007
1.2GHz	0.072	0.002	0.077	0.006
2100MHz	0.078	0.004	0.087	0.010
1700MHz	0.075	0.003	0.082	0.008
1800MHz	0.076	0.003	0.085	0.009
2.2GHz	0.079	0.004	0.088	0.011

There is 7.59% for 1400MHz, 6.49% for 1.2GHz, 10.34% for 2100MHz, 8.53% for 1700MHz, 10.58 % for 1800MHz, 10.22% for 2.2GHz saving in total power dissipation when we use non-gated clock instead of gated one on 28nm FPGA and temperature is 313.15K ambient temperature as illustrated in Table 7 and Figure 8.

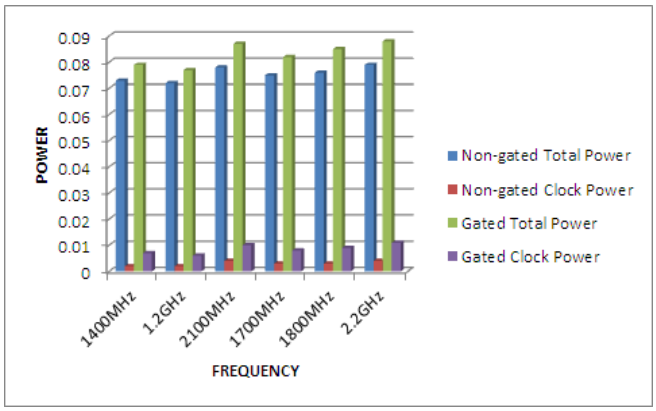

Figure 8. Power Analysis at 313.15K on 28nm FPGA

Table 8. Effect of Clock Gating and 40nm FPGA on Power Dissipation

Frequency	Non-gated Total Power	Non-gated Clock Power	Gated Total Power	Gated Clock Power
1400MHz	0.066	0.003	0.071	0.007
1.2GHz	0.065	0.002	0.069	0.006
2100MHz	0.071	0.004	0.079	0.010
1700MHz	0.068	0.003	0.075	0.008
1800MHz	0.069	0.003	0.076	0.009
2.2GHz	0.071	0.004	0.080	0.011

There is 70.42% for 1400MHz, 5.79% for 1.2GHz, 10.12% for 2100MHz, 9.33% for 1700MHz, 9.21% for 1800MHz, 11.25% for 2.2GHz saving in total power dissipation when we use non-gated clock instead of gated one on 40nm FPGA and temperature is 313.15K ambient temperature as illustrated in Table 8 and Figure 9.

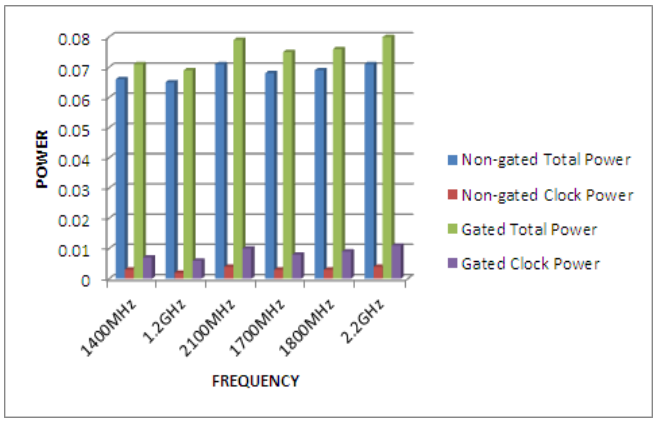

Figure 9.Power Analysis at 313.15K on 40nm FPGA

D. Power Analysis at 294.15KAmbient Temperature

Table 9. Effect of Clock Gating and 28nm FPGA on Power Dissipation

Frequency	Non-gated Total Power	Non-gated Clock Power	Gated Total Power	Gated Clock Power
1400MHz	0.050	0.002	0.055	0.007
1.2GHz	0.048	0.002	0.053	0.006
2100MHz	0.054	0.004	0.063	0.010
1700MHz	0.051	0.003	0.058	0.008
1800MHz	0.052	0.003	0.060	0.009
2.2GHz	0.055	0.004	0.064	0.011

There is 9.09% for 1400MHz, 9.43% for 1.2GHz, 14.28% for 2100MHz, 12.06% for 1700MHz, 13.33% for 1800MHz, 14.06% for 2.2GHz saving in total power dissipation when we use non-gated clock instead of gated one on 28nm FPGA and temperature is 294.15K ambient temperature as illustrated in Table 9 and Figure 10.

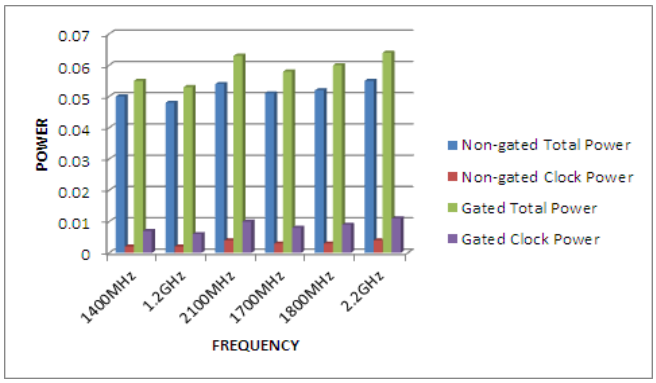

Figure 10. Power Analysis at 294.15K on 28 nm FPGA

Table 10. Effect of Clock Gating and 40nm FPGA on Power Dissipation

Frequency	Non-gated Total Power	Non-gated Clock Power	Gated Total Power	Gated Clock Power
1400MHz	0.048	0.003	0.053	0.007
1.2GHz	0.047	0.002	0.051	0.006
2100MHz	0.053	0.004	0.061	0.010
1700MHz	0.050	0.003	0.057	0.008
1800MHz	0.051	0.003	0.058	0.009
2.2GHz	0.053	0.004	0.062	0.011

There is 9.43% for 1400MHz, 7.84% for 1.2GHz, 13.11% for 2100MHz, 12.28% for 1700MHz, 12.06% for 1800MHz, 14.51% for 2.2GHz saving in total power dissipation when we use non-gated clock instead of gated one on 40nm FPGA and temperature is 294.15K ambient temperature as illustrated in Table 10 and Figure 11.

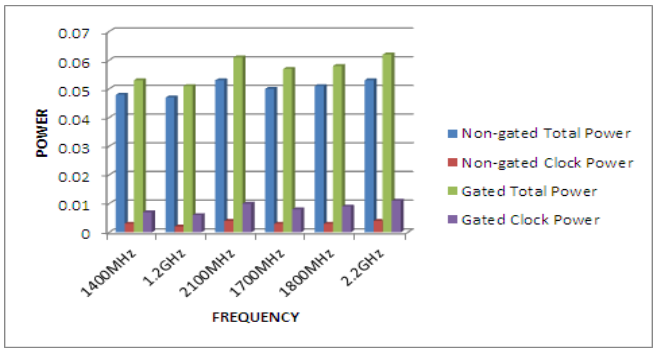

Figure 11. Power Analysis at 294.15K on 28 nm FPGA

E. Power Analysis ForDifferent Frequencies andDifferent Temperature on 28nm FPGA

Table 11. Variation in Power Dissipation with Frequency & Thermal Scaling

Frequency	329.85K	326.65K	313.15K	294.15K
1400MHz	0.124	0.113	0.079	0.055
1.2GHz	0.121	0.110	0.077	0.053
2100MHz	0.131	0.120	0.087	0.063
1700MHz	0.127	0.116	0.082	0.058
1800MHz	0.128	0.117	0.085	0.060
2.2GHz	0.132	0.121	0.088	0.064

From Table 11 and Figure 12, we can state that the maximum power consumption is at 2.2GHz and minimum power consumption is at 1.2GHz. When we talk in terms of temperature, we can see that maximum power is consumed at 329.85K and minimum power is consumed at 294.15K.

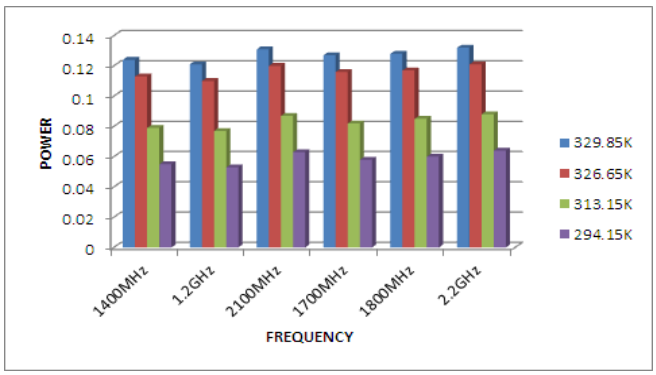

Figure 12. Power Dissipation with Frequency & Temperature Variation

F. Power Analysis For Different Frequencies & Different Temperature on 40nm FPGA

Table 12. Variation in Power Dissipation with Frequency & Thermal Scaling

Frequency	329.85K	326.65K	313.15K	294.15K
1400MHz	0.105	0.097	0.071	0.053
1.2GHz	0.103	0.095	0.069	0.051
2100MHz	0.113	0.104	0.079	0.061
1700MHz	0.108	0.100	0.075	0.057
1800MHz	0.110	0.101	0.076	0.058
2.2GHz	0.114	0.106	0.080	0.062

From Table 12 and Figure 13, we can state that the maximum power consumption is at 2.2GHz and minimum power consumption is at 1.2GHz. When we talk in terms of temperature we can see that maximum power is consumed at 329.85K and minimum power is consumed at 294.15K.

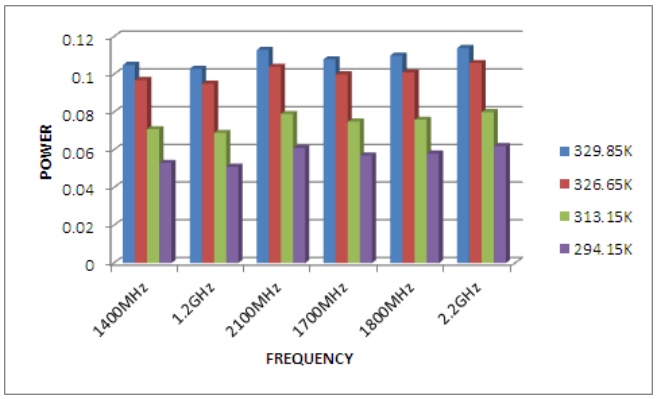

Figure 13. Power Dissipationwith Frequency& Temperature Variation

G. Comparison between Kintex-7 and Artix-7 FPGA

Table 13. Total Power Analysis for 40nm and 28nm FPGA at 329.85K

Frequency	Kintex-7	Artix-7
1400MHz	0.124	0.105
1.2GHz	0.121	0.103
2100MHz	0.131	0.113
1700MHz	0.127	0.108
1800MHz	0.128	0.110
2.2GHz	0.132	0.114

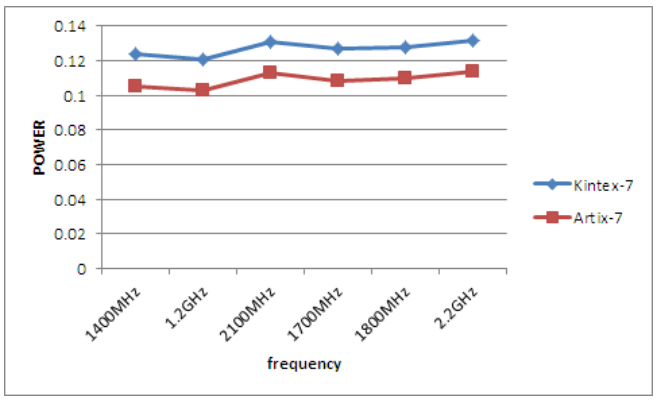

Figure 14. Total Power for Different Frequency and FPGA at 329.85K

Table 14. Total Power Analysis for 40nm and 28nm FPGA at 294.15K

Frequency	Kintex-7	Artix-7
1400MHz	0.055	0.053
1.2GHz	0.053	0.051
2100MHz	0.063	0.061
1700MHz	0.058	0.057
1800MHz	0.060	0.058
2.2GHz	0.064	0.062

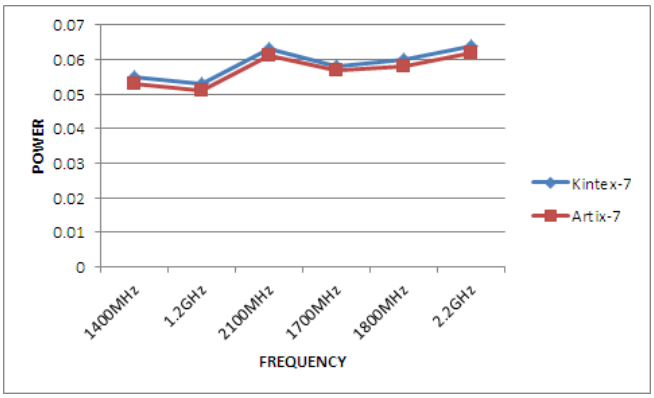

Figure 15. Total Power for Different Frequency and FPGA at 294.15K

From Table13-14 and Figure 14-15, we can state that the power dissipation is less in the case of 40nm (Artix-6) and is more in the case of 28nm (Kintex-7). Changing the parameter (Temperature) doesn't affect the clock power in both cases (Gated and Non-gated).

3. Conclusion

Our design is based on 28nm FPGA (Kintex-7) and 40nm FPGA (Artix-7). In order to test the portability of our design, we are operating our design with respective frequency of different mobile architecture. In this paper we have done frequency scaling technique to obtain energy efficient design. For thermal analysis of our energy efficient design, we have taken temperatures of four different regions from reference. Latin Unicode reader takes 16-bit hexadecimal code of alphabet and clock input. And also the power dissipation is less in the case of 40nm (Artix-6) and is more in the case of 28nm (Kintex-7). Changing the parameter (Temperature) doesn't affect the clock power in both cases (Gated and Non-gated).

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