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A 12-bit 100kS/s SAR ADC for Biomedical Applications

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Abstract

This paper describes a 12-bit 100kS/s successive approximation register analog-to-digital converter (SAR ADC) for biomedical system. Both top-plate sampling technique and VCM-based switching technique are applied to the capacitor digital-to-analog converter (CDAC) to implement a 12-bit SAR ADC with 10-b capacitor array DAC. To enhance the linearity of proposed ADC, thermometer decoder is used in capacitor array DAC. Switching-energy minimization technique, asynchronous control with a low-power delay circuit and true single phase clocking (TSPC) D_FF are also adopted to reduce power consumption. Simulation results show that the proposed ADC achieves the SNDR of 70.97dB, the SDFR of 80.23dB and the ENOB of 11.49b with the CMOS 0.18μm technology. Total power consumption is 11.16μW under the supply voltage of 1.8V at the sampling frequency of 100 kHz. And the figure of merit (FoM) is 38.79fJ/conversion-steps.

Keywords: *Analog-to-digital converter (ADC), SAR ADC, thermometer decoder DAC, dummy Cap switching, energy-efficient, biomedical system*

1. Introduction

Due to the good power efficiency, the SAR type analog-to-digital converter (ADC) is widely used in biomedical system [1-3]. In biomedical applications such as electro-cardiogram (ECG) and electro-encephalogram (EEG), the resolution of ADC over 10-bit to 12-bit is required for high accuracy in analog front end. Since the SAR ADC is substantially implemented with the capacitor array in internal DAC, the capacitor array in 12-bit DAC requires large chip area if it is implemented with direct binary weighted capacitor array. And as the recent biomedical devices are implemented with portable form, low power consumption is essential design condition for battery operated system. In accordance with this trend, this paper focuses on the implementation of 12-bit SAR type ADC with low power consumption and small chip area.

The organization of this paper is as follows: section 2 presents the architecture of the proposed 12-bit SAR ADC, section 3 describes the details of the proposed 12-bit SAR ADC with 10-bit DAC, low power delay circuits [4], section 4 reports the simulation results and performance summary, and finally the conclusion is in section 5.

2. Architecture of the Proposed ADC

Figure 1 shows the block diagram of proposed 12-bit SAR ADC. It has differential charge redistribution DAC, an output offset cancelled comparator, a SAR and an asynchronous control block. The proposed 12-bit SAR ADC used top plate sampling technique [5] and also dummy capacitor switching technique based on common mode

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voltage (VCM) [6] to reduce the chip area and power consumption. Split capacitor arrays with attenuation capacitor in differential DAC are also adopted to reduce hardware as shown in Figure 2. In addition, for the enhanced accuracy, output offset cancelled comparator and thermometer decoder DAC is used. And, for the low power consumption in asynchronous digital control block, leakage based low power delay circuit is adopted.

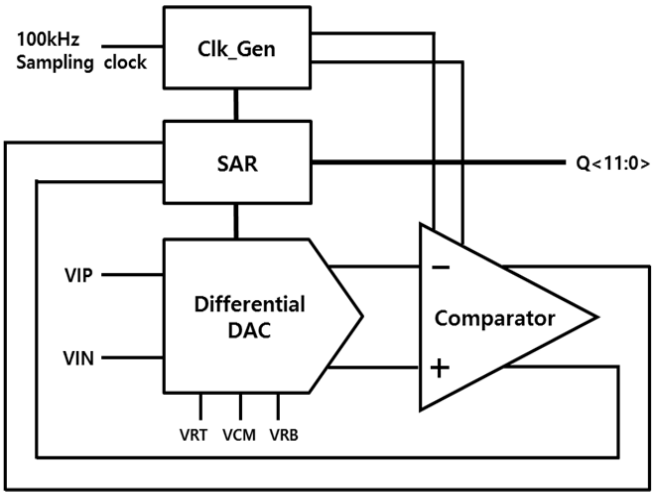


Figure 1. Block Diagram of the 12-bit SAR ADC

3. Proposed ADC

3.1. Proposed DAC

Figure 2, shows the architecture of 10-bit DAC in 12-bit ADC. The thermometer decoder is applied to the MSB array in DAC to improve the linearity of the SAR ADC. In sampling mode, input signal is applied to the top plate of differential capacitor array. In holding mode, DAC holds VIN and VIP. Since the MSB value is determined by comparing the initial holding values of differential DAC, the MSB capacitor array in conventional DAC is not needed. This technique enables to reduce the total capacitance by half compared to the conventional design. By switching the reference voltage on the last unit capacitor (dummy capacitor) between (VRT, VCM) instead of (VRT, VRB), additional LSB comparison is allowed. This dummy capacitor switching technique based on VCM in LSB decision could reduce the lower sub-capacitor array to another half. As a result, this V_{CM}-based LSB switching technique [6], together with aforementioned top-plate sampling technique [5], allowed us to implement a 12-bit ADC with a 10-bit capacitor array DAC.

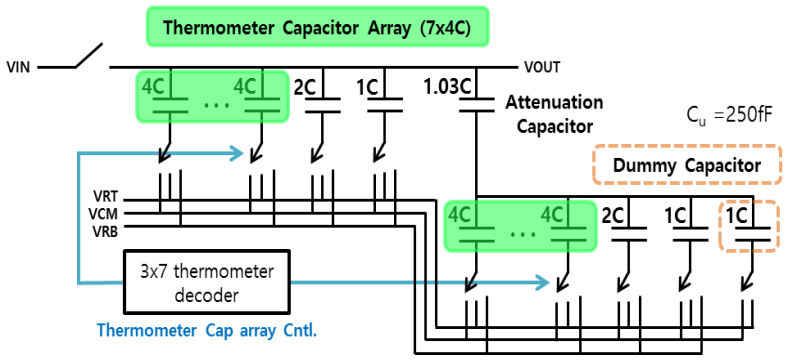
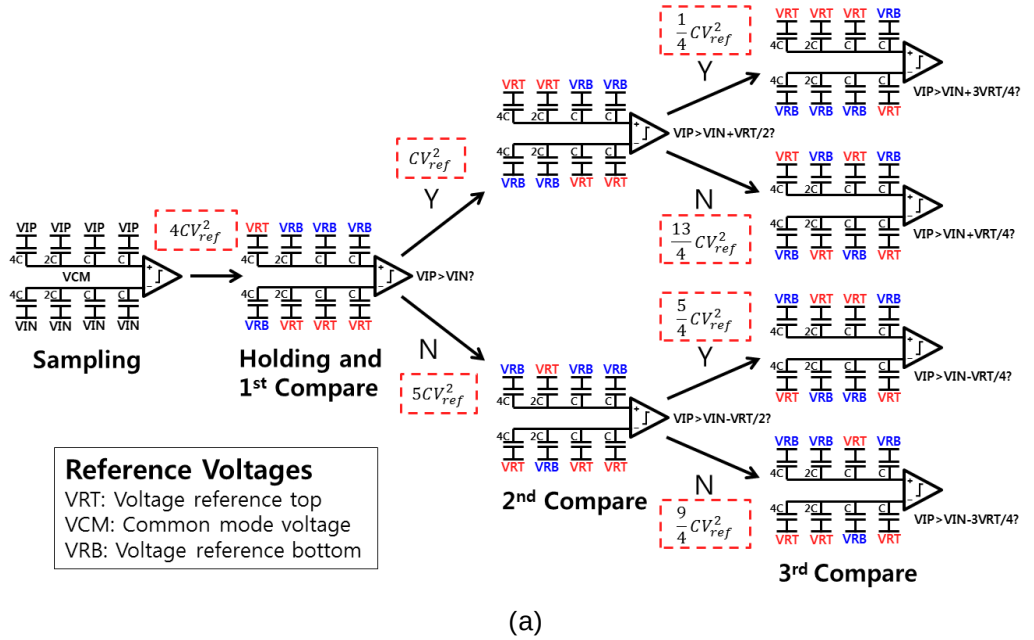


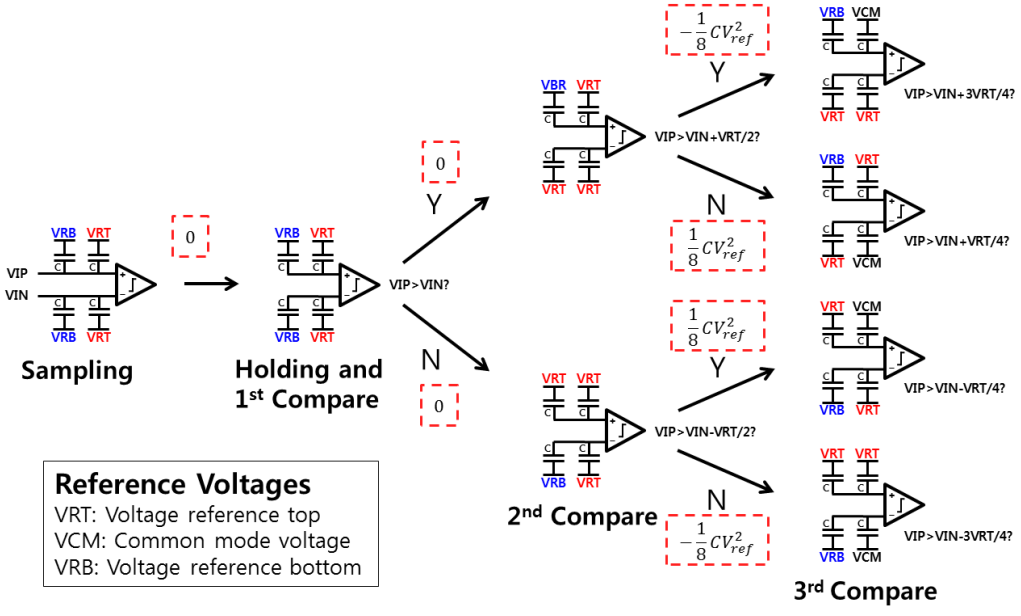
Figure 2. Diagram of the Proposed 10-Bit DAC in 12-Bit ADC

3.2. Dummy Capacitor Switching Technique

Figure 3, (a) shows the conventional switching process of 3-bit DAC as an example. In the sampling periods, both VIP and VIN are sampled to the bottom plate of capacitor arrays. During the 1st conversion process in holding periods, the MSB capacitors are switched to voltage reference top (VRT) and other capacitors are connected to voltage reference bottom (VRB) in the upper array of DAC. And reverse reference voltages are also connected in the lower array of DAC.



(a)



(b)

Figure 3. (a) Conventional Switching Process with 3b DAC Example (b) Implementation of the Low Switching Energy Process with 3b DAC Example

In this case, all the capacitors switched the reference voltage and hence consume the switching power of $4CV^2$. [7] Also, during the 2nd and 3rd conversion process in holding period, this conventional switching technique consumes more switching energy as shown Figure 3, (a).

Figure 3, (b) shows the process of proposed low switching energy technique with 3-bit DAC as a conceptual example. Capacitors in proposed DAC are one quarter of capacitors in conventional DAC as mentioned earlier. If both VIP and VIN are sampled to the top plate of each capacitor array, there we have zero switching energy during 1st conversion. Also for the remaining LSB decisions, we need zero switching energy in 2nd conversion cycle and $1/8CV^2$ in 3rd conversion cycle, as shown Figure 3, (b).

3.3. Low Power Delay Circuits

Figure 4(a) shows the delay circuits [4] in asynchronous control block for low power consumption. In conventional delay circuits with inverters and load capacitors, a large amount of static current flows. However, the adopted delay circuits make the longer delay time without large static currents, because its leakage-based large resistance of MOS transistors and gate capacitance generate the longer RC delay as shown in Figure 4, (b). It consumes a current of 400nA when the delay circuit generates the delay of 200ns.

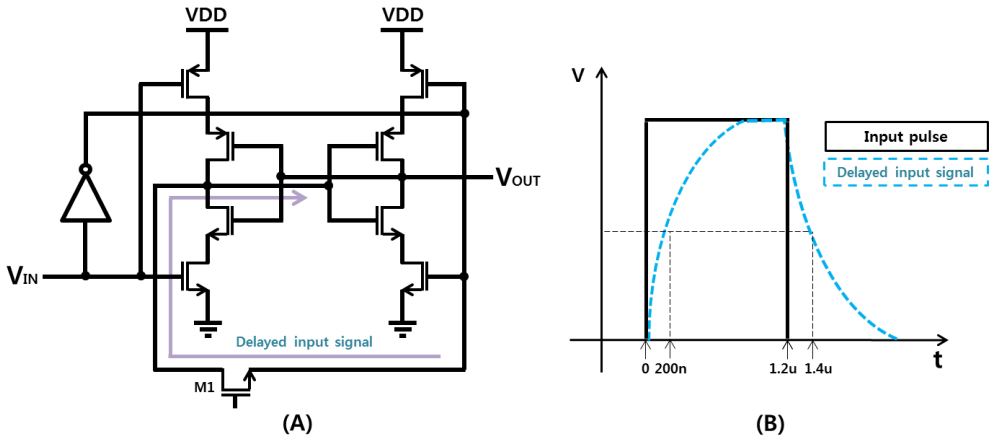


Figure 4. (a) Implementation of the Low Power Delay Circuits (b) Input Pulse and Output Pulse with the Delay of 200ns

4. Simulation Results and Performance Summary

The chip was implemented with a 0.18μm CMOS technology. The core area, as shown in Figure 6, is 877μm x 479 μm, excluding pads. The FFT simulation results with the 21 kHz input signal at sampling rate of 100 kHz are shown in Figure 7. The proposed ADC achieves the SNDR of 70.97dB, the SFDR of 80.23dB and the ENOB of 11.49bits. The power consumes 11.16μW at a sampling frequency of 100 kHz under supply voltage of 1.8V. And the figure of merit (FoM) is 38.49fJ/conversion-steps. The performance is summarized in Table 1.

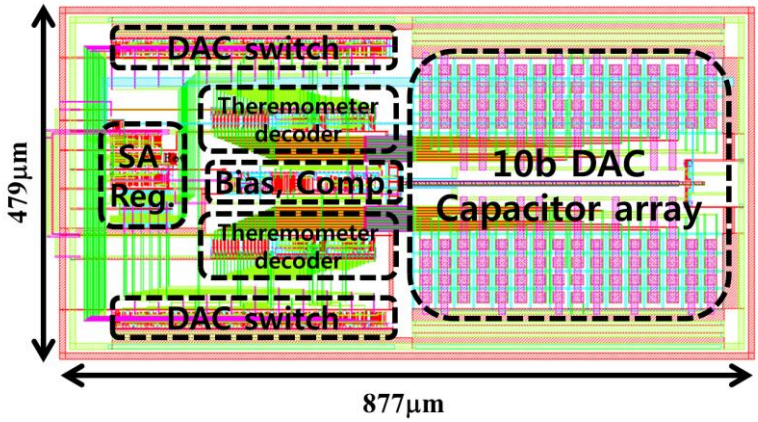


Figure 6. Chip Layout (w/o Pad)

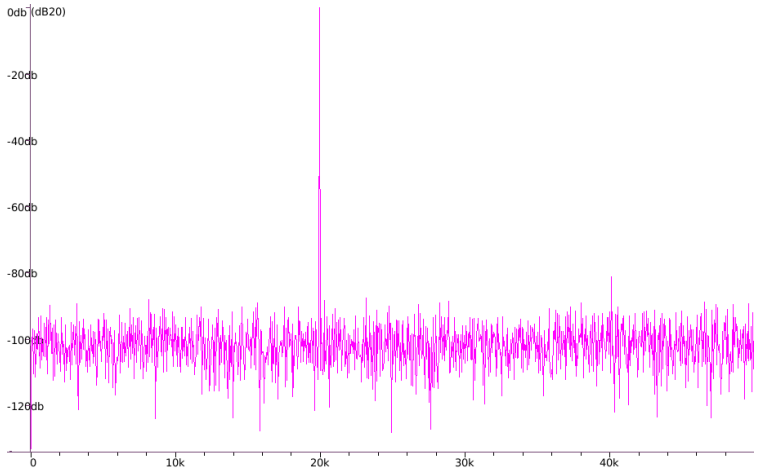


Figure 7. FFT Simulation Results

Table 1. Performance Summary

Technology	Magna 0.18μm CMOS
Resolution	12-bit
Power supply	1.8V
Sampling rate	100kHz
FoM	38.49fJ/conv.
SNDR, SFDR	70.97dB, 80.23dB
ENOB	11.49-bit
Layout	877μm x 479μm

5. Conclusion

The 12-bit 100kS/s SAR ADC was designed with both a top-plate sampling technique and a VCM-based switching technique to reduce chip area and also to reduce power consumption. Additionally, for further reducing power consumption, a leakage-based delay circuit and TSPC D_FF are used. The thermometer decoder applied to the MSB arrays in DAC improves the linearity of the SAR ADC.

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