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Integration of Standalone Solar Power System with Flying Capacitor Multilevel Inverter Contingent on Synchronous Sequential Circuit

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Abstract

The proposed system deals with the conversion of solar power into fundamental AC power by using flying capacitor multilevel inverter controlled by synchronous sequential circuits. The flying capacitor multilevel inverter controls the real and reactive power flow, deep voltage sags and short duration outages. The performance of the inverter is enhanced by using a synchronous sequential circuit, which gives the superior performance by reducing the total harmonic distortion in load voltage and capacitor voltage fluctuations. The synchronous sequential circuit based multilevel inverter offers several advantages like simpler structure, easy fault identification, cost-effectiveness and low power consumption. The performance of proposed strategy has been confirmed through simulation and hardware investigations.

Keywords*: Standalone solar power system, Flying capacitor multilevel inverter, Synchronous sequential circuits, Pulse width modulation, Total harmonic distortion*

1. Introduction

The total electrical energy consumption is increasing day by day. To meet this increasing demand, the electrical generating capacity has to be increased. Today the new capacity installation decisions are becoming complicated. However, that will need clean coal burning technologies that are fully acceptable to the public. An alternative to the coal burning, nuclear and fossil fuel power is renewable energy (hydro, wind, solar, biomass, geothermal and ocean). Hydroelectric projects have become difficult to realize because of the competing use of land and water. Among the other renewable power resources, wind and solar energy has recently experienced a rapid growth around the world. For remote villages outside two miles from the nearest transmission line, a stand-alone wind and solar energy system could be more economical [1].

After invention of the power electronic semiconductors, the controlling of power became easy in the field of generation, transmission, industrial motors and home appliances etc. The inverters are widely applied in the speed control of induction motors and standalone renewable energy systems like solar, fuel cell, magneto hydro dynamics etc. The two-level inverter has few limitations which are switching losses, constraint in the device rating and the EMI problem. In 1975 the multilevel inverters was introduce, which reduced the drawbacks of the two-level inverter and it has offered high voltage capability, low switching losses and reduced the harmonic. The multilevel inverter converts the DC into the staircase of AC. The staircase AC can be achieved by various

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topologies of multilevel inverter, such as cascaded, diode clamp, flying capacitor multilevel inverter (FCMLI) [2-4].

The n-level cascaded multilevel inverter requires a number of separate DC sources. A series of power semiconductor switches with several DC sources are used and a staircase AC waveform is synthesized. This is also called as multisource multilevel inverter [5]. The diode clamp multilevel inverter contains diodes and splitting capacitors, these splitting capacitors and switching state combination produce the staircase AC [6]. Flying capacitor multilevel inverter has flying capacitors and splitting capacitors. Due do the combination of switching states and flying capacitors the inverter produce staircase AC waveform. The diode clamp and flying capacitor multilevel inverters comes under the category of single source multilevel inverter. The flying capacitor multilevel inverter controls the real and reactive power but others cannot control the real and reactive power [7-10].

The harmonic levels are controlled by using various kinds of switching techniques such as single, multi and sinusoidal pulse width modulation techniques *etc.*, [11-14]. The digital system also plays a wider role for the control of power electronics; it is simple, cost effective and improves the system performance.

The proposed system is focuses on the implementation of the synchronous sequential circuit (SSC) to control a seven-level flying capacitor multilevel inverter for standalone solar array system. The synchronous sequential circuit is a digital system which consists of digital logic devices. The digital logic devices produce the PWM signals for controlling the seven-level inverter. The proposed system is investigated through simulation and a portable hardware model.

2. Introduction Standalone Solar System with Flying Capacitor Multilevel Inverter

The solar array is mounted on a pole and the output DC supply from the array is connected to the flying capacitor multilevel inverter. The different combination of flying capacitors allows charging and discharging in order to produce the staircase AC waveform from flying capacitor multilevel inverter. A seven-level flying capacitor multilevel inverter circuit configuration with standalone solar array is shown in Figure 1. This circuit configuration contains (n-1)(n-2)/2 flying capacitors (n-1) DC link capacitors,(n-1) semiconductor switching devices, the inverter have(n-1)/2 upper and(n-1)/2 lower side of semiconductor switching devices. The switches (S_1, S_1') (S_2, S_2') (S_3, S_3') (S_4, S_4') (S_5, S_5') and (S_6, S_6') are functioned with complementary manner like switch S_1 is ON, S_1'is OFF and vice-versa [15].

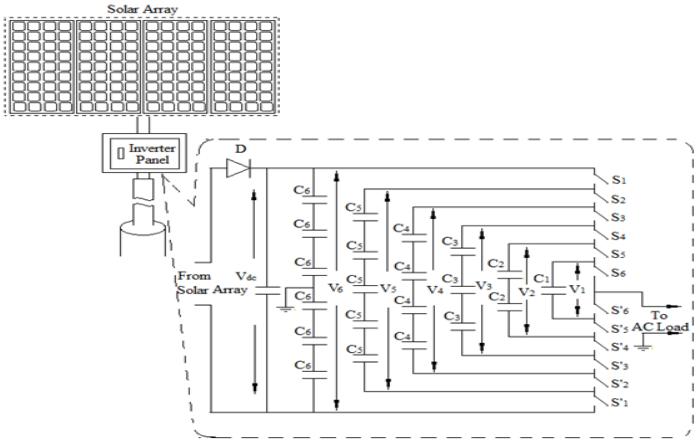


Figure 1. Seven-Level Flying-Capacitor Multilevel Inverter with Standalone Solar Array

This topology has a ladder structure of DC capacitors, the voltages in each leg of the flying capacitors is different and they have been denoted as V_1, V_2, V_3, V_4 and V_5.The switching state of the flying capacitor multilevel inverter is shown in Table 1, it denotes the sequence of switching and the corresponding voltage levels with respect to the neutral point. With the implementation of the incremental voltage of adjacent flying capacitors and the sequence of switching states, the stepped AC waveform is produced. In each switching state the voltage polarity of flying capacitors position are changed as positive, negative or no connection (NC) which is described in Table 2.

The main DC link capacitor voltage is Vdc, The inverter output voltage expressed as

$$V_o = S_1(V_6 - V_5) + S_2(V_5 - V_4) + S_3(V_4 - V_3) + S_4(V_3 - V_2) + S_5(V_2 - V_1) + S_6 V_1 - \frac{V_6}{2} \quad (1)$$

State No.	S_6	S_5	S_4	S_3	S_2	S_1	S_6'	S_5'	S_4'	S_3'	S_2'	S_1'	Volt Level
1.	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	vdc/2
2.	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	Vdc/3
3.	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	Vdc/3
4.	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	Vdc/3
5.	OFF	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	Vdc/6
6.	OFF	ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	Vdc/6
7.	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	Vdc/6
8.	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	0
9.	OFF	OFF	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	0
10.	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	0
11.	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	OFF	-Vdc/6
12.	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	OFF	ON	-Vdc/6
13.	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	-Vdc/6
14.	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	-Vdc/3
15.	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON	-Vdc/3
16.	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	-Vdc/3
17.	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	-Vdc/2

Table 1. Switching State of Flying Capacitor Multilevel Inverter

The voltage of inner most capacitor is

$$\frac{V_{dc}}{n-1} \quad (2)$$

The next innermost capacitor voltage is

$$\frac{V_{dc}}{n-1} + \frac{V_{dc}}{n-1} = \frac{2V_{dc}}{n-1} \quad (3)$$

Each flying capacitor leg voltage is incremented by

$$\frac{V_{dc}}{n-1} \quad (4)$$

Table 2. Status of Capacitor with Various Switching State

State No.	C_1	C_2	C_3	C_4	C_5	Voltage Level
1.	NC	NC	NC	NC	NC	vdc/2
2.	NC	NC	NC	NC	+	Vdc/3
3.	NC	NC	NC	+	-	Vdc/3
4.	NC	NC	+	-	NC	Vdc/3
5.	NC	-	NC	NC	NC	Vdc/6
6.	-	+	-	NC	NC	Vdc/6
7.	-	NC	+	-	NC	Vdc/6
8.	-	NC	NC	+	NC	0
9.	NC	-	NC	NC	+	0
10.	NC	NC	-	NC	NC	0
11.	+	NC	NC	NC	-	-Vdc/6
12.	+	NC	NC	-	+	-Vdc/6
13.	+	NC	-	+	NC	-Vdc/6
14.	+	NC	NC	NC	NC	-Vdc/3
15.	-	+	NC	NC	NC	-Vdc/3
16.	NC	-	+	NC	NC	-Vdc/3
17.	NC	NC	NC	NC	NC	-Vdc/2

3. Designing of Synchronous Sequential Circuit

Almost all power electronic converters are operated in the switching mode. The switches within the multilevel inverter are always turned either ON or OFF. The flow of power in the multilevel inverter is controlled by changing the switches between these two states, for this required switching pulses are designed by using a synchronous sequential circuit. The proposed system is developed for standalone solar power system with seven-level flying capacitor multilevel inverter; the level of voltage is decided by the switching pulses of synchronous sequential circuit. The synchronous sequential circuits based multilevel inverters offer several advantages like simple control of circuitry-level, ease of formulation, etc. The following steps are followed as the designing procedure of clocked sequential circuits [16-17].

This proposed system focuses on the seven-level output voltage; these levels converted to equivalent binary numbers are as shown in Figure 2. The positive or the negative waveform is being considered for designing because a sinusoidal waveform is a symmetrical waveform. The equivalent decimal numbers of phase voltages are 0, 12, 14, 15, 6, and 4. P_1, P_2, P_3 are the switching pulses of the inverter and AP is the auxiliary switching pulse.

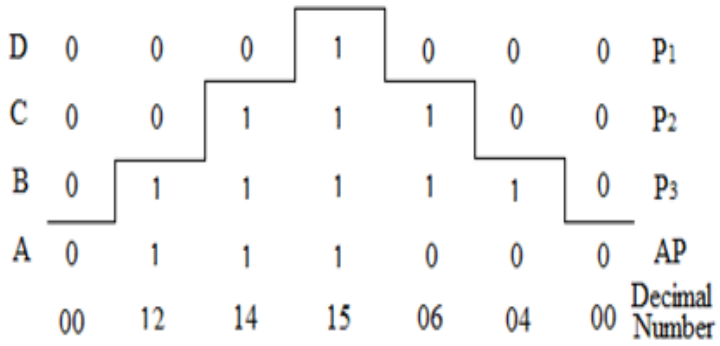


Figure 2. Seven-Level Voltage to Binary Conversion

The state diagram is drawn from the equivalent decimal numbers shown in Figure 2. The state diagram provides another useful tool when the state of the entities in the system will change in response to events. The next state of the state variables is assigned as the order of equivalent binary of phase voltage as per Figure 3.This state diagram as acting as a ring counter.

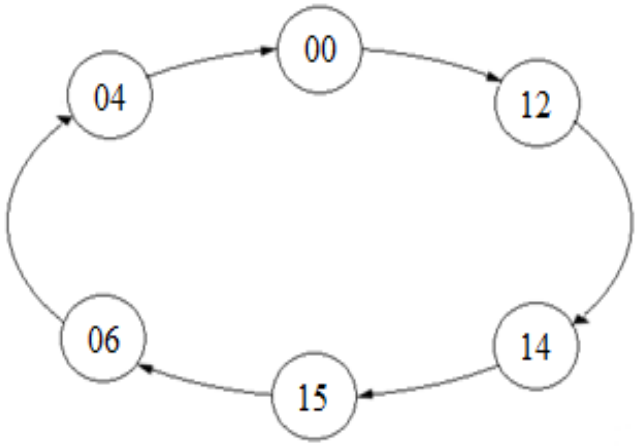


Figure 3. State Diagram

From the state diagram, the state table is developed and binary values are assigned to each state in the state table. The JK flip flop is taken for designing the synchronous sequential circuits. The JK flip flop excitation table is shown in Table 3, and the state table of synchronous sequential circuit is shown in Table 4. Present state and next state of state table has been derived from state diagram. In this state table the flip flop input of J_A, K_A, J_B, K_B, J_C, K_C and J_D, K_D is developed from present state and next state of JK flip flop excitation table.

Table 3. Excitation Table of JK Flip Flop

Q n	Q n+1	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Table 4. State Table

Decimal Number	Present State				Next State				Flip Flop							
	Q_A	Q_B	Q_C	Q_D	Q_{A+1}	Q_{B+1}	Q_{C+1}	Q_{D+1}	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	1	1	0	0	1	×	1	×	0	×	0	×
1	0	0	0	1	×	×	×	×	×	×	×	×	×	×	×	×
2	0	0	1	0	×	×	×	×	×	×	×	×	×	×	×	×
3	0	0	1	1	×	×	×	×	×	×	×	×	×	×	×	×
4	0	1	0	0	0	0	0	0	×	×	×	1	0	×	0	×
5	0	1	0	1	×	×	×	×	×	×	×	×	×	×	×	×
6	0	1	1	0	0	1	0	0	×	×	×	0	×	1	0	×
7	0	1	1	1	×	×	×	×	×	×	×	×	×	×	×	×
8	1	0	0	0	×	×	×	×	×	×	×	×	×	×	×	×
9	1	0	0	1	×	×	×	×	×	×	×	×	×	×	×	×
10	1	0	1	0	×	×	×	×	×	×	×	×	×	×	×	×
11	1	0	1	1	×	×	×	×	×	×	×	×	×	×	×	×
12	1	1	0	0	1	1	1	0	×	0	×	0	1	×	0	×
13	1	1	0	1	×	×	×	×	×	×	×	×	×	×	×	×
14	1	1	1	0	×	×	×	×	×	0	×	0	×	0	1	×
15	1	1	1	1	0	1	1	0	×	1	×	0	×	0	×	1

The Boolean function of synchronous sequential circuit has been determined from the state Table 4.The K-map method has been implemented to find the Boolean function of synchronous sequential circuit. In the K-maps plotted from Table 4, notice that the terms which are having output 1, the corresponding cells marked as 1's similarly other cells are marked as zero's and don't care condition (×). The sum of product form of Boolean expression can be plotted from the K-map, derivation of K-map are shown in Table 5 to Table 12.

Table 5. K-Map for Find J_A

	C'D'	C'D	CD	CD'
A'B'	1	×	×	×
A'B	0	×	×	0
AB	×	×	×	×
AB'	×	×	×	×
	JA = A'B'C'D'			

Table 6. K-Map for Find K_A

	C'D'	C'D	CD	CD'
A'B'	×	×	×	×
A'B	×	×	×	×
AB	0	×	1	0
AB'	×	×	×	×
	KA = ABCD			

Table 7. K-Map for Find J_B

	C'D'	C'D	CD	CD'
A'B'	1	×	×	×
A'B	×	×	×	×
AB	×	×	×	×
AB'	×	×	×	×
	JB= A'B'C'D'			

Table 8. K-Map for Find K_B

	C'D'	C'D	CD	CD'
A'B'	×	×	×	×
A'B	1	×	×	0
AB	0	×	0	0
AB'	×	×	×	×
	KB = A'BC'D'			

Table 9. K-Map for Find J_C

	C'D'	C'D	CD	CD'
A'B'	0	×	×	×
A'B	0	×	×	×
AB	1	×	×	×
AB'	×	×	×	×
	JC = ABC'D'			

Table 10. K-Map for Find K_C

	C'D'	C'D	CD	CD'
A'B'	×	×	×	×
A'B	×	×	×	1
AB	×	×	0	0
AB'	×	×	×	×
	KC = A'BCD'			

Table 11. K-Map for Find J_D

	C'D'	C'D	CD	CD'
A'B'	0	×	×	×
A'B	0	×	×	0
AB	0	×	×	1
AB'	×	×	×	×
	JD = ABCD'			

Table 12. K-Map for Find K_D

	C'D'	C'D	CD	CD'
A'B'	×	×	×	×
A'B	×	×	×	×
AB	×	×	1	×
AB'	×	×	×	×
	KD = ABCD			

From the derivation of K-Map (Table 5 to Table 12) Boolean expressions are determined

$J_A = A'B'C'D'$ (5)

$K_A = ABCD$ (6)

$J_B = A'B'C'D'$ (7)

$K_B = A'BC'D'$ (8)

$J_C = ABC'D'$ (9)

$K_C = A'BCD'$ (10)

$J_D = ABCD'$ (11)

$K_D = ABCD$ (12)

4. Execution of Synchronous Sequential Circuit

The logical circuits based synchronous sequential circuit is designed from the Boolean expression of equations 5 to 12 and the resultant logic circuit is shown in the Figure 4. The synchronous sequential circuit contains JK flip flop (A, B, C, D), four input and single output AND gate. The flip flop outputs are compliment function; it has high or low output. Four input AND gate is connected based on the derivation of K-map and the output of AND gate is connected to flip flop input as per Figure 4. The clock pulse generator produces the sequence of square pulses, which is desired for seven-level flying capacitor multilevel inverter fundamental frequency. The frequency of clock pulse generator is 650Hz.

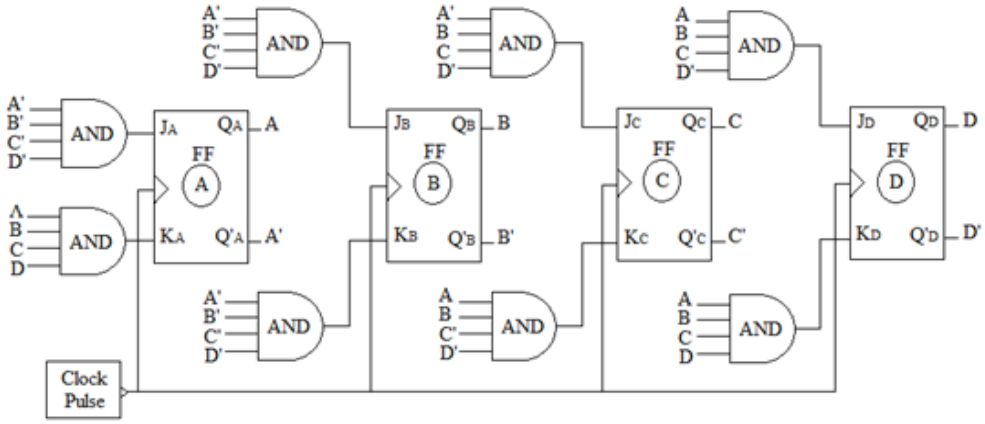


Figure 4. Synchronous Sequential Circuit

The synchronous sequential circuit produces the sequence of switching pulses, this sequence of pulses are used for both half cycles. The continuation of switching pulse is broken up in every half cycle by using breakup logic circuits it has been shown in Figure 5. The breakup logic circuit consists of a flip flop and required clock pulse is taken from the output QB of the flip flop-B.

The breakup logic circuit is designed from the possibility of switching state of flying capacitor multilevel inverter; the following functions are used for breaking the sequence of switching pulses

$$S1 = D'E' \quad (13)$$

$$S2 = C'E' \quad (14)$$

$$S3 = B'E' \quad (15)$$

$$S4 = DE' \quad (16)$$

$$S5 = CE' \quad (17)$$

$$S6 = BE' \quad (18)$$

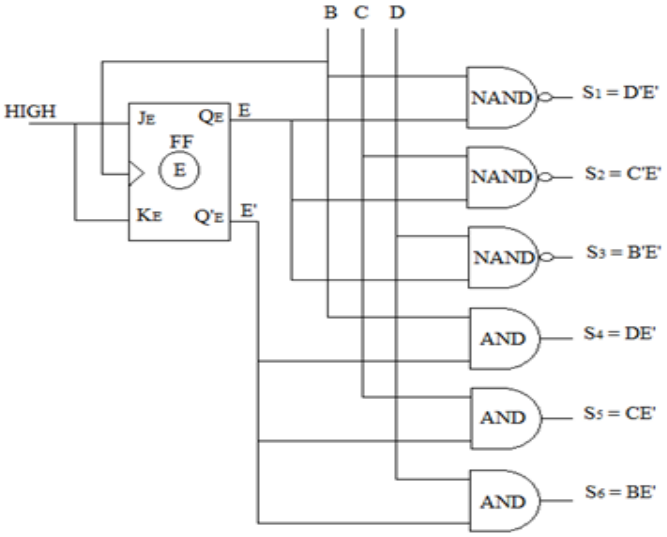


Figure 5. Break Up Logic Circuits

5. Results and Discussion

In order to verify the proposed PWM method, the extensive system is carried out through simulation and hardware. The digital modulation scheme based synchronous sequential circuit switching pulses are shown in Figure 6a, and 6b, the separated synchronous sequential circuit PWM and flying capacitor multilevel inverter switching pulses are shown in Figure 7a, 7b, 7c, and 7d.

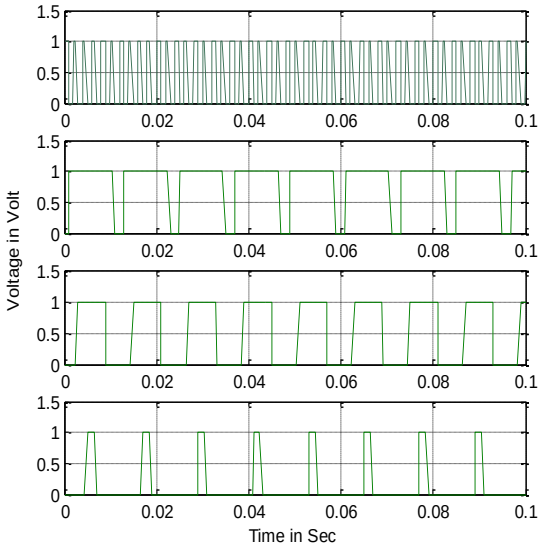
The separated six digital modulated PWM pulses are applied to seven-level multilevel inverter upper semiconductor switching devices and by using NOT gate the upper semiconductor switching's pulses are inverted and the inverted switching pulses are given to the lower semiconductor switching devices of the flying capacitor multilevel inverter. The behavior of the proposed topology has been validated based on the simulation and a prototype model. The prototype model has a solar panel, light load, clock pulse generator which has 650Hz, IRF 540 MOSFET, and 3200µF capacitors.

Clock pulse and inverter output frequency are derived from

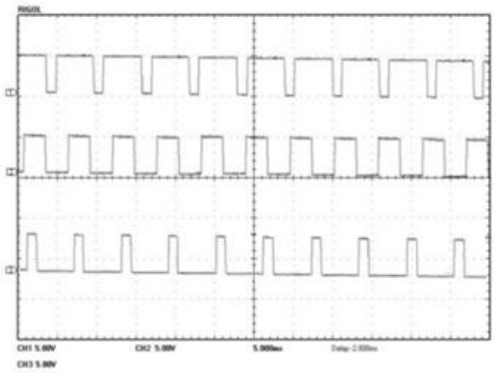
$$F_{CP} = ((n \times 2) - 1) \times F_I \quad (19)$$

$$F_I = \frac{F_{CP}}{((n \times 2) - 1)} \tag{20}$$

The valid digital modulated PWM switching combinations can synthesize a seven-level output voltage, which is shown in Figure 8a, and 8b, Total Harmonic Distortion (THD) is measured by using the digital analyzer it has shown in Figure 9a, and 9b. This synchronous sequential circuit based flying capacitor multilevel inverter obtained the output voltage 192V, frequency 50Hz and THD 16.7%. The experimental setup of simulation and prototype model of seven-level flying capacitor multilevel inverter are shown in Figure 10 and Figure 11 respectively.

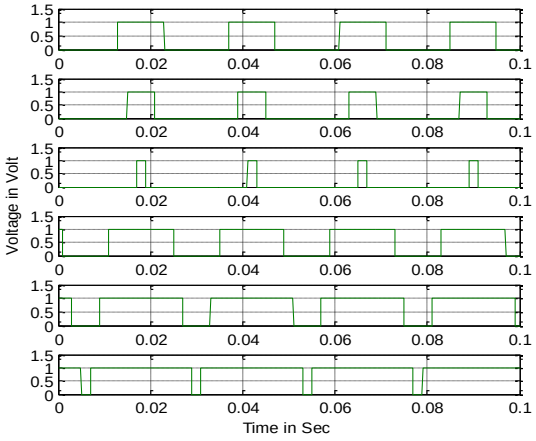


(a)



(b)

Figure 6. Switching Pulse of Synchronous Sequential Circuit, (a) Simulation Results of Clock Pulse, Flip Flop E, C, D (b) Prototype Model Results of Flip Flop E, C, D



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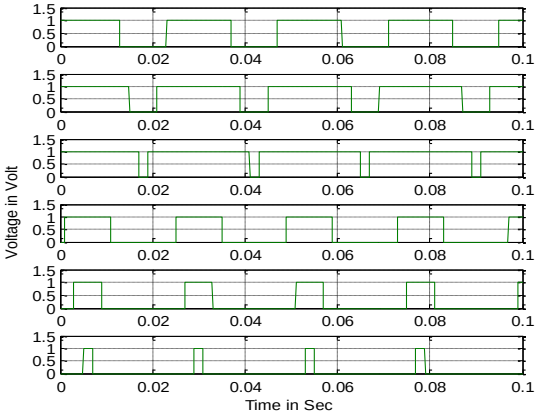

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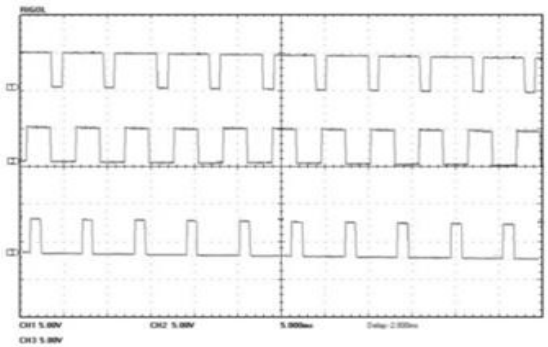

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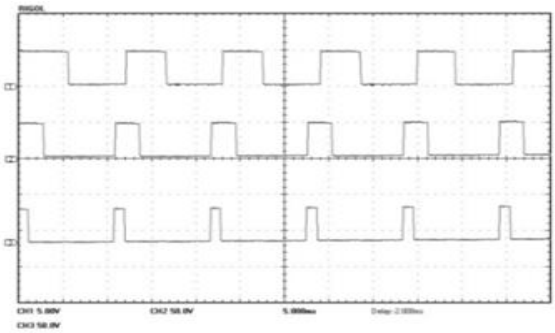
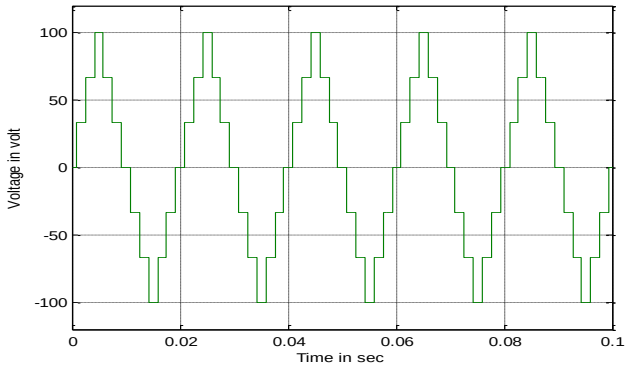
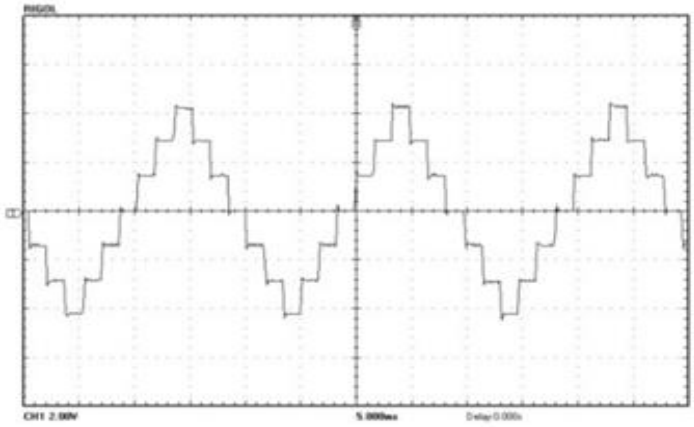


(d)

Figure 7. Switching Pulse of Flying Capacitor Multilevel Inverter, (a) Simulation Results of S1 – S6, (b) Simulation Results of S'1 –S'6, (c) Prototype Model Results of S1 – S3, (d) Prototype Model Results of S4 – S6

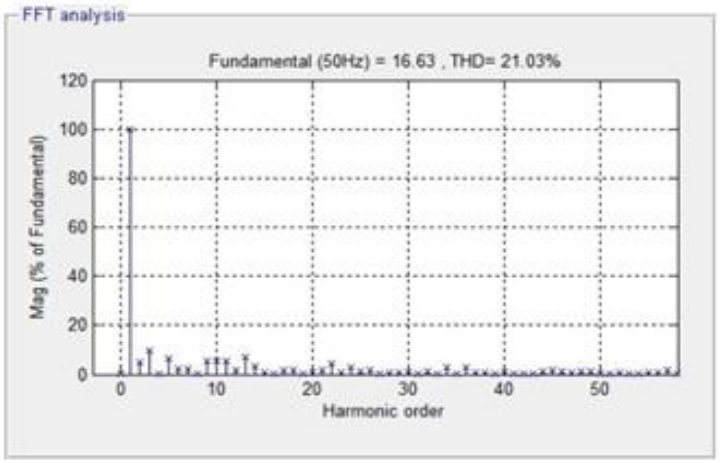


(a)



(b)

Figure 8. Voltage Waveform of Flying Capacitor Multilevel Inverter, (a) Inverter Output from Simulation Model (b) Inverter Output from Prototype Model



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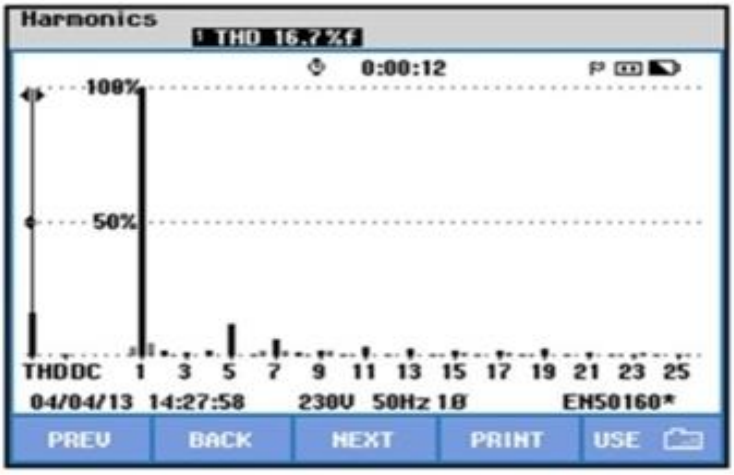

(b)

Figure 9. Total Harmonic Distortion of Voltage Waveform (a) THD Result of Simulation Model (b) THD Result of Prototype Model

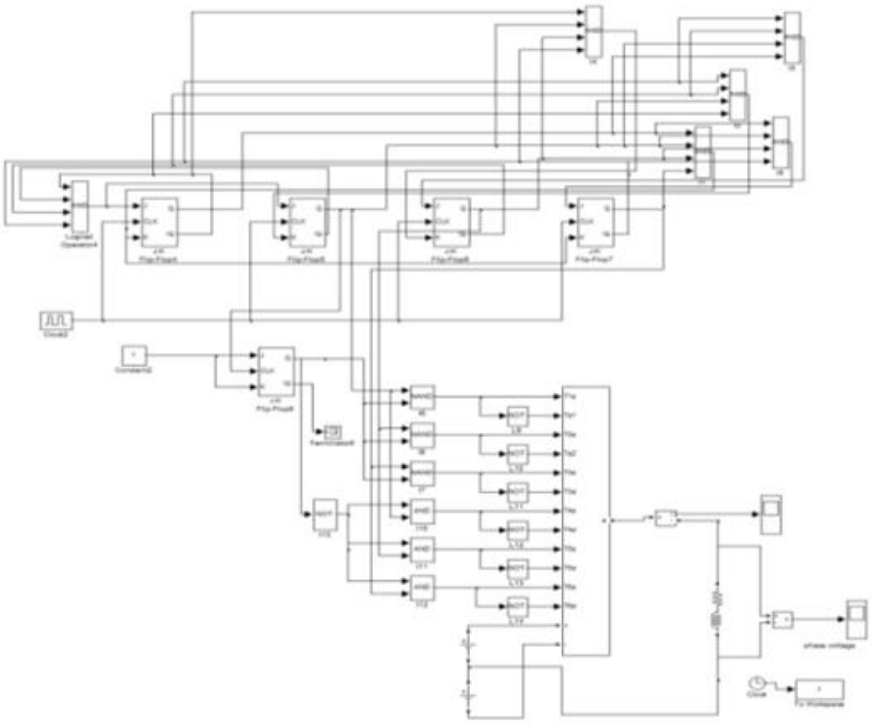

Figure 10. Experimental Setup of Simulation

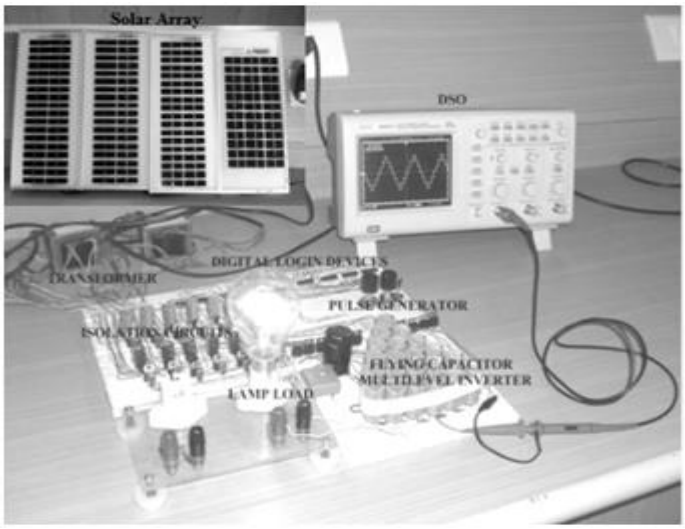

Figure 11. Experimental Setup of Prototype Model

6. Comparative Study of SSC PWM and SHE PWM

The selective harmonic elimination pulse width modulation (SHE PWM) control circuit of seven-level flying capacitor multilevel inverter is shown in Figure 12. The control circuit consists of a RC phase shift oscillator, triangular wave generator, positive clamping, negative clamping and comparator circuits. It has many numbers of active and passive components. The fault identification of selective harmonic elimination PWM control circuit is difficult compared to the synchronous sequential circuit (SSC). The synchronous sequential circuit has digital logic devices, it is simple to identify the faults

and easy to replace the logic devices. For standalone solar system, synchronous sequential circuit based multilevel inverter has a simple structure, it is cost-effective, and it has low power consumption and fast dynamic response.

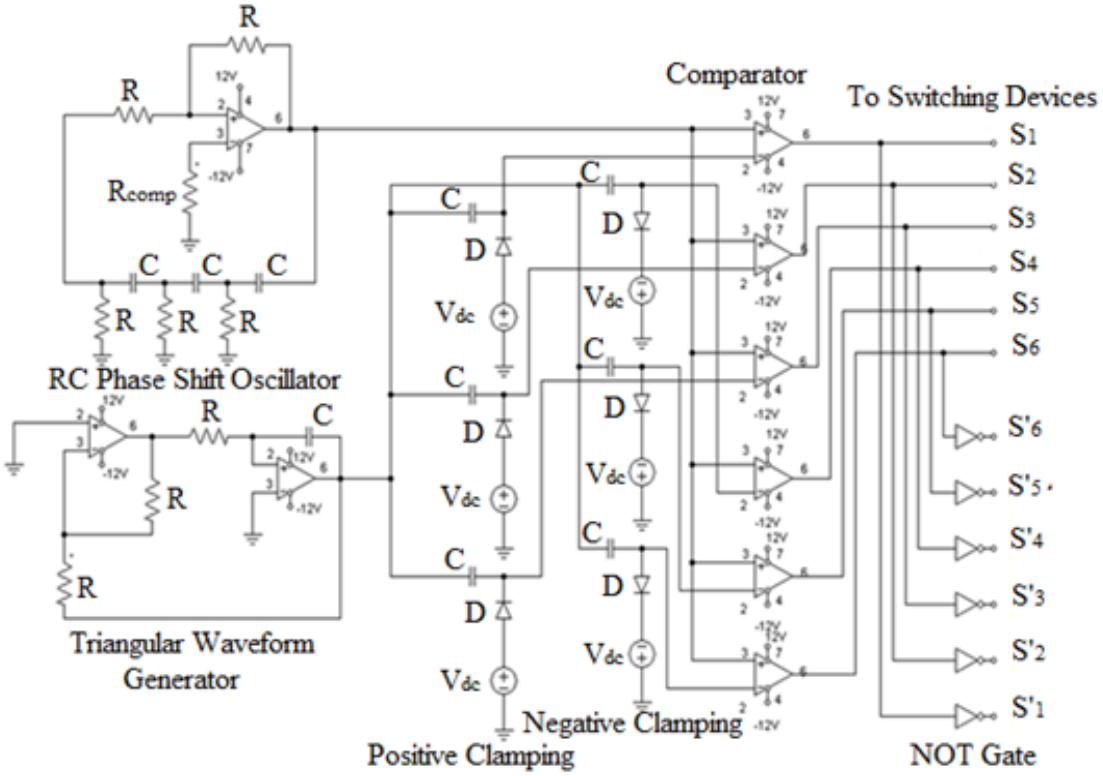

Figure 12. Selective Harmonic Elimination PWM Circuits for Seven–Level FCMLI

7. Conclusion

This paper proposes a new switching topology designed for seven-level flying capacitor multilevel inverter with standalone solar system, it provides the stepped sinusoidal waveform and improves the behavior of the inverter and simplifies the standalone solar system structure. Using this proposed method, the inverter fundamental frequency can be also changed by changing the clock pulse generator's frequency, the calculation of switching angle is simple and less time consuming. The digital logic algorithm can be implemented to different topology of multilevel inverter and n-level of inverter can be designed easily. The future scope of this paper is to incorporate the synchronous sequential circuit based multilevel inverter into a single chip using VLSI technology.

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