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Design and Implementation of 4 Bit Static RAM through Low-Power Pulse-Triggered Flip-Flop

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Abstract

In this paper a low-power pulse-triggered structure and a modified true single latch structure based on a signal feed-through scheme is designed in TSMC CMOS 180 nm technology. The Pulse triggered flip-flop (P-FF) solves the problem of long discharging path and achieves better speed and power performance. The pre and post lay-out simulations has been done using Cadence tool, the performance analysis on power-delay-product metrics are obtained through simulation and finally a 4-bit RAM is designed by using P-FF and then the implementation has been done on SOC 11.10 technology.

Keywords: *S-RAM, Signal feed-through, SoC Technology*

1. Introduction

Low power consumption in very-high density VLSI chips have resulted to speedy and innovative developments. Flip-flops (FFs) are the fundamental storage element in every digital design. It is approximated that the power consumption of the clock distribution network of the clock system, is as high as 50% of the total system power. FFs thus contribute an important portion of the chip region and power consumption to the total system design [2, 3]. Pulse-triggered FF (P-FF), because of its single-latch structure, is more accepted than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. In addition to the speed improvement, its circuit simplicity reduces the power consumption of the clock tree structure. A P-FF generally consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are narrow enough, then the latch acts like an edge-triggered FF. While only one latch in the conventional master–slave arrangement is required, a P-FF is simpler in circuit complexity. This leads to a good toggle rate for high-speed operations [4–5]. P-FFs besides permit time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Regardless of these advantages, pulse generation circuitry requires delicate pulse width control to manage with feasible variations in process technology and signal distribution system. In [6], a statistical design structure is developed to obtain these factors into account balanced performance among power, delay, and area must be achieved, design space exploration is also a broadly used technique [7–8]. In this paper, we present a low-power P-FF design based on a signal feed-through scheme. Observing the delay incongruity in latching data "1" and "0," the longer delay is shortened by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by placing a simple pass transistor for extra signal driving. When pulse generation circuitry is combined with this, it forms a new P-FF design with improved speed and power-delay-product (PDP) performances.

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2. P-FF Design based on Signal Feed through Scheme

The proposed design employs a static latch structure and a conditional discharge method to keep away from surplus switching at an internal node connection. On the other hand, the differences which lead to an exclusive TSPC latch structure and make the proposed design separate from the earlier one. Firstly, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first phase of the TSPC latch, which gives growth to a pseudo-nMOS logic procedure design, and the charge keeper circuit for the internal node *X*. In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X* [10, 11]. A pass transistor MNX forced by the pulse clock is included so that input data can compel node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this spare passage facilitates auxiliary signal driving from the input source to node Q.

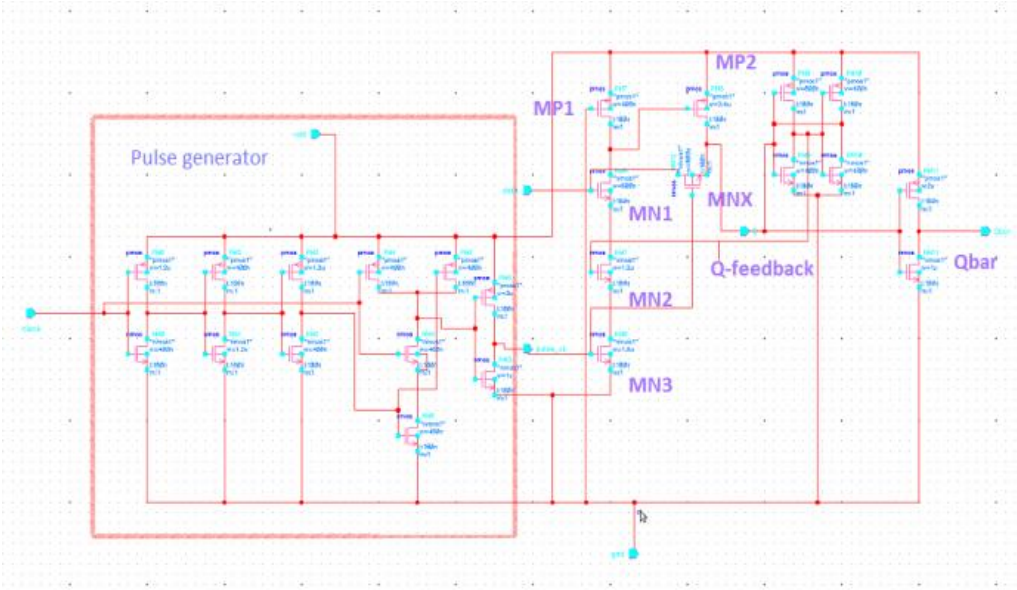

Figure 1. Schematic Diagram of P-FF Design

The node level can thus be rapidly pulled up to cut down the data transition delay. Third, the pull-down network of the second stage inverter is absolutely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The responsibility played by MNx is thus twofold, *i.e.,* on condition that extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" transitions of data. Compared with the latch structure that used in SCDFF design[9], the circuit saving of the power in the proposed design which includes a charge keeper (two inverters) and a pull-down network (two nMOS transistors), and a control inverter. The only additional component placed is an nMOS pass transistor to maintain signal feed through. This design really improves the "0" to "1" delay and which reduces the inequality stuck between the rise time and the fall time delays. If no data transition occurs when a clock pulse arrives *i.e.*, the node Q and input data are at the same level, on current passes all the way through the pass transistor MNx, which keeps the input stage The standard FF operation of the projected design are explained as follows. When a clock pulse turn up if no data transition take place, *i.e.*, the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. Simultaneously, the output feedback Q_fdbk and the input data assume opposite signal levels and the pull-down path of node X is off. Thus, no signal switching occurs in any

internal nodes. Conversely, node X is discharged to turn on transistor MP2 if a “0” to “1” data transition is occurred, which then pulls node Q high. The discharging path conducts only for a pulse duration, this is the worst case timing of the FF operation. However, a boost can be obtained with the signal feed-through scheme from the input source via the pass transistor MNx and the delay can be significantly shortened. Even though this seems to burden the input source with direct charging or discharging responsibility, which is a general pitfall of all pass transistor logic, the situation is dissimilar in this case as MNx conducts only for a very short period. When a “1” to “0” data transition occurs then transistor MNx is turned on by the clock pulse and node Q is discharged by the input stage through this route. In contrast to the case of “0” to “1” data transition, the sole discharging responsibility is beard by the input source. The loading effect to the input source is not significant because the MNx is turned on for just a short time slot. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size regulation to improve the speed.

3. Design of 4 Bit Static-RAM using P-FF

A 4 bit Static-RAM is designed using the P-FF structure. Memory is used to store the binary data, the memory is denoted as m x n, Where ‘m’ and ‘n’ refers to the amount of words and number of bits per word. An array of memory with size 4 X 4, refers that the system has 4 rows and 4 columns of memory. Using decoder memories can be repeatedly accessed. Decoder is used to pick out the actual address of the location within the memory. Then if a write pin (‘W’) is selected then data is allowed be written or if read pin is selected (‘R’) then data is read from the memory. Finally the OR circuit’s role is to show the word that is read out. Row of the memory is selected through the selection lines S1 and S2. Data0-Data3 are four data lines and ‘W’/’R’ (write/read) line is employed for choosing the write or read operation.

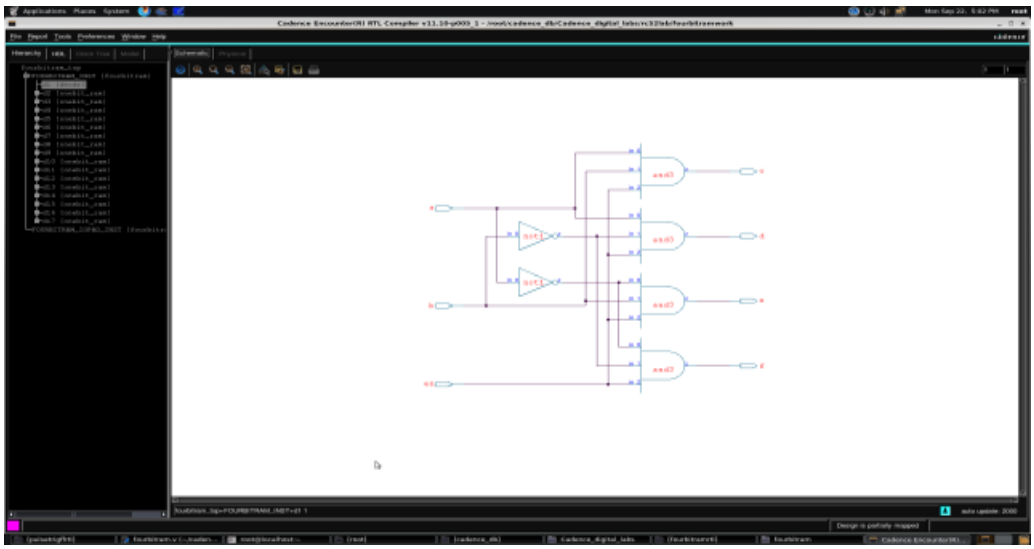

Figure 2. Decoder Circuit in Cadence Digital

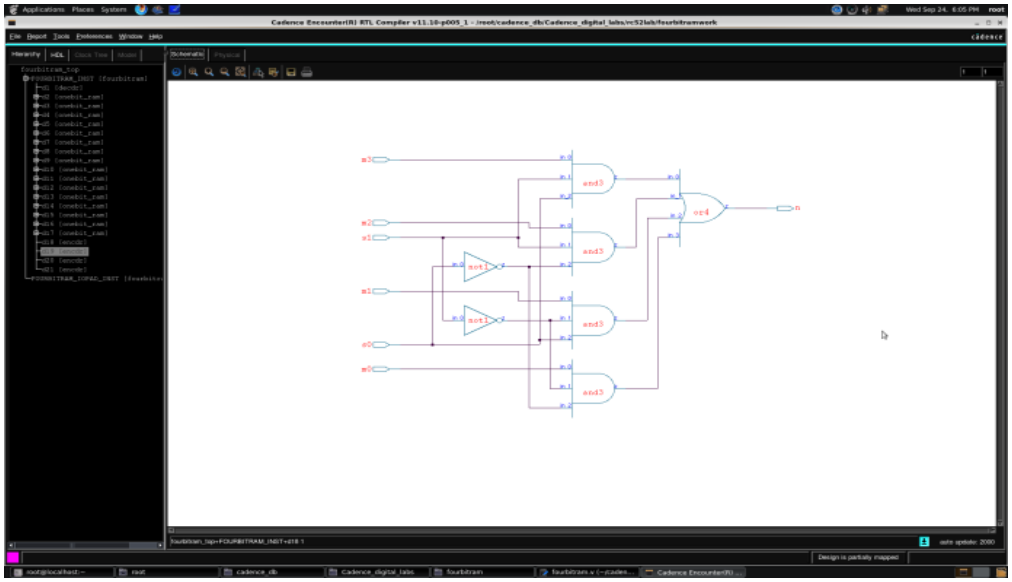

Figure 3. OR circuit in Cadence Digital

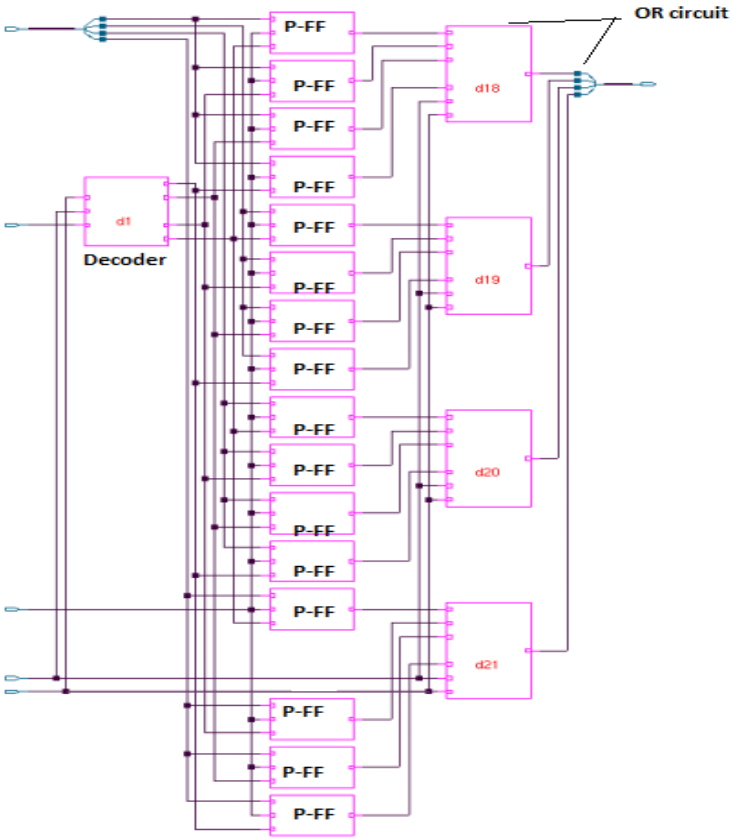

Figure 4. Elaboration of 4 Bit Static-RAM in Cadence Digital Window

4. Implementation of 4 Bit Static-RAM using P-FF on SoC (System on Chip)

A SoC is a system on an IC that integrates software and hardware Intellectual Property (IP) using more than one design methodology for the purpose of defining the functionality

and behavior of the proposed system. The designed system is application specific. The 4 bit S-RAM that is designed using P-FF structure is finally implemented in SoC 11.10 technology.

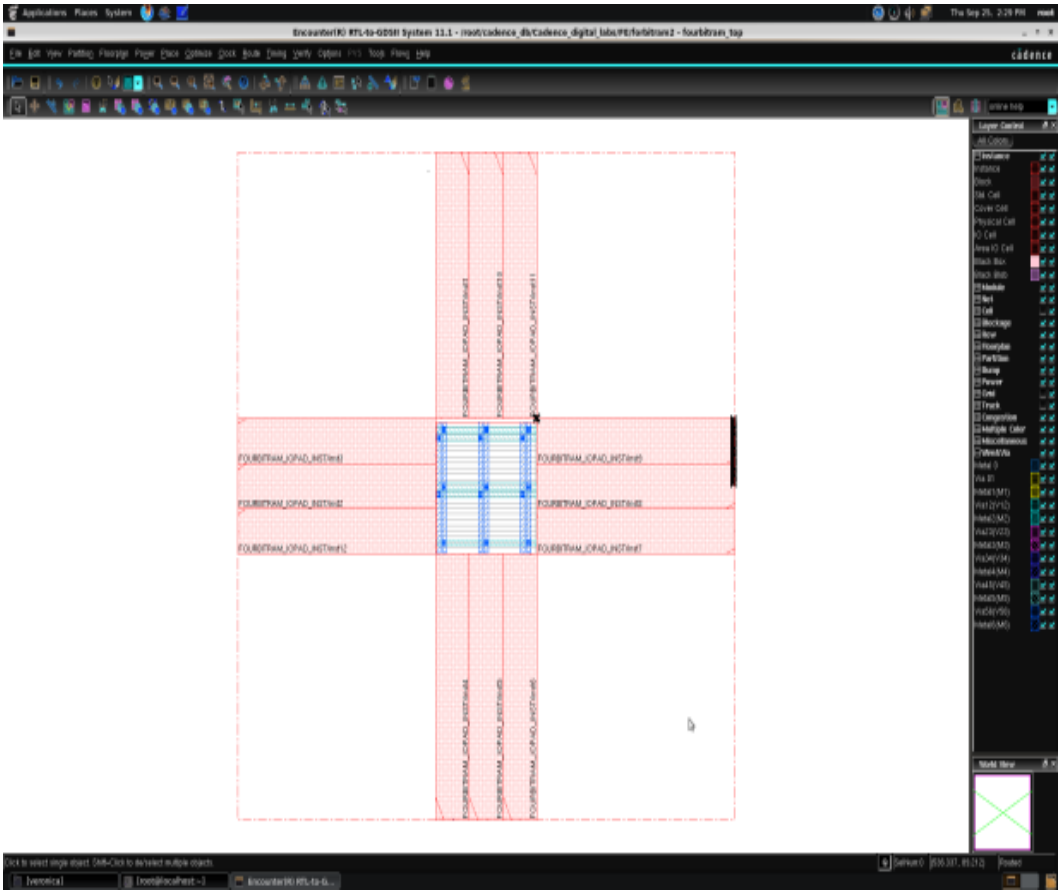

Figure 5. Implementation of 4 Bit S-RAM on SoC 11.10 Technology

5. Simulation Results

The performance of the proposed P-FF design is evaluated through the layout simulations. The technology used is 180nm CMOS for simulation. The pre-layout and post-layout simulations of P-FF and the waveforms are shown in Figure 6 and Figure 9 respectively. The operating condition used in simulations is 5MHz/5V The D-Q delay of the pre-layout simulation is 21.28 nsec and is shown in Figure 7. The D-Q delay after the post-layout simulation is 124.6 psec and the simulation waveform is shown in Figure 10. The layout of the P-FF design is shown in Figure 8. The leakage and dynamic power is obtained and is shown in Figure 11.

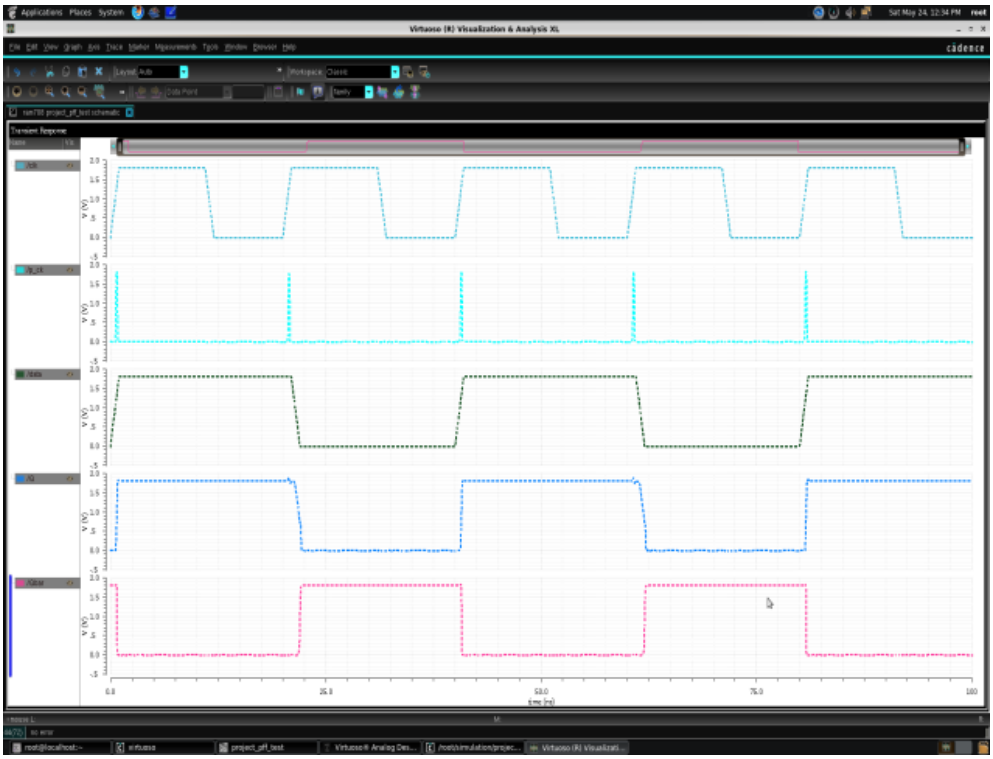

Figure 6. P-FF waveform of pre-layout simulation

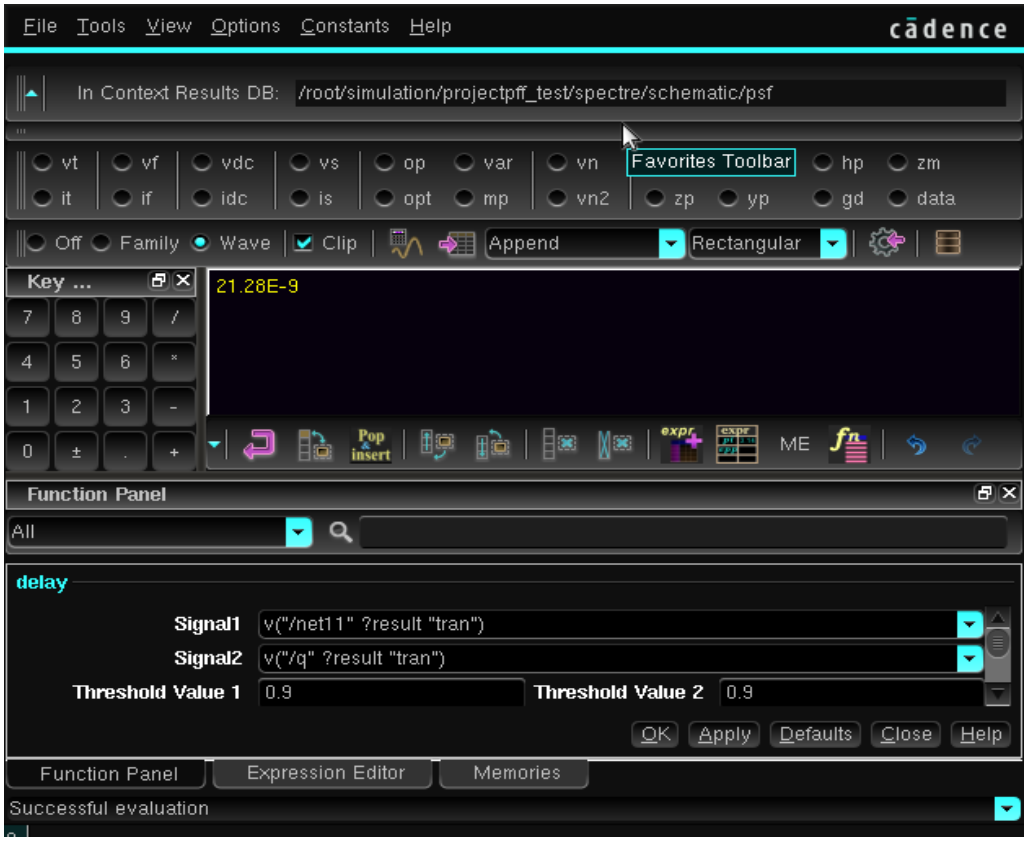

Figure 7. D-Q Delay of the Pre-layout Simulation

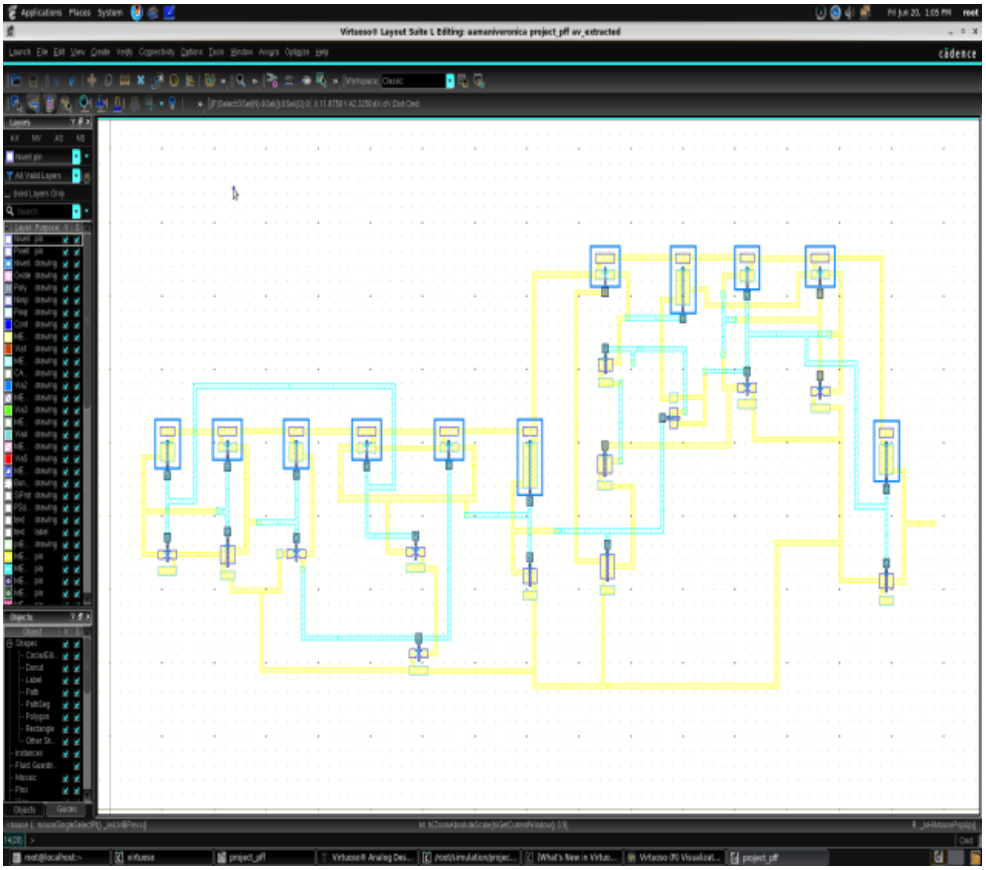

Figure 8. Layout of P-FF Design

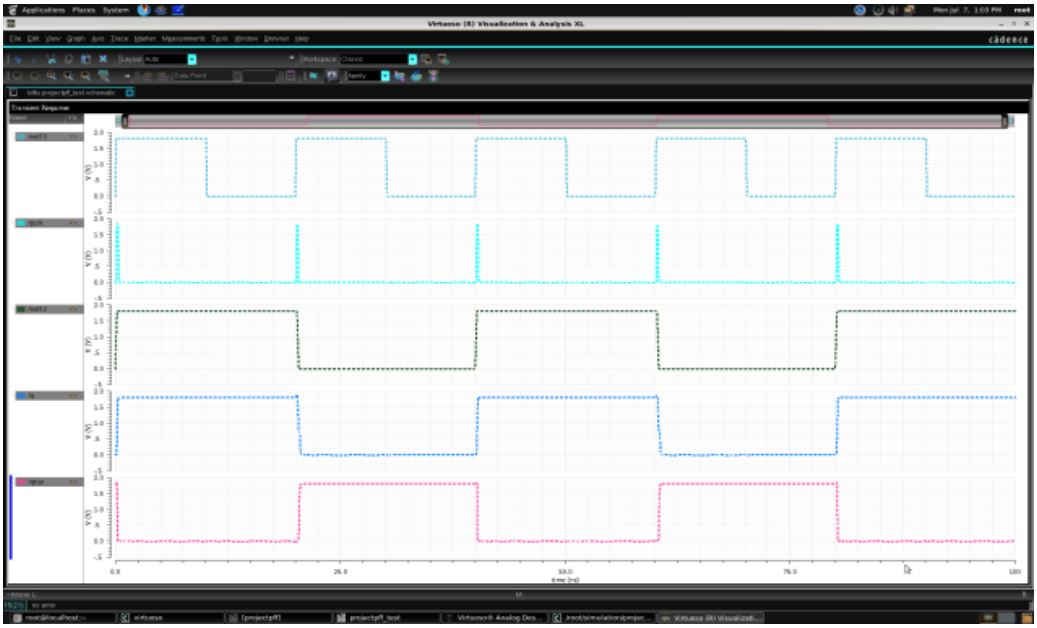

Figure 9. P-FF Waveform of Post Layout Simulation

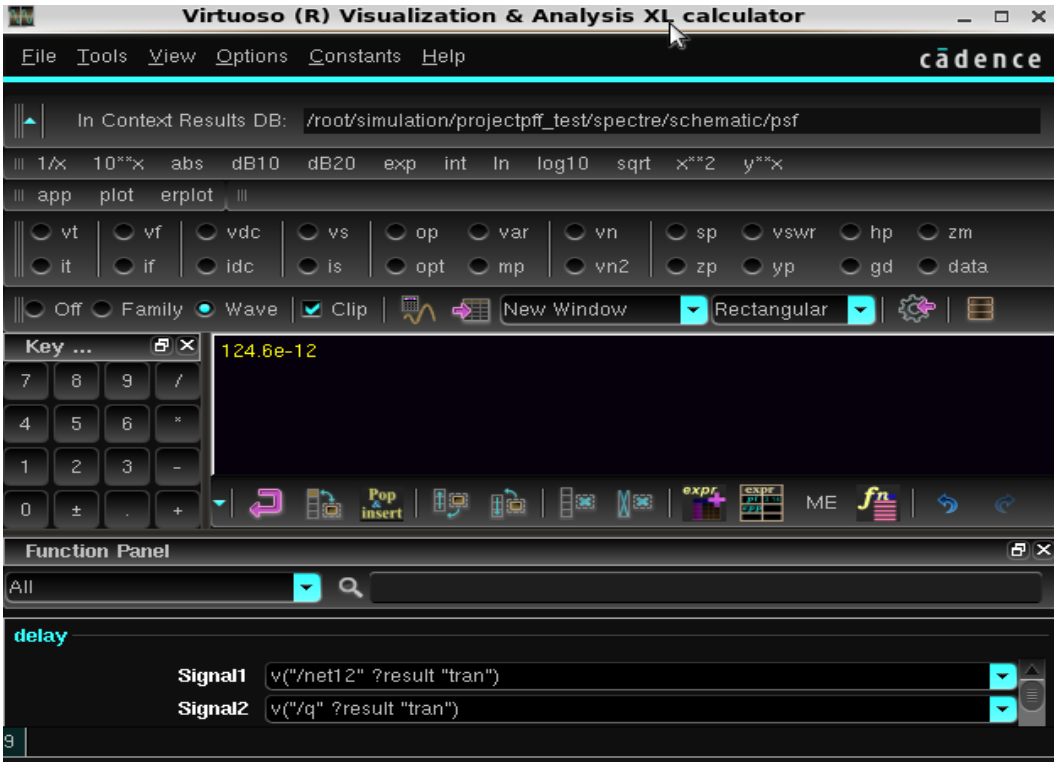

Figure 10. D-Q Delay after the Post Layout Simulation

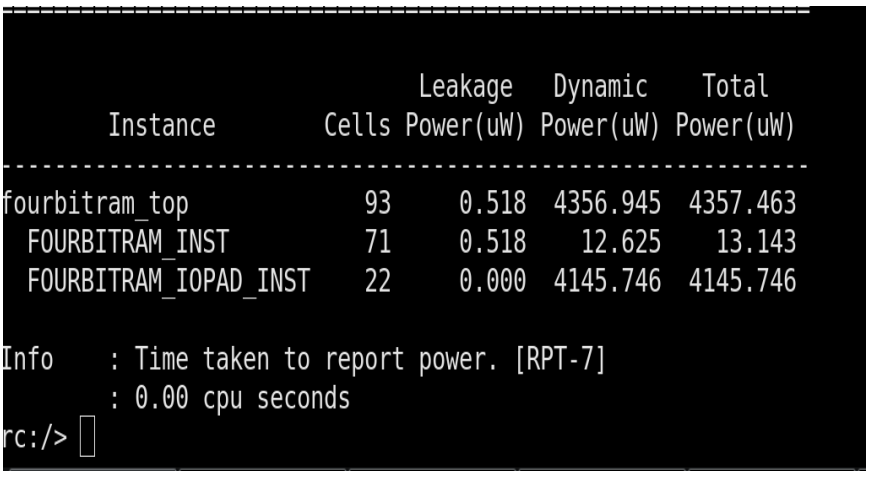

Figure 11. Power Report of the 4bit Static- RAM after Low Power Synthesis

6. Conclusion

In this paper, a 4-bit Static-RAM is designed based on a P-FF design using modified TSPC latch structure employing a pseudo-nMOS logic and a pass transistor. Extra driving is achieved through signal feed through and is provided from input source to the internal node of the latch, to condense the transition time and improve both speed and power performance. All the simulations are conducted on Cadence platform. The design was achieved and SoC implementation is also done and the results did support the claims of the proposed design in various performance aspects.

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