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Modeling and Simulation with Spice of the New Power SiC JFET

Messaadi Lotfi[1] and Dibi Zohir[1]

[1]*Department of Electronics, Advanced Electronic Laboratory (LEA), Batna University, Avenue Mohamed El-hadi Boukhlouf, 05000,Batna, Algeria*
lotfi.messaadi@gmail.com,zohirdibi@yahoo.fr

Abstract

This paper present the development of a SPICE SiC JFET model and its corresponding characterization process. The device under study is a 1.3 kV, 15 A SiC JFET prototype manufactured by SiCED, packaged in a TO-220 case. The static and dynamic behavior of the SiC power JFET is simulated and compared to the measured data to show the accuracy of the Spice model. The switching characteristics have been tested on a double pulse tester under multiple conditions. A similar double pulse test circuit with parasitics in consideration has been simulated in Spice with the MOSFET model, which gave good results.

Keywords: *SiC JFET, Power Devices, Modeling, Simulation, High voltage, Spice, Matlab*

1. Introduction

There has been a remarkable progress in the development of SiC power devices the last years. Currents in excess of 100 A and blocking voltages in excess of 19000 V has been demonstrated. Several discrete SiC transistors are now available from different manufacturers. The first available SiC transistor was the normally-on JFET, which was followed by the normally-off JFET. The development and application of silicon carbide (SiC) JFETs are still very hot topics today due to its reliability and more mature manufacturing techniques compared to other categories of SiC devices (e.g. SiC MOSFET). At the time of this work, the only available 1.3 kV level SiC active switches that have been demonstrated to operate reliably at temperatures beyond 150 ℃ are SiC JFETs, which are also expected to be the first commercialized SiC active switches, following the SiC Schottky diodes. So far there have been many efforts on the characterization and modeling of SiC JFETs.

This paper presents the characterization and Modeling of 1.3 kV, 15 A SiC JFET, the static characteristics, such as the forward and transfer curves, is extracted and calculated. The comparison of static characteristic between Spice model and measured data show good agreement with each other. The switching characteristics have been tested on a double pulse tester under multiple conditions. The junction capacitances of the SiC MOSFET and the SiC diode have been extracted using an impedance analyzer. A similar double pulse test circuit is simulated in Spice, which gave satisfactory results. With both static and switching comparison, the PSpice model has been proved to be valid for predicting the SiC JFET performance in power converters.

2. SiC JFET Structure

The SPICE JFET model is originally developed for lateral structure device, therefore it is inadequate to model the vertical structure SiC JFET. Figure 1 exhibits a typical cross-sectional structure of SiC JFET. As seen, instead of all three terminals being on the same side, the drain terminal of the device is on the bottom in vertical structure while the source and gate sit on the top. The P+ layer buried under the source terminal

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and the N layers under that constitute a PN junction between the drain and source terminals. This equivalently forms a body diode as well as a drain-source junction capacitance C_{DS} to the JFET, which is not modeled for lateral structure in the SPICE model. This body diode is included in the proposed model by adding an anti paralleled power diode model to the SPICE model, and the drain-source capacitance is then interpreted as the diode junction capacitance, as seen in Figure 1.

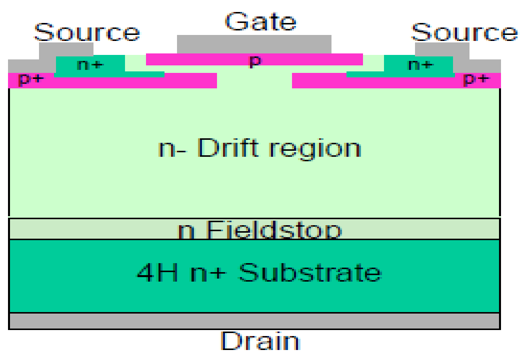
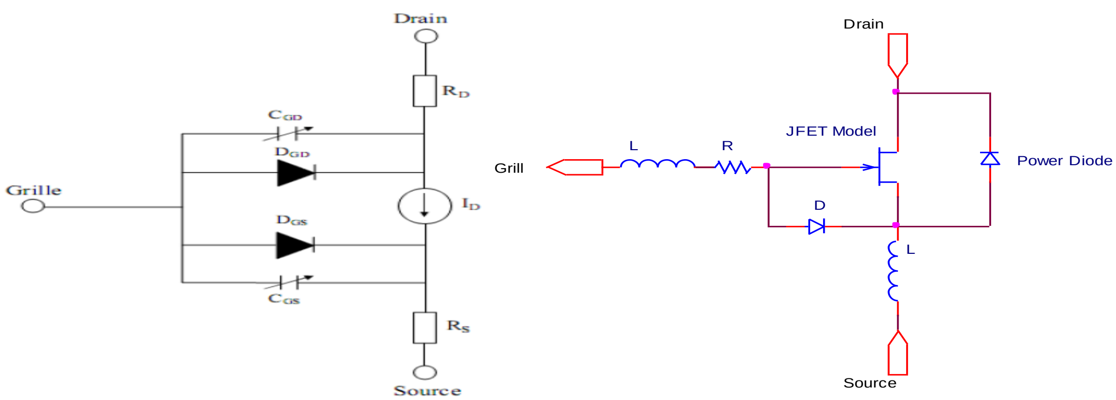


Figure 1. Typical Cross-Sectional Structure of SiC JFET [1]

Besides the body diode, an extra SPICE diode model is also added across the gate source terminals in order to model the gate breakdown characteristics of the device. This is necessary for the case when the gate of the SiC JFET is intentionally driven in breakdown mode. Also seen in Figure 2-a is a resistor connected in series with the gate terminal representing the internal gate resistance of the device, while the package stray inductances are lumped into two series inductances. All these components together describe the SiC JFET static and switching behavior under normal operating conditions.

3. SPICE SiC JFET Model

The proposed SiC JFET model is illustrated in Figure 2-b. The core of this model is a SPICE JFET model which describes the basic JFET static (current-voltage, I-V) and dynamic (capacitance-voltage, C-V) characteristics, as seen in Figure 2.



(a) (b)

Figure 2. Schematic representation of the SiC JFET

This level-1 SPICE model contains less than 20 parameters, which can be easily extracted from conventional characterization data, such as the output and transfer characteristics.

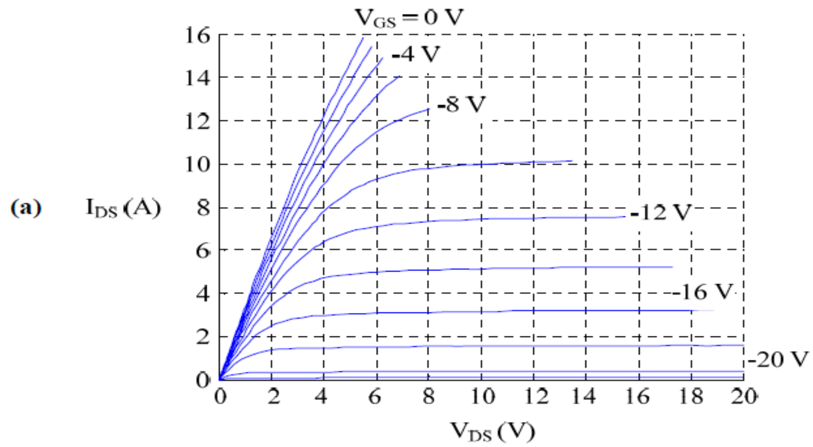


Figure 3. Schematic Representation of the SiC JFET

In SPICE, the JFET model uses the following equations to describe the output characteristics:

$$I_D = \begin{cases} 0 & V_{GS}-V_{T0} < 0 \quad \text{(pinch off)} \\ \beta(V_{GS}-V_{T0})(1+\lambda V_{DS});\ 0 < V_{GS}-V_{T0} < V_{DS} & \text{(Saturation)} \\ \beta V_{DS}[2(V_{GS}-V_{T0})-V_{DS})](1+\lambda V_{DS}); 0 < V_{DS} < V_{GS}-V_{T0} & \text{(linear)} \end{cases}$$

Where model parameter β is the transconductance, λ is the channel-length modulation parameter, and V_{T0} is the threshold voltage. A curve-fitting method is carried out in Matlab to extract these parameters. Basically VT0 can be extracted from the interception point of VGS for the square root value of $I_{DS}V_{GS}$ graph. The square root of β can be approximated by the slope of the square root value of the same graph. The optimized V_{T0}, β and λ can be determined by running a least-mean-square (LMS) Matlab program to curve fit the measurement data. Considering the nominal current rating of the DUT, the curve fitting is done within a current range of 0 to 3 A. The result is shown in Figure 2 as the set of red dashed curves, where as seen a good agreement is achieved between the measured and simulated curves.

4. Characterizations of SiC JFET and Model Parameter Extractions

4.1. Static I-V Characteristics

Figure 4 shows the output and transfer characteristics of the SiC JFET, from which it can be told that device under test (DUT) has an on-state resistance $R_{DS(ON)}$ of around 0.3 Ω at V_{GS} = 0 V and I_{DS} = 5 A, and the device is pinched off at $V_{GS} \approx$ -25 V.

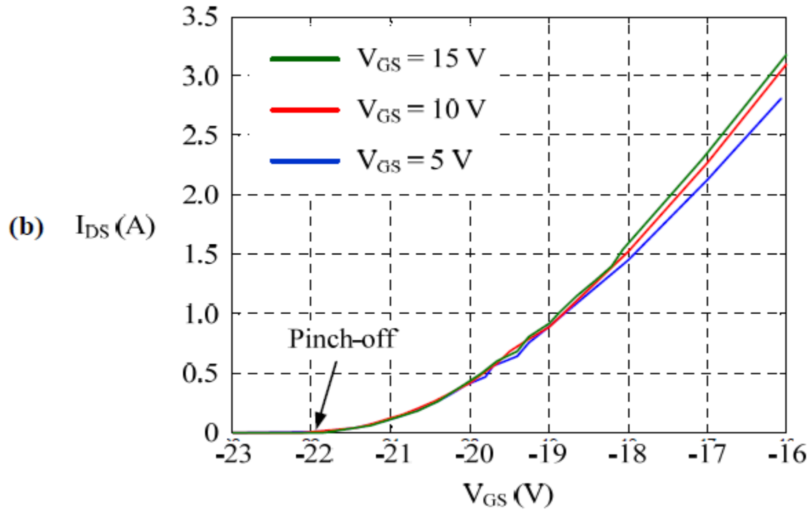


Figure 4. Transfer (a) and Output (b) Characteristic of a SiC JFET

4.2. Body Diode Characteristics

Unlike conventional PiN or Schottky diodes, the I-V characteristic of the SiC JFET body diode is gate-voltage dependent [6]. Figure 5 shows an example of this characteristic. For this SiC JFET (not the same DUT as used above), the channel is completely pinched off below -19 V, whereas the I-V curve is seen to shift to the right with decreasing gate source voltage, *i.e.*, the turn-on voltage becomes bigger. The slopes of these curves remain constant, which means there is no change in the diode series resistance.

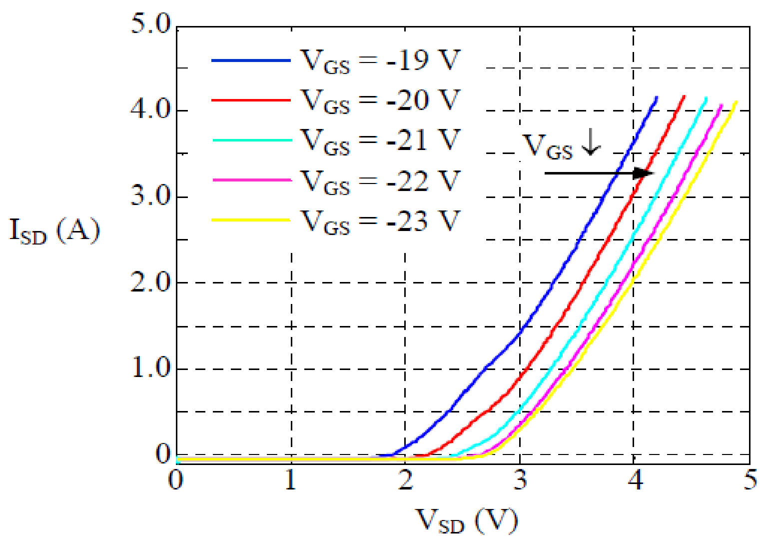


Figure 5. Gate-voltage-dependent body diode I-V curves

This gate-voltage dependence cannot be modeled by any existing model. In this work, the body diode is still treated as being independent of the gate voltage, and a specific I-V curve is picked for modeling according to the final gate voltage used in the circuit. The model is built with the Power Diode Tool in Synopsys Saber, where the device characteristics (*i.e.*, I_{SD}-V_{SD} and C_{DS}-V_{DS} curves) are tuned visually to fit the characterization data. The curve-fitting results are shown in Figure 5, where a good agreement can be seen between the simulation and the measurement. The resultant power diode model is then connected in anti-parallel with the SPICE JFET model as shown in Figure 1.

5. Model Verifications

SiC power JFET were tested in a double pulse tester with the schematic of the test circuit shown in Figure 6. The freewheeling diode was a SiC Schottky diode. An IXDD 414 chip was used as the gate driver. The gate resistors Rg1 was 15 Ω, and the gate capacitor C1 was 30 nF. The combination of Rg2 and C was used to reduce transient time and increase switching speed. The gate voltage swing was 0 V to 20 V.

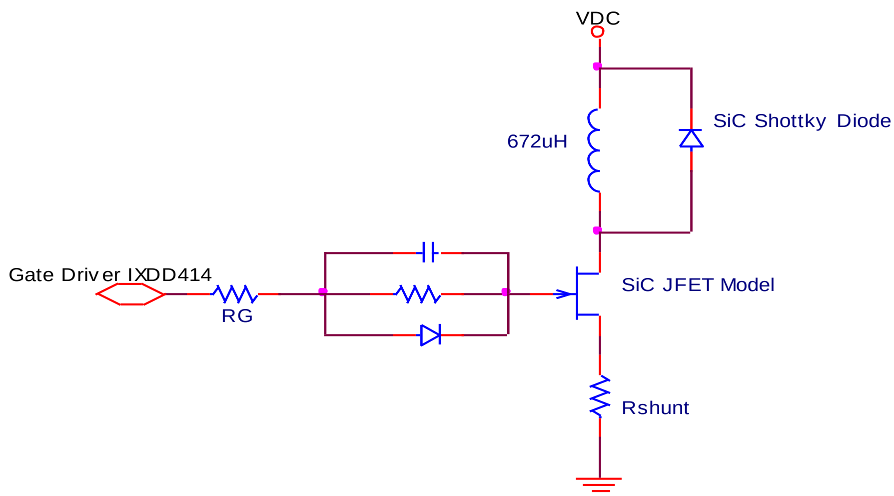


Figure 6. Schematic of Double Pulse Tester in the Spice

The SiC JFET switching waveforms are obtained using the double-pulse. A 0 Ω external gate resistance is used to switch the JFET as fast as possible. A comparison of experimental switching waveforms and the simulated results is displayed in Figure 7.

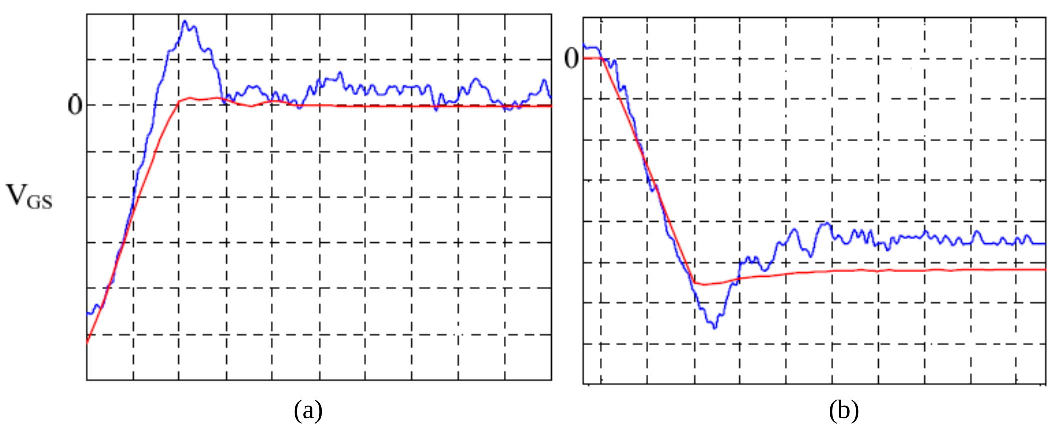
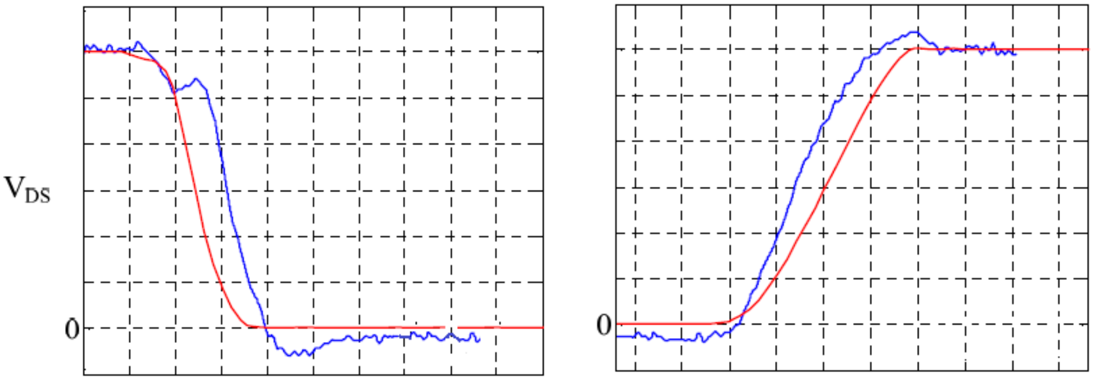
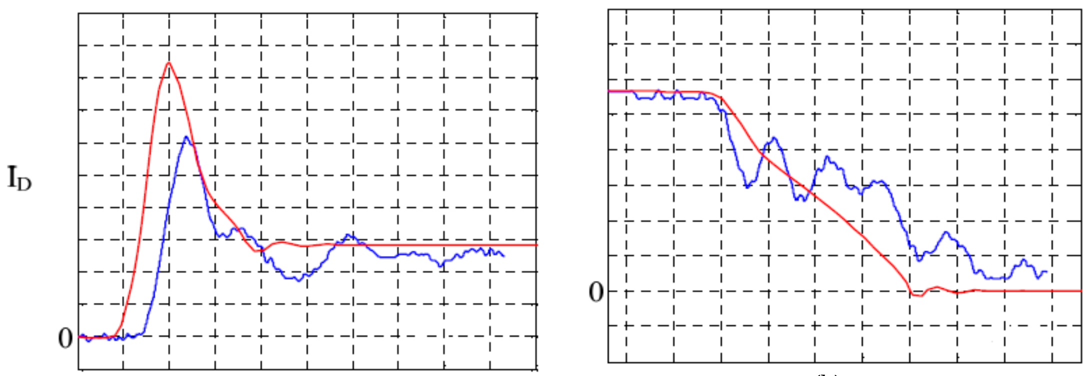


Figure 7. Simulated Turn on Waveforms Experiment (blue) and Simulation (Red): (a) turn on (b) turn off (5 V/div, Time: 5 ns/div)



(a) (b)

Figure 8. Simulated Turn on Waveforms Experiment (blue) and Simulation (Red): (a) turn on (b) turn off (100 V/div, Time: 5 ns/div)



(a) (b)

Figure 9. Simulated Turn On Waveforms Experiment (blue) and Simulation (Red): (a) turn on (b) turn off (5 V/div, Time: 5 ns/div)

The waveforms are obtained under 500 V and 4.5 A load conditions. To do the comparison the experimental and simulated VGS waveforms are aligned in time. As seen, for the turn-on transients the JFET drain-source voltage VDS and drain current ID have around 4 ns advance in time compared to the experiments, which means the model predicts less turn-on delay than the real condition. Nonetheless this 4 ns is small enough and tolerable in this work.

The slew rates of V_{DS} and I_D are predicted quite well by the model during both turn-on and turn-off processes, indicating that the model is good enough overall in predicting the correct waveforms and switching loss of the SiC JFET. Also note that the additional SPICE diode model is working well because during turn-off V_{GS} ends at around -28 V, the gate breakdown voltage, instead of -30 V, the gate drive turn-off voltage. The only discrepancy is the turn-on current spike which in the simulation is about 4 A higher than the experiment. This current spike is mainly related to the characteristics of the freewheeling diode, and in this work a different diode model is used in the simulation. If the Infineon diode model is available, the simulation would match the experiment even better. Another fact worth noting is the fast switching speed of this SiC JFET. As seen from Figures 8, 9 and 10, the DUT switches 600 V and 5.5 A within 20 to 30 ns, achieving a maximum dv/dt rate of around 60 kV/μs and a maximum di/dt rate of 3 kA/μs, much faster than the conventional silicon bipolar devices (*e.g.*, IGBT) of similar nominal voltage and current ratings. It is thus foreseeable that with the use of SiC devices, the high-frequency, high-temperature and high-power-density applications become achievable more easily.

6. Conclusions

In this paper we have proposed a SPICE SiC JFET model which is suitable for system-level simulation, and has presented the modeling process of SiC JFET prototype from SiCED. Device characterizations have been conducted on this JFET to extract the model parameters. Issues during the characterization process have been explained and solutions have been provided. By comparing the simulation with the experiment, the effectiveness of the device model has also been verified.

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