International Journal of u- and e- Service, Science and Technology
Vol.7, No.3 (2014), pp.85-102
http://dx.doi.org/10.14257/ijunesst.2014.7.3.09

Behavioral non-ideal Model of 8-bit Current-Mode Successive Approximation Registers ADC by using Simulink

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Abstract

In this paper a new non-ideal model of 8-bit Current Mode Successive Approximation Analog-Digital Converter (CM-SAR-ADC) has been proposed, the main blocks of CM SAR ADC are a current sample and hold, a current comparator, SAR logic register and current steering digital to analogue converter (DAC). The model is implemented in Matlab Simulink environment with non ideals factors such as switching noise, clock feed through, charge injection, flicker noise, clock jitter, settling error, and the effect of MOS transistor mismatch in the current sample and hold(S/H) and in the current steering DAC models, the delay time and the current offset are introduced as non-ideal sources to the current comparator model. The comparisons of the simulation results using 8-bits CM SAR ADC with ideal and non-ideal models confirmed the effects of the non ideality sources on the parameters of the ADC.

Keywords: *analog to digital converter, digital to analogue converter, CMOS, current mode, modeling and simulation, SAR ADC, steering DAC, thermometer encoder*

1. Introduction

Due to the huge increase of the architecture and the complexity of mixed signal circuits, the use of behavioral model is necessary to design and simulate the performance of those circuits, the complexity of mixed signal circuits require to using faster and more complex mixed-signal testers, the behavioral model based on MATLAB and SIMULINK environment are becoming good method to design and simulate the performance of the complex circuits such as the data converter, Modeling and simulation have increased the designer efficiency and ability to develop increasingly complex and useful electronic circuits, particularly at the integrated circuit (IC) level. Each type of circuit considered has its own particular requirements, in terms of design performance (specifications), design methodologies required to realize the design, modeling and simulation toolsets utilized, designer experience and skills set.

Research in analog integrated is being oriented in the direction of low-voltage (LV) and low-power (LP) design. This is especially the case for portable systems where a low supply voltage generated by a single-cell battery is used. Current mode circuit technique offers a number of advantages [1]. The design of high-performance ADCs presents difficult challenges as applications call for higher speed and resolutions. For this purpose the current-mode technique brought many solutions for compatibility with low power supply, high speed, small chip area, and less dynamic range to achieve higher operating speeds. Selecting architecture is important since each analog-to-digital converter (ADC) architecture has specific advantages with respect to sampling rate, noise, resolution, dynamic range, power consumption, and implementation area [2].

The SAR ADCs have received renewed attention due to their excellent power efficiency and low-voltage potential compared to pipelined and cyclic ADCs [3]. Since it does not require operational amplifiers, the voltage mode SAR ADC uses only a

ISSN: 2005-4246 IJUNESST

comparator and capacitors array in DAC circuit part. This raises two main issues; the first one is the need for large chip area and the second issue is the long settling time [4]. In the other part the Power consumption in the voltage SAR ADC is mainly from the DAC [5], for this reason, the CM SAR ADC is designed with current source array serving in the DAC for decreasing the effect of long settling time and the power consumption. Moreover, No capacitors are used in the DAC and thus can be made very small compared to voltage SAR ADC [6].

In this paper we are developed a new version of non-ideal model of 8 bit CM SAR ADC by using MATLAB and SIMULINK environment, The model's target is to predict the static and dynamic performance of this type of circuit and check them for the effect of non-ideal sources on the parameters of the CM SAR ADC. The main non-ideal factors introduced in the model are clock feed through, charge injection, thermal noise, flicker noise, clock jitter and settling time in the CM sample and hold, delay time, and the current offset error in current mode comparator, the problem of matching of current sources and non-idealities of switches in the current steering DAC. The main advantage of the behavior of this modeling approach is that it offers a low computing time and it is characterized by a less complexity of design in comparison to the level transistor method. These models are implemented using elementary SIMULINK of library blocks taking into consideration that the computational cost should be as minimum as possible.

This paper is organized as the flowing; after the introduction, the ADC architecture is presented in the second section and the behavioral model of SAR ADC in the third section. The different parts of the model with non ideals factors are reported in the fourth section of the paper. Finally, Simulation results with the static and dynamic performance, the comparison of simulation results of the models with others results references and conclusion can be found in the fifth and the sixth sections respectively.

2. The ADC Architecture

The block diagram of current mode SAR ADC architecture is shown in Figure 1, this architecture which consists of a front end current S/H, current comparator, current steering DAC and SAR logic. SAR logic is basically a shift register combined with decision logic and decision register, the operation principle of this current mode SAR ADC is similar to the conventional voltage mode SAR ADC [4]. However, current-mode converters are now demonstrating excellent characteristics and in particular, high resources efficiency (power and area) [7]. The ADC works by using a DAC and comparator to perform a binary search to find the input signal. A sample and hold circuit (S&H) is used to sample the analog input and hold the sampled value whilst the binary search is performed. The binary search starts with the Most Significant Bit (MSB) and works towards the Least Significant Bit (LSB). For a 8-bit output resolution [8], and in contrast to voltage mode, the current mode ADC uses only CMOS transistor in the DAC as current sources and logical operation. This has the advantage to reduce the area requirements, reduce power consumption and achieve high speed operation [7].

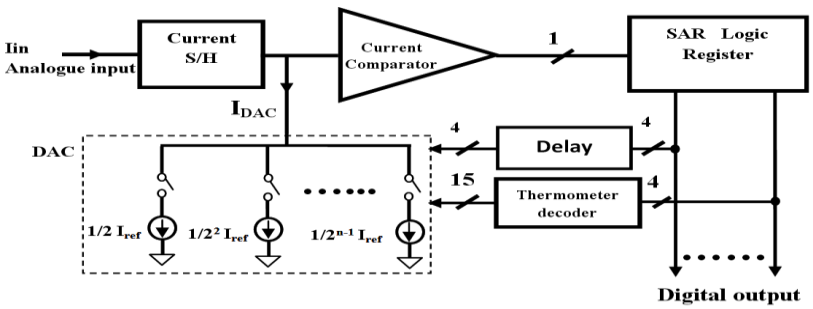

Figure 1. Current Mode SAR ADC Architecture

3. Behavioral Model of CM SAR ADC

Simulink model of CM SAR ADC is shown in Figure 2. It consists of five major blocks; a current S/H, a current comparator, SAR logic register, a thermometer decoder, and 8-bit current steering DAC with 4 MSB and 4 LSB, The current steering DAC is the critical building block of the CM SAR ADC. The operation principle of CM SAR ADC is similar to the conventional voltage mode SAR ADC [4]. However, current-mode converters are now demonstrating excellent characteristics and in particular, high resources efficiency (power and area) [9]. The ADC works by using a DAC and comparator to perform a binary search to find the input signal. A sample and hold circuit (S&H) is used to sample the analog input and hold the sampled value whilst the binary search is performed. The binary search starts with the Most Significant Bit (MSB) and works towards the Least Significant Bit (LSB). For a 8-bit output resolution [10], and in contrast to voltage mode, the CM SAR ADC uses only CMOS transistor in the DAC as current sources and logical operation. This has the advantage to reduce the area requirements, reduce power consumption and achieve high speed operation [9].

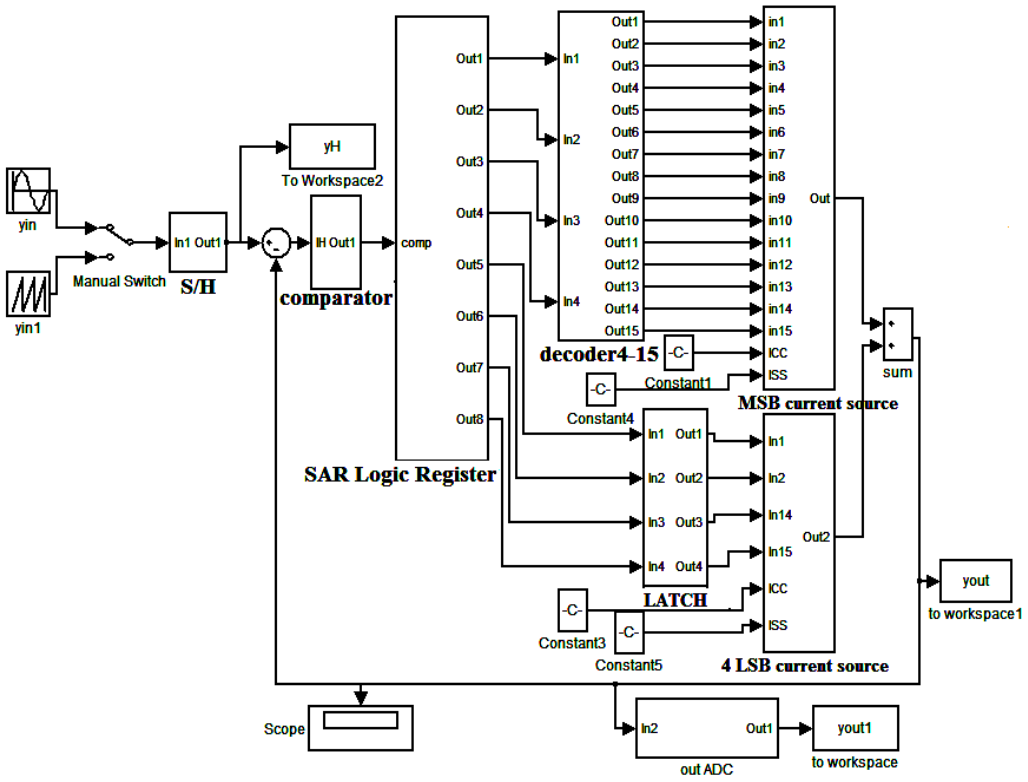

Figure 2. Simulink Model of Current Mode SAR ADC

4. Building Blocks and Non Idealities Factors in CM SAR ADC

The non-ideal effects will hurt the overall ADC performance, in this section the most important affects in the CM SAR ADC are discussed, the main non-ideals errors analysis in this section, current offset, clock feed through, charge injection, thermal noise, flicker noise, clock jitter, and mismatch errors in current S/H and in current steering DAC.

4.1. The non-idealities of Current Sample and Hold

The S/H circuit is an important block in the data converter systems. Recently, more focus is granted to current-mode S/H, due to their high speed and low voltage supply in

comparison with voltage mode circuits (switch capacitor) [11]. The current-mirror circuit is the basic component in the current-based sample-and-hold IC [12]. Figure 3 presents the basic schematic of the current S/H. The operation is controlled by the switch MS1; when it is closed, the gate node is connected to the input signal and the drain-source current Ids will be a function of the gate-source voltage. When the switch S1 however is open, the gate node remains isolated and hence, the charge stored on the gate oxide capacitance Cgs of the transistor M1 can hold the output current at the value of the time instant.

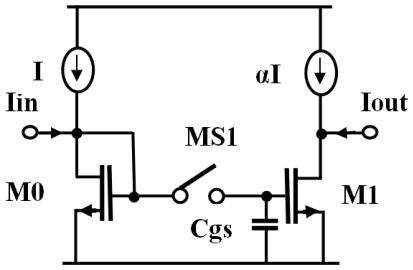

Figure 3. Basic Current Sample and Hold

In the CM SAR ADC the accuracy linearity and dynamic range will be dominated by the S/H circuit [10], A Sample and Hold (S/H) block is a critical part of an ADC [13] The S/H samples the analogue input signal and holds the value for certain time, the model ideal of the sample and hold is shown in Figure 4.

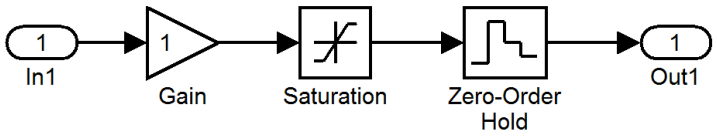

Figure 4. Sample and Hold Model

In the current mode circuits there are some technical limitations of non ideality factors; and thus significantly degrade performance of current S/H circuits in practical realizations, the S/H circuit suffers from various non-ideality sources; such as components mismatch and non ideality of the switches, the switches are a source of many errors such as charge injection, clock feed through, clock jitter, thermal noise, and flicker noise.

4.1.1. Charge Injection

In current mode S/H circuits, the charge injection and the Clock feed-through becomes one of the main performance limitations. When MOS is on, it carries certain amount of charge in its channel; the charge under the gate oxide resulting from the inverted channel is approximated by

$$Q_{ch} = C_{ox} * W * L * (V_{GS} - V_{TH}) \qquad (01)$$

When the device turns off, the charges accumulated in the channel re-injected into the circuit via the drain and source of the MOS transistor. This phenomenon is called charge injection, this charge leaves the channel through the source and drain terminals, the charge injected via the drain does not introduce error. In contrast, the charge injected on the other side (source), introducing an error voltage ΔV on the sampling capacitor as shown in Figure .5

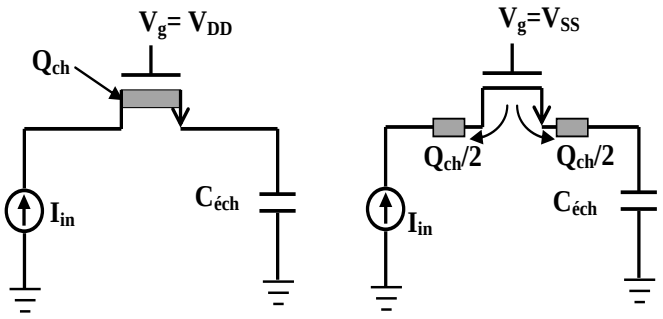

Figure 5. Charge in the NMOS Transistor Channel

The amplitude of charge injection of n-channel switch, for instance can be calculated as

$$\Delta V_{INJ} = \frac{Q_{ch}}{C} = \frac{C_{OX} * W * L * (V_{GS} - V_{TH})}{2 * C_{gs}} \qquad (02)$$

Figure 06 presents the charge injection simulator module achieved by a derivative block. The random variable generator block generates outputs in a form of series of pulsed signal. After passing through the derivative block, the zero-order block is used to specify the time constant of charging and gain factor is used to adjust the amount of the charge injected

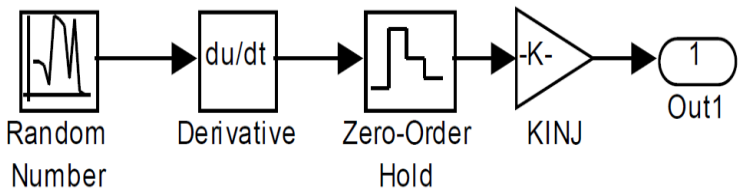

Figure 6. Charge Injection Model

4.1.2. Clock feed-through

Another source of error in MOS switches is clock feed through, a MOS switch couples the clock signal VCLK to the sampling capacitor through overlap capacitances (Covl) between the gate and source or drain terminals as shown in Figure 7 [14], this error appears as an offset if Qch is constant, the overlap capacitance is give by

$$C_{OVl} = C_{ox} * w_{eff} * L_d \qquad (03)$$

Where Cox is the thin-oxide capacitance per unit width, Ld is the lateral diffusion length, and. Weff is the effective channel width.

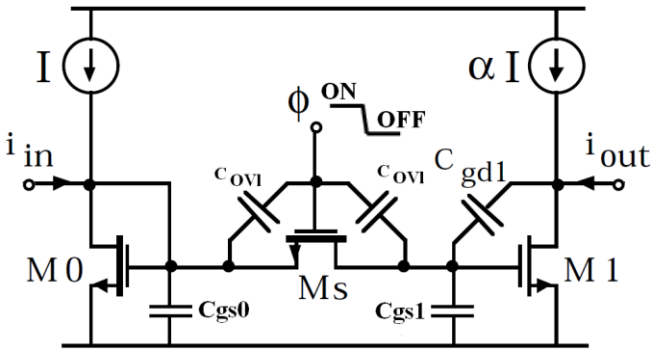

Figure 7. Clock Feed-Through in a Sampling Circuit

With the switching of the clock, the charges accumulated in the overlap capacitances are also, injected into the circuit, in the fast clock transition the error signal produced on the sampling capacitor is given by the following formula [14]

$$\mathrm{Eclk} = \frac{3}{2} \times \Delta\phi_{\mathrm{clk}} \times \frac{\mathrm{W_s}}{\mathrm{W_1 \times L_1}} \times (\frac{\eta}{2} \times \mathrm{L_{S1}} + \mathrm{L_D}) \qquad (04)$$

The $\Delta\phi_{\mathrm{clk}}$ is the amplitude of the control signal.

Where $\Delta\phi_{\mathrm{clk}} = \phi_{low} - \phi_{high}$, $\eta = \frac{\phi_{high} - \mathrm{v_{gs0}}}{\Delta\phi_{\mathrm{clk}}}$ and L_D is the lateral diffusion length.

The error Eclk is independent of the level of the input signal. It results in a constant offset it's added to the sampled signal.

4.1.3. Clock Jitter

Sampling clock jitter is another phenomenon that has attracted attention in the design of ADCs, Sampling of the analog input cannot occurs exactly at the desired time. This uncertainty Δt the sampling instant, commonly called jitter, this non-ideal factor produces a conversion error Δy proportional to the slope of the signal; The error result from clock jitter can be expressed as[15]

$$y(t + \Delta t) - y(t) = \Delta t * \frac{d}{dt} y(t) \qquad (05)$$

With sinusoidal input signal as shown in Figure 8, where A is the input signal amplitude, $\mathrm{f_{in}}$ is the input signal frequency and Δt is the time jitter error, the maximum amplitude error $\Delta \mathrm{y_{max}}$ of the jitter model can be expressed as

$$\Delta y(t)|_{\max} = \Delta t.A.\frac{d\,cos(2\pi\, f_{in} t)}{dt}\Big|_{\mathrm{t=0}} = A.\Delta t.2\pi\, f_{in} \qquad (06)$$

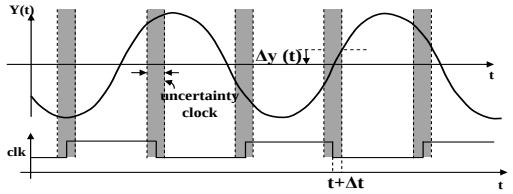

Figure 8. Clock Jitter Error Model

Figure 9 Show the behavioral model clock jitter effect [20]

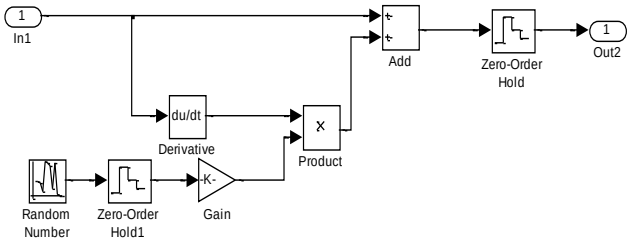

Figure 9. Clock Jitter Model

4.1.4. Flicker Noise

The flicker noise or 1/f noise phenomenon has been observed in almost all kinds of devices with resistive components, thus this kind of noise is very dominant in lower frequency, and it is negligible in higher frequencies. In a MOS transistor shows the highest 1/f noise due to its surface conduction mechanism, Other authors attribute this

noise to mobility fluctuations, this noise component typically increases with technology scaling [16], The PSD of the flicker noise current can be expressed as [17]

$$S_{fl}(f) = \frac{K_f * I_{DQ}}{C_{ox} * W * L} * \frac{1}{f} \qquad (07)$$

Where Kf is the flicker noise coefficient, Cox is the oxide capacitance, and W and L are the width and length respectively of the MOSFET transistor. Figure 10 illustrate the model used four simulate the effect of flicker noise

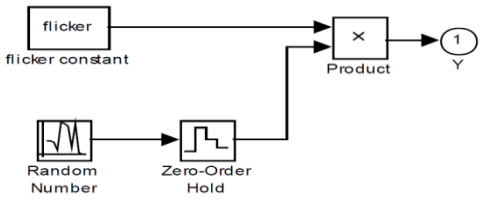

Figure 10. Flicker Noise Model

4.1.5. Thermal Noise

The thermal noise is present in all circuit elements containing resistor [16], a MOS transistor operating in the saturation region identical to a passive resistor between its drain and source terminals (the inversed channel), Thermal noise is caused by the random thermal motion of carriers in the channel [18], the short circuit thermal noise current spectral density Id is then given by

$$I_d^2 = 4KT\frac{2}{3}g_m \qquad (08)$$

Where k is the Boltzman constant, T represents the absolute temperature, and gm is the transconductance of the MOS transistor, this noise model is valid only for long channel devices, the new thermal noise in MOS transistors models have been described in the literature [19-20]

In small geometry devices the thermal noise was modeled as

$$I_d^2 = 4KT\frac{\mu_{eff}}{L_{eff}^2}Q_{inv}\Delta f \qquad (09)$$

Where µeff is the effective carrier mobility in the channel, Qinv is the inversion channel charge per unit area, Experimental results the thermal noise in the channel is directly proportional to the drain current [21], to keep the value of thermal noise low this correspond to smaller drain currents.

The thermal noise is usually modeled as an additive white noise source with Gaussian distribution, Figure 11 present the thermal noise model, it can be modeled as a random variable generator with zero-order block, the gain block is used to adjust the value of the total thermal noise.

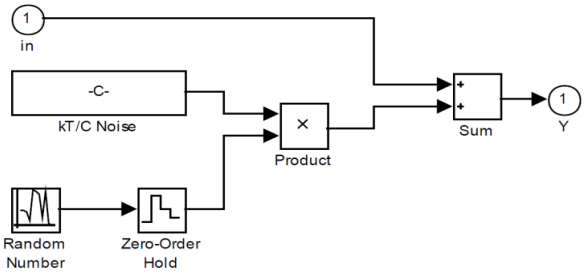

Figure 11. Thermal Noise Model

4.1.6. Settling Error

Settling time is the most important non-ideal factor associated in the current S/H circuits (SI memory cells), this defines the time it takes the output to reach its final value within a given settling error, Figure 12 below shows the qualitative behavior of the typical settling behavior of the step response.

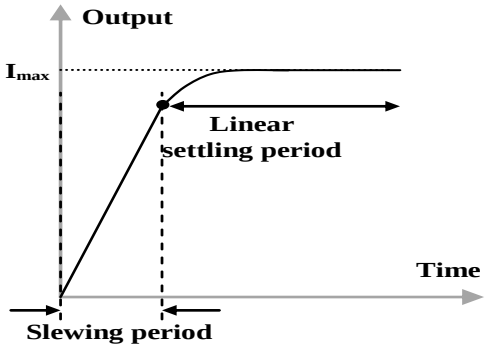

Figure 12. Step Response of Current Mode S/H

Suppose the sampling switch is closed at the instant t0, the transient response of the current S/H Ids can be expressed as [22]

$$\boldsymbol{i_{ds}(t) = I_i + (i_{ds}(t_0) - I_i) * e^{((t-t0)/\tau)}} \qquad (10)$$

The exponential term represents the settling errors of CM S/H circuit at the instant t,with τ=C/gm, and ids(t0)=gm.vgs(t0).

Settling errors in SI circuits should therefore generally be considered as non-linear errors [14].

4.2. Comparator Model

The comparator is a key component of the data converter as it is the link between the analogue and digital domain [23], the current comparator is a fundamental component of CM SAR ADC, a critical design aspect for comparator is good tradeoff between sensitivity, speed and power dissipation [24], Figure 13 present the comparator model, the input is the subtraction between the output of the S&H and the DAC. On the top of this, a constant value is added to this subtraction to model the offset of the real comparator (in the ideal case the value of the offset is zero). The result is then multiplied by a gain that represents the amplification stage. Then the result is saturated to full logic levels and compared to zero to define which of the two inputs the highest one is.

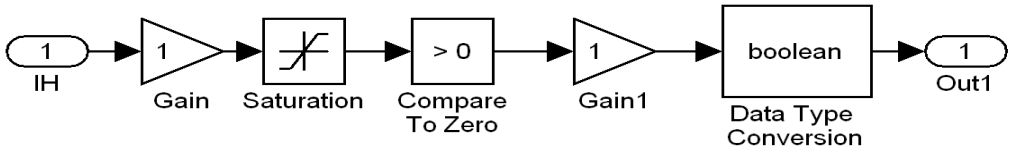

Figure 13. Comparator Ideal Model

The non ideal model of the CM comparator is shown in Figure 14 with the imperfection effects; the main limitation of the CM comparator the current offset due to process mismatch, thermal noise and the time response (delay time).

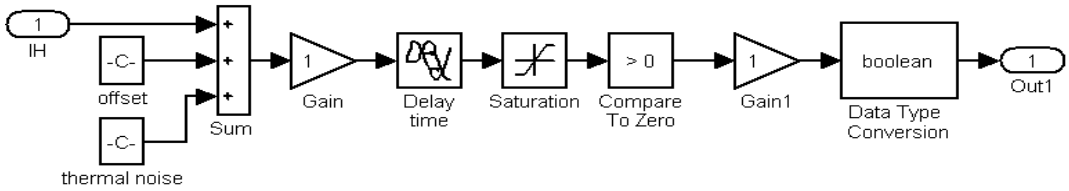

Figure 14. Comparator Non Ideal Model

4.3. SAR Logic Register

The SAR logic Register is the heart of the system. It generates the controls signal used by the current steering DAC. The logic block (as shown in Figure 15) has been implemented using two shift registers in order to perform the successive approximation routine. Each shift register is composed of a chain of nine D Flip-Flops. The shift register on the top is used as a sequencer and is synchronous with the internal clock. The bottom register stores the conversion value. Each sampled value (sampling is performed by S/H) of the analogue signal current input is compared by the current comparator with the output of the current DAC. The result of the comparison is used then by the SAR to elaborate the next step.

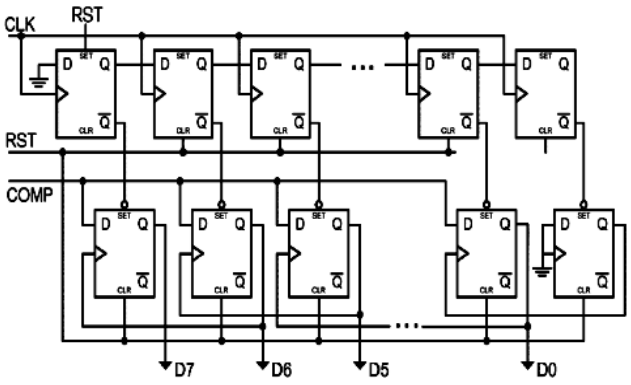

Figure 15. SAR Logic Register

4.4. 4 to 15 Binary to Thermometer Encoder

The 2-bit binary-to-thermometer encoder it consists of on AND gate and on OR gate this is the simplest form with the 2 bit input and 3 output, we call 2-3 encoding, bay using this structure to achieve 3-7 thermometer encoder, and with the same method we can achieve 4-15 thermometer encoder as shown in Figure 16, such as it consists of 08 OR gates and 08 AND gates, the main disadvantage of the thermometer encoder, the complex decoding logics and the large area requirement.

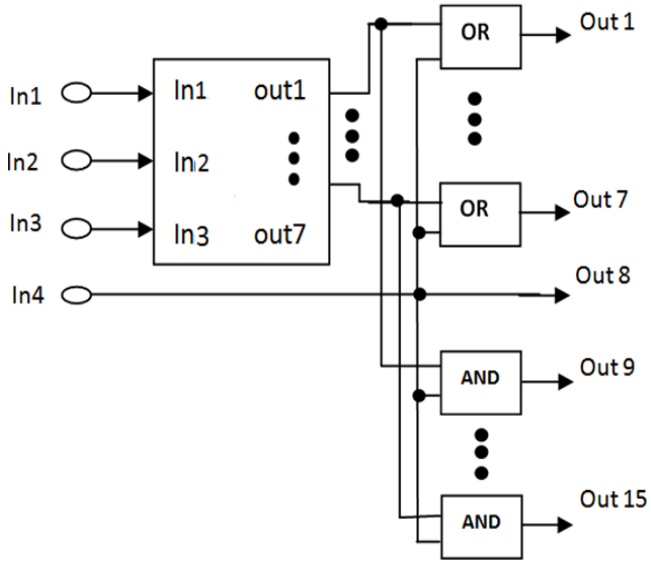

Figure 16. 4 to 15 Binary Thermometer Encoder

4.5. The Current Steering DAC

The current steering DAC is suitable for high speed and high resolution application [25]. Figure 17 displays general structure of proposed current steering DAC with thermometer code as according in ref [5]. The 8-bit input binary data is segmented into the 4 most significant bits (MSBs) and 4 least significant (LSBs), for 4 MSBs bits are decoded by the thermometer in order to control 15 identical current sources, such as the first MSB bit control 23 current source, the second MSB bit control 22 current sources, the third MSB bit control 21 current sources, and the fourth MSB bit control 20 current sources, and 4 LSBs are directly applied to the 4 current sources.

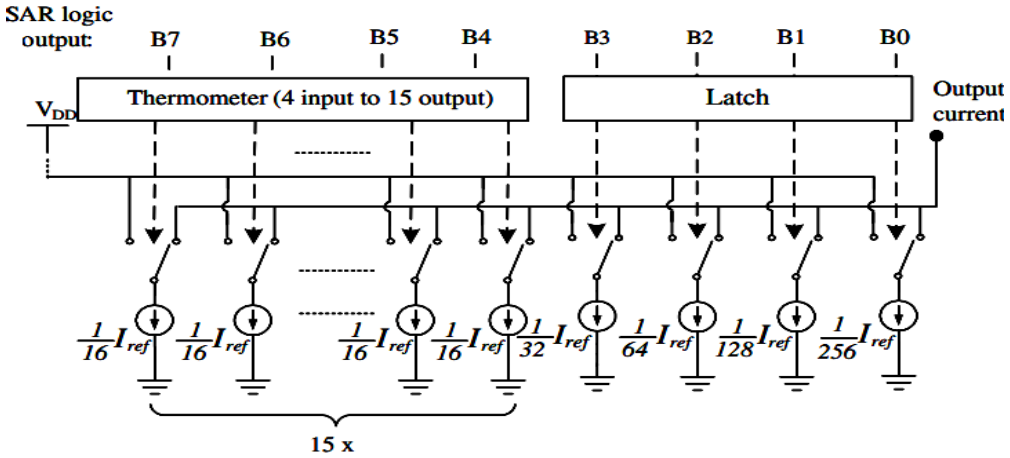

Figure 17. General Structure of Current-steering DAC

In the DAC model, each current source is multiplied by gain factor in such a way it became equal to the current source value, the model of DAC for 4 LSB bits it is shown in Figure 18.

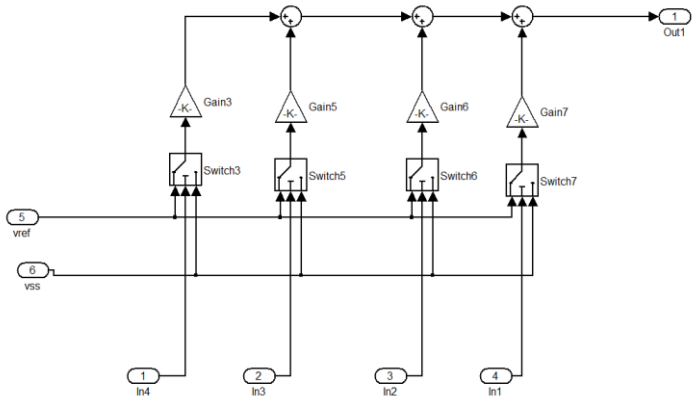

Figure 18. Model of Switches and Current Sources for 4 LSBs Bits

4.5.1. The Non Idealities in Current-Steering DAC

The current-steering DAC structure is shown in Figure 19, the advantage of this architecture it requires a small area by using small number of transistors, for 8 bits DAC we use 8 current sources and the same number of switch, the basic structure of this kind of DAC do not require no operational amplifier no feedback loops, Each current source utilizes 2K parallel unit current sources Iunit. The bits bi chooses which current sources to connect to the output, b0 is the least significant bit (LSB) and bn-1 is the most significant bit (MSB) [4].

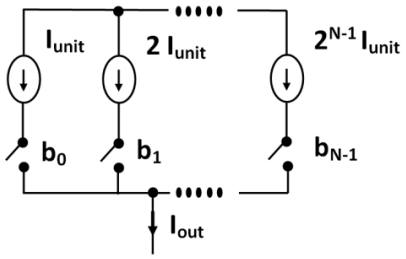

Figure 19. Current Steering DAC Architecture

For the ideal current steering DAC the total output current is give by this equation.

$$I_{OUT} = [b_{N-1}(n) * 2^{N-1} + \cdots + b_1(n) * 2 + b_0(n)] * I_{unit} \quad (11)$$

The performance of the DAC is limited due to non idealities sources errors, two critical basic building blocks used in current-steering DACs are the switches and the current source. The main non idealities factors we are included in the model are the non-idealities of switches and current source mismatch errors, the non ideality of the switches we are presented in the previous sections (charge injection, clock feed-through, clock jitter, settling errors, flicker noise and thermal noise), in the next section we will present the non ideality coming from mismatch of the devices (transistors) in current sources.

4.5.2. The Mismatch Analysis

The current-mode technique has main advantages pointed such as its high-speed, low voltage potential and its compatibility with digital CMOS technology. There is however a set of technical limitations, In CMOS circuits design, the matching determines the accuracy of the current source. The physical quantity such as the oxide thickness, threshold voltage, transistor width, varies over the chip area during the creation process. Due to the matching error, identical designed transistors become unmatched, the influence

of the matching errors makes the sizes of the transistors to differ from their designed values, and therefore the output current will not be correct.; in the circuits current S/H Figure 3 and current steering DAC; due to the mismatch cannot be realized exactly the ideal relation between the current of M0 and M1.

They are three types of mismatch, mismatch in transconductance (B1=B0+ΔB), mismatch in threshold voltage (Vth1=Vth0+ΔVth), and mismatch in channel length modulation (λ1=λ0+Δλ); the drain saturation current of transistors M0 is given by this equation.

$$I_{ds0} = \frac{B_0}{2} \times (V_{gs} - V_{th0})^2 \times (1 + \lambda_0 \times V_{ds0}) \quad (12)$$

The drain saturation current of transistor M1 is give by equation (13), this equation describer matching error due to the variation of process parameters.

$$I_{ds1} = \frac{B_0 + \Delta B}{2} \times (V_{gs} - (V_{th0} + \Delta V_{th}))^2 \times (1 + (\lambda_0 + \Delta\lambda) \times V_{ds}) \quad (13)$$

The basic circuit of current DAC using binary weighted current sources is shown in figure 20; the current mode DAC circuit consists of a binary weighted current splitting array using cascaded current mirrors, the current sources are connected in parallel to each other; and connected to the output node via MOS switches, which are controlled by the input code. Therefore, the output current of the DAC is proportional to the input code.

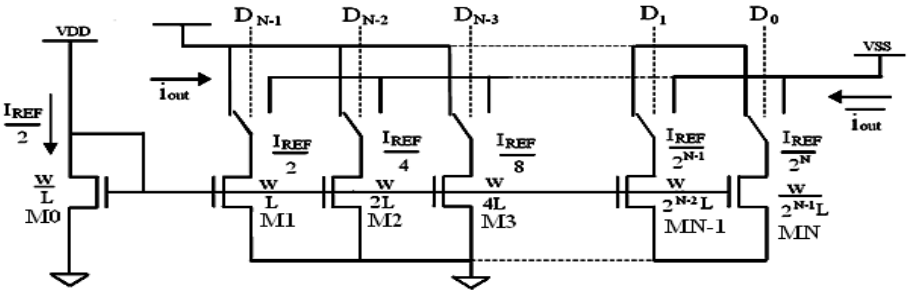

Figure 20. Basic Circuit of Current DAC using Binary Weighted Current Sources

The equation (17) illustrates the relation between the current of transistor M0 and each other transistors in the DAC.

$$\frac{I_{dsn}}{I_{ds1}} = \frac{B_n}{B_1} \times \frac{(V_{gs1} - V_{th})^2 \times (1 + \lambda \times V_{dsn})}{(V_{gs1} - V_{th})^2 \times (1 + \lambda \times V_{ds1})} \quad (14)$$

A current source with a mismatch error can be modeled as an additional current source in parallel with the nominal current source as illustrated in Figure 21 [25].

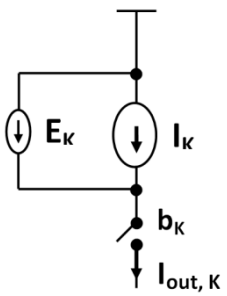

Figure 21. Model of Current Source with Matching Error

The total output current of the non-ideal DAC will now become

$$I_{OUT}(n) = \sum_{K=0}^{N-1} b_k\,(n) * I_{OUT,K} \qquad (15)$$

Where

$$I_{OUT,K}=I_{unit} * 2^K + E_K \qquad (16)$$

We can see from (18) the mismatch error in I_{bais} current source will only cause a constant offset EK in $I_{OUT,k}$.

5. Simulation Results

To check and to confirm the performance of the new proposed model with the various non idealities sources, simulation results verifies the performance from the behavioral level modeling, simulation is performed for the ideal and non-ideal model of the CM SAR ADC, its results are reported in these sections with the static and the dynamic performances.

5.1. Dynamic Performance

In order to test the model and to confirm its dynamic performance, an analogue signal equivalent to a sine wave with a frequency of 63 KHz is applied to the input of the ADC with sampling rate of 5 MHz as shown in figure 22. Simulation results of the output signal from the DAC and reconstructed analog signal from ADC are shown in figure 23 and 24.

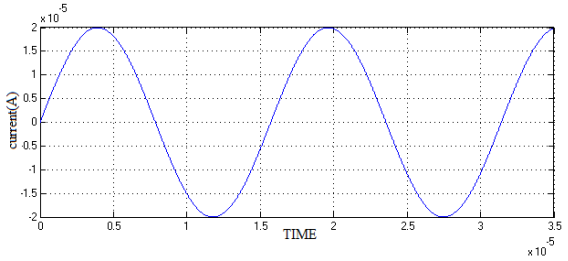

Figure 22. The Analogue Input Signal

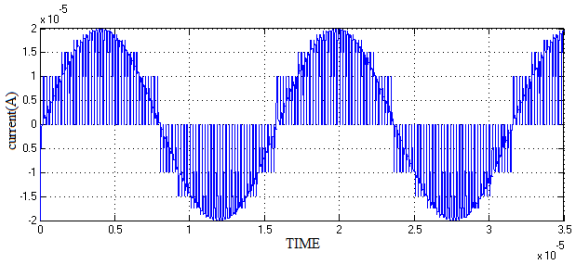

Figure 23. The Analogue Signal Output from the DAC

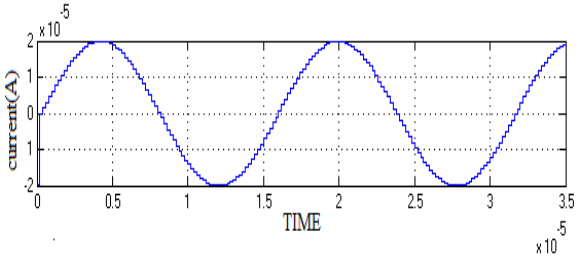

Figure 24. The Analogue Signal Reconstructed from the Output of the ADC

The dynamic performances including Signal to Noise Ratio (SNR), Spurious-Free Dynamic Range (SFDR) and Total Harmonic Distortion (THD). By using the Fast Fourier Transform (FFT), the SFDR and THD can be calculated from the power spectrum, the FFT output for an ideal model and a non-ideal model of CM SAR ADC are shown in Figure 25 and 26 respectively, For the ideal model we extracted a SNR is 49.25dB, the SNDR is 49.2 dB, The SFDR is 65.3 dB and the effective number of bits is ENOB=7.9bit, and for non-ideal model we have a SNR is 46.33 dB, the SNDR is 46.03 dB, The SFDR is 60.5 dB and the effective number of bits is ENOB=7.35bit.

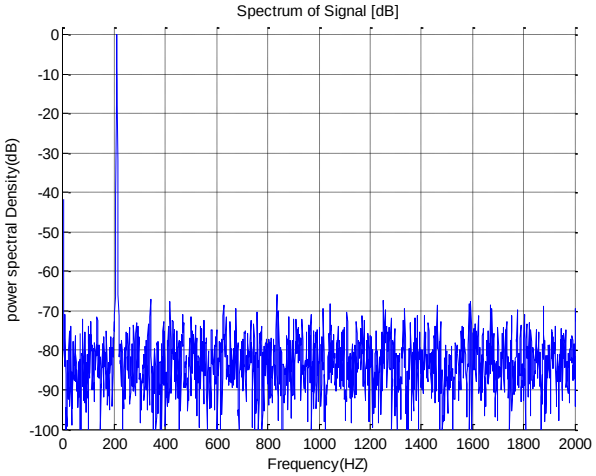

Figure 25. FFT of the ADC Output Signal in the Ideal Case with *F*in = 63 kHz*; Fs* = 12.5MHz

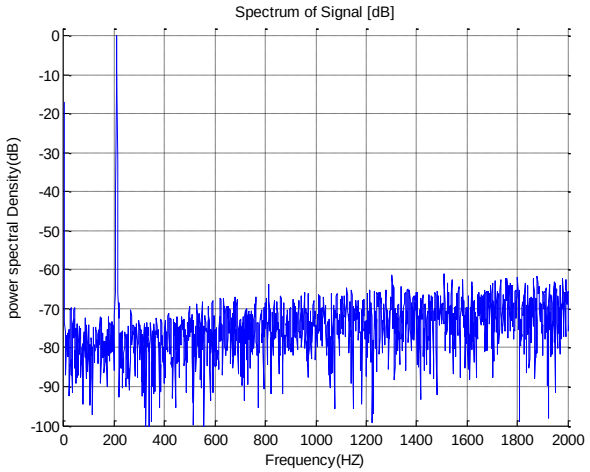

Figure 26. FFT of the ADC Output Signal in the Non-Ideal Case with *F*in = 63 kHz*; Fs* = 12.5MHz

5.2. Static Performance

The linearity is the most important parameter in the data converter. The linearity performance includes Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). The INL is defined as the maximum deviation of a transition point of a conversion from corresponding transition point of an ideal conversion. The INL is simulated using a MATLAB code. Based on INL definition, the LSB will be the deviation of the real transfer function from a straight line. For the DNL, it is defined as the difference between an actual step width and the ideal value of 1LSB. Hence, INL will

represent cumulative DNL errors. The INL is simulated using MATLAB code based by this equation

$$INL_J = \sum_{i=1}^{j-1} DNL_J \qquad (17)$$

The simulation results of DNL and INL for ideal model are shown in Figure 27 and Figure 28 respectively. The results are of a 8-bit current mode SAR ADC for ideal model. The simulation results show that the variation of the DNL and INL is more or less around 1LSB, it is between +0.02/-0.02 LSB for DNL, and for INL it is in the range of INLmax of +0.12 LSB and INLmin of -0.03 LSB.

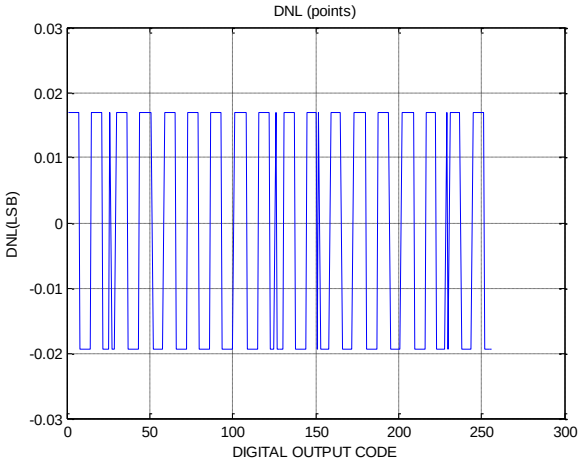

Figure 27. DNL of the Ideal 8 Bit Current Mode SAR ADC

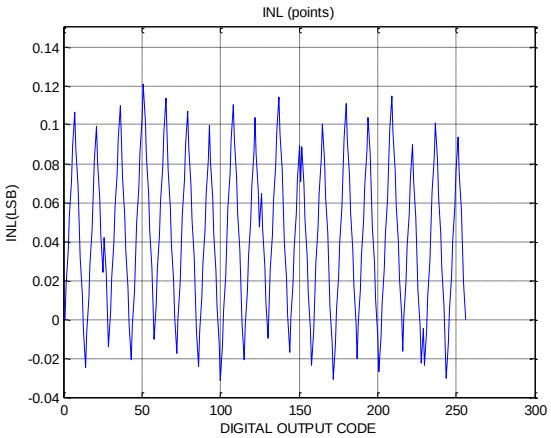

Figure 28. INL of the Ideal 8 Bit Current Mode SAR ADC

Figure 29 and 30 shows the simulated differential nonlinearity (DNL) and integral nonlinearity (INL) profiles of a 8-bit ADC including various non-idealities, The DNL is found to be −0.04/0.23 LSB, and the INL is −0.6/0.1 LSB.

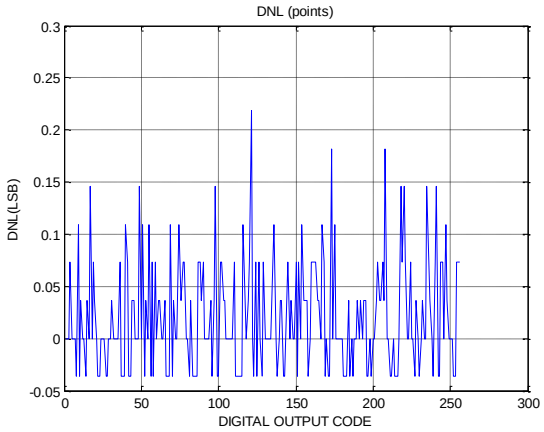

Figure 29. DNL of the Non-Ideal 8 Bit Current Mode SAR ADC

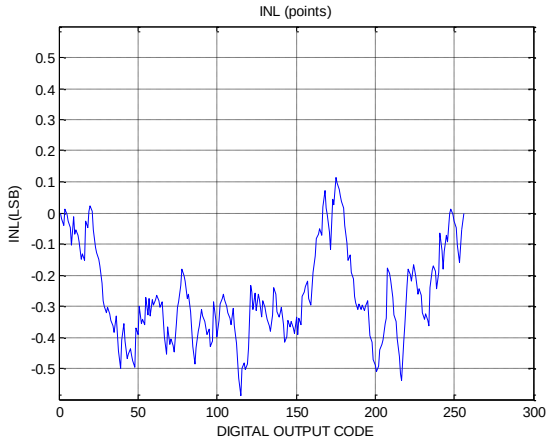

Figure 30. INL of the Non-Ideal 8 Bit Current Mode SAR ADC

The results of the behavioral level simulations were a set of specifications for the mentioned non-idealities, which are shown in Table 1.

Table 1. Specifications of the 08-bit CM SAR ADC Model

Specification	Value
Technology TSMC	0.18 μm
Resolution	08 bits
Hold capacitance *C*gs	0.08fF
Overlap capacitance Covl	0.08 fF
Oxide capacitance *C*ox	$8.78*10^{-3}$ F/m2
Sampling frequency *fs*	10MHz
Offset of the comparator	100nA
Delay time of the comparator	50ns
Current flicker noise	$50*10^{-12}$ A
DAC component matching (ε)	20 %

From the results presented in the previous sections, a comparison can be made between our behavioral model in the ideal and non ideal case to the real ADCs [5, 26]. It can be

seen from Table 02 that proposed models shows a good match to the real ADCs with current and voltage mode; this proves the accuracy of our behavior model.

Table 2. Comparison the Performance of the Current Mode SAR ADC MODEL

Parameters	This work/ Ideal model	This work/ Non ideal model	[5]	[26]
Mode	I-Mode	I-Mode	I-Mode	V-mode
Resolution (bit)	8-bits	8-bits	8-bits	8-bits
INL (LSB)	-0.023/0.12	-0.6/0.1	-0,56/0,9	-0.2/0.27
DNL (LSB)	-0.018/0.019	-0.04/0.23	-0,84/1,0	-0.18/0.34
SNR (dB)	49.25	46.33	/	/
SFDR (dB)	65.3	60.5	61.64	/
SNDR (dB)	49.2	46.03	46.2	48.2
ENOB (bit)	7.9	7.35	7.38	7.8

6. Conclusion

A new model of 8-bit CM SAR ADC has been reported. The analysis of static and dynamic performances using MATLAB environment confirm the good performance of the CM SAR ADC with its ideal and non ideal models. The conversion is performed without missing codes. In the non ideal behavioral model, the most non ideals sources in CM SAR ADC have been taken into account. For current comparator, it has been modeled by taking into account the offset with the delay time, the effect of the charge injection; clock feed-through, flicker noise and thermal noise for S/H. The matching errors of current sources and non-idealities of switches in the current steering DAC have been introduced. A behavioral model in Matlab simulink has been implemented to study the effects of non-idealities on the converter performances .The behavioral model and the simulation results will help the designer to achieve 8-bit CM SAR ADC circuit with a low power, a current range in the scale of µA and high efficiency in the chip area by using current steering DAC.

References

[1] C. Toumazou, F. J. Lidgey, D. G. Haigh (Eds.), "Analogue IC Design: the Current Mode Approach", IEE Circuits and Systems Series 2, **(1990)**.
[3] Y.-Z. Lin, C.-C. Liu, G.-Y. Huang, "A 9-Bit 150-MS/s Subrange ADC Based on SAR Architecture in 90-nm CMOS", IEEE Transactions on Circuits and Systems-I, vol. 60, no. 3, **(2013)** March, pp. 570-581.
[4] N. Nambiar, B. J. Blalock and M. N. Ericson, "A Novel Current-mode Multi-channel Integrating ADC", Analog Integr Circ Sig Process, vol. 63, **(2010)**, pp.283–291.
[5] X. Tang and K. P. Pun, "A Novel Switched-Current Successive Approximation ADC", Journal of Circuits Systems, and Computers, vol. 20, no. 1, **(2011)**, pp.15-27.
[6] W. Hu, Donald, Y.C. Lie, and Y.-T. Liu, "An 8-bit Single-Ended Ultra-Low-Power SAR ADC with a Novel DAC Switching Method", IEEE Transactions on Circuits and Systems-I, vol. 60, no. 7, **(2013)**, pp. 1726–1739.
[7] S. Heydarzadeh, A. Kadivarian, and P. Torkzadeh, "Implemented 5-bit 125-MS/s Successive Approximation Register ADC on FPGA", World Academy of Science, Engineering and Technology, vol. 69, **(2012)**, pp. 394-397.
[8] R. Dlugosz and K. Iniewski, "Flexible Architecture of Ultra-low-power Current-mode Interleaved Successive Approximation Analog-to-digital Converter for Wireless Sensor Networks", VLSI Design, vol. 2007, no. 2, **(2007)**, pp.1–13.
[9] S. Heydarzadeh, A. Kadivarian, and P. Torkzadeh, "Implemented 5-bit 125-MS/s Successive Approximation Register ADC on FPGA", World Academy of Science, Engineering and Technology, vol. 69, **(2012)**, pp. 394-397.
[10] R. Dlugosz and K. Iniewski, "Flexible Architecture of Ultra-low-power Current-mode Interleaved Successive Approximation Analog-to-digital Converter for Wireless Sensor Networks",VLSI Design, vol. 7, no. 2, **(2007)**, pp.1–13.

[11] O. Hashemipour, and S. G. Nabavi, "A 1.5V 100MS/S 12 Bit Current-mode CMOS Sample and hold", World Academy of Science, Engineering and Technology, **(2006)**.
[12] Y. Sugimoto, "A 1.5-V Current-Mode CMOS Sample-and-Hold IC with 57-dB S/N at 20 MS/s and 54-dB S/N at 30 MS/s", IEEE Journal of Solid-State Circuits, vol. 36, no.4, **(2001)** April.
[13] E. Bilhan, P. C. Estrada-Gutierrez, A. Y. Valero-Lopez and F. Maloberti, "Behavioral Model of Pipeline ADC by Using Simulink", Southwest Symposium on Mixed-Signal Design SSMSD, **(2001)**, p 147 – 151.
[14] B. Jonsson, "Switched-Current Circuits: from Building Blocks to Mixed Analog- Digital Systems", Ph.D thesis, Royal Institute of Technology, Stockholm, **(1999)**.
[15] S. Barra, A. Dendouga, S. Kouda and N.-E. Bouguechal, "Contribution to the Analysis and Modeling of the Non Ideal Effects of Pipelined ADCs using MATLAB",Journal of Circuits Systems and Computers, vol. 22, no. 2, **(2013)** February.
[16] Y. Tsividis, "Operation and Modeling of the MOS Transistor, 2nd ed.", Boston: McGraw-Hill, **(1999)**.
[17] J. M. de la Rosa , B. P. Verdú and A. R. Vázquez , "Systematic Design of CMOS Switched-Current Bandpass Sigma-Delta Modulators for Digital Communication Chips", Kluwer Academic Publishers, New York, **(2002)**, p. 179.
[18] M. Helfenstein and George S. Moschytz, "Improved Two Step Compensation Technique for Switched-currents", IEEE Trans, on Circuits and Systems, vol. 45, no. 6, **(1998)**, pp. 739-743.
[19] L.J. Sander., G. Eric, A. M. Klumperink, A. P. V. der Wel, G. Hoogzaad, E. van Tulji, and B. Nauta, "Intrinsic 1/f Device Noise Reduction and its Effect on Phase Noise in CMOS Ring Oscillators", IEEE Journal of Solid-State Circuits, vol. 34, no. 7, **(1999)**, pp.1022-1025.
[20] G. Knoblinger, P. Klein, and M. Tiebout, "A New Model for Thermal Channel Noise of Deep-Submicron MOSFETS and its Application in RF-CMOS Design", IEEE Journal of Solid-State Circuits, vol. 36, no. 5, **(2001)**, pp. 831-837.
[21] D. D. Venuto, D. T. Castro, Y. Ponomarev and E. Stikvoort, "0.8 mW 12-bit SAR ADC Sensors Interface for RFID Applications", Microelectronics Journal, vol.41, **(2010)**, pp.746–751.
[22] J. M. de la Rosa, B. P. Verdú and A. R. Vázquez, Systematic Design of CMOS Switched Current Bandpass Sigma-delta Modulators for Digital Communication Chips, Kluwer Academic Publishers, Dordrecht, **(2002)**, pp. 148-149.
[23] M.S. Bhat and H.S. Jamadagni, "Power Optimization in Current Mode Circuits", Proceeding of 18th International Conference on VLSI Design, **(2005)**, pp.1063-9667.
[24] I. Myderrizi, and A. Zeki, "Behavioral Model of Segmented Current-Steering DAC by Using SIMULINK", in the Proceeding of Ph.D Research in Microelectronics and Electronics, **(2009)**, pp.156 – 159.
[25] O. Andersson, "Mismatch Modeling and Design of CMOS Current-Steering Digital-to Analog Converters", Thesis for Degree of Master of Science, Department of Electrical Engineering, Linköping University, Sweden, pp. 08-09, **(1999)** November.
[26] W. Hu, D. Y.C. Lie and Y.-T. Liu, "An 8-bit Single-Ended Ultra-Low-Power SAR ADC with a Novel DAC Switching Method", Journal on Electrical Engineering, Special Issue on VLSI Design Methodologies/Embedded Systems, vol. 4, no. 3, **(2011)**, pp. 17-22.

