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FPGA-Based Model-Free Nonlinear Control Approach with Application to First Order Delays System

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Abstract

The Proportional-Integral-Derivative (PID) controller to control of first order delay system has fluctuations in presence of uncertainty. To reduce the rate of fluctuations as well as improve the first order delay rise time, the first objective is design a Proportional-Integral-Integral-Derivative (PI^2D) controller. This algorithm is complex control technique which requires faster micro-controllers; therefore the second objective of this article is to present the implementation of the PI^2D on the Field Programmable Gate Array (FPGA). The maximum output required time in PI^2D is 32.88 ns and the maximum output frequency in PI^2D algorithm is 30.4 MHZ.

Keywords: *First order delays system, PID controller, PI^2D algorithm, FPGA control algorithm*

1. First Order Delay System

First order delay (FOD) is a nonlinear and time variant system. A first order model can represent many industrial processes; Equation (1) shows the mathematical plant model (in *s-plane*). Discrete transfer function of this model has obtained using ZOH method, and the selected sampling period (T) is 0.1, Equation (2) shows the discrete transfer functions, (in *z-plane*).

$$CS_1(s) = \frac{1}{S+1} \tag{1}$$

and;

$$CS_1(z) = \frac{0.09516}{Z-0.9048}, T = 0.1 \tag{2}$$

The time delay occurs when a sensor or an actuator are used with a physical separation. Equation (3), shows the mathematical plant model (in *s-plane*). Discrete transfer functions of this model has been obtained using ZOH method, and the selected sampling period (T) is 0.1, Equation (4 and 5), show the discrete transfer functions, (in *z-plane*).

$$CS_2(s) = \frac{1}{S^2 \times (S+1)} \tag{3}$$

$$CS_2(z) = Z^{-2} \times CS_1(z) \tag{4}$$

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$$CS_2(z) = Z^{-2} \times \frac{0.09516}{Z - 0.9048}, T = 0.1 \quad (5)$$

2. MATLAB-Based Controller

Design PID and PI^{2}D MATLAB-based controller introduce in this part. The formulation of PID controller is:

$$U_{PID} = K_p \times e + K_v\left(\frac{de}{dt}\right) + K_i \int e\, dt = K_p \times e + K_v \dot{e} + K_i \sum e \quad (6)$$

Where $\boldsymbol{e} = \boldsymbol{q_{i_d}} - \boldsymbol{q_{i_a}}$, $\dot{\boldsymbol{e}} = \dot{\boldsymbol{q}}_{\boldsymbol{i_d}} - \dot{\boldsymbol{q}}_{\boldsymbol{i_a}}$ and $\sum \boldsymbol{e} = \int (\boldsymbol{q_{i_d}} - \boldsymbol{q_{i_a}})$.
To show this controller is stable and achieves zero steady state error, the Lyapunov function is introduced;

$$V = \frac{1}{2}\left[\dot{q}^T S\dot{q} + e^T K_p e\right] = \quad (7)$$

$$\frac{1}{2}\frac{d}{dt}\left[\dot{q}^T S\dot{q}\right] = \dot{q}\, U$$

If the conversation energy is written by the following form:

$$\frac{1}{2}\frac{d}{dt}\left[\dot{q}^T S\dot{q}\right] = \dot{q}\, U \quad (8)$$

Where $(\dot{\boldsymbol{q}}\, \boldsymbol{U})$ shows the power inputs and $\frac{\boldsymbol{1}}{\boldsymbol{2}}\frac{\boldsymbol{d}}{\boldsymbol{dt}}\left[\dot{\boldsymbol{q}}^{\boldsymbol{T}}\, \boldsymbol{S}\dot{\boldsymbol{q}}\right]$ is the derivative of the kinetic energy.

$$\dot{V} = \dot{q}^T\left[U + K_p e\right] \quad (9)$$

Based on $\boldsymbol{U} = -\boldsymbol{K_{p_i}}\boldsymbol{e} - \boldsymbol{K_{v_i}}\dot{\boldsymbol{e}}$, we can write:

$$\dot{V} = \dot{q}^T K_p \dot{q} \leq 0 \quad (10)$$

If $\dot{\boldsymbol{V}} = \boldsymbol{0}$, we have

$$\dot{q} = 0 \rightarrow \ddot{q} = 0 \rightarrow \ddot{q} = A^{-1}K_p e \rightarrow e = 0 \quad (11)$$

In this state, the actual trajectories converge to the desired state.

However, PID controller is used in many applications but it has the challenge in presence of uncertainty. To reduce these challenges PI^{2}D controller is introduced.

$$U_{PI^2D} = K_p \times e + K_v\left(\frac{de}{dt}\right) + \left[K_{i_1}\int e\, dt \times K_{i_2}\int e\, dt\right] = K_p \times e + K_v\dot{e} + K_{i_1} \times K_{i_2}(\sum e)^2 \quad (12)$$

$$U_{PI^2D} = K_p + K_v S + \frac{K_{i_1} \times K_{i_2}}{S^2} \quad (13)$$

Lyapunov function is introduced;

$$V = \frac{1}{2}\left[\dot{q}^T S\dot{q} + e^T K_p e + \frac{K_{i_1} \times K_{i_2}}{S^2} e^T\right] = \quad (14)$$

$$\frac{1}{2}\frac{d}{dt}\left[\dot{q}^T S\dot{q}\right] + \frac{1}{2}\frac{K_{i_1} \times K_{i_2}}{S^2} = \dot{q}\, U + \sum U$$

$$\dot{V} = \dot{q}^T\left[U + K_p e + K_{i_1} \times K_{i_2}\sum U\right] \quad (15)$$

If $\dot{V} = 0$

$$\dot{q} = 0 \rightarrow \ddot{q} = 0 \rightarrow \ddot{q} = K_p e + K_{i_1} \times K_{i_2} \dot{e} \rightarrow e = 0 \, or \, \dot{e} = 0 \quad (16)$$

Figure 1, shows the trajectory following in PID controller, PI2D controller, and control free in first order delay system. Regarding the following graph, the rise time in control free first order delay system in a certain condition is about 3.939 seconds and, the rise time in PID control algorithm is about 0.36 seconds and PI^{2}D controller reduces the rise time to 0.023 seconds.

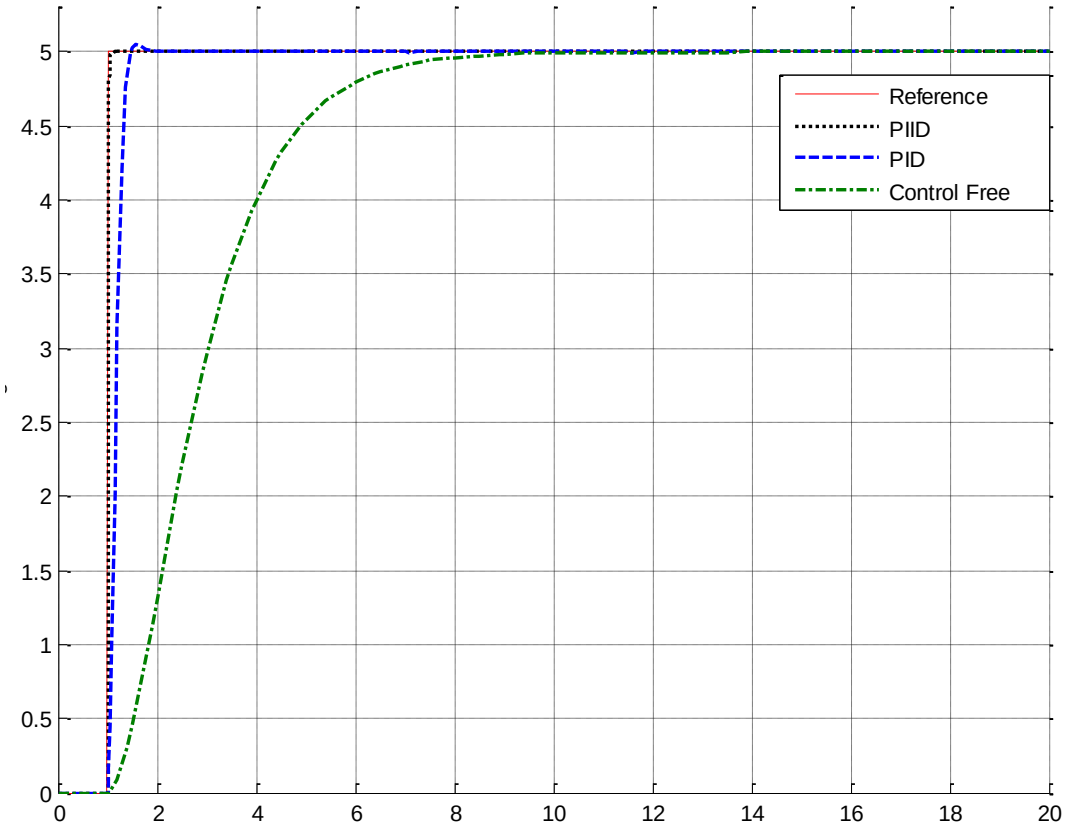

Figure 1. Trajectory Following: PID Controller, PI^{2}D and Control Free

Figure 2, shows the power of disturbance rejection in PID controller, PI^{2}D controller, and control free for first order delay system. In presence of uncertainty, PI^{2}D controller is robust than PID controller and control free technique. Based on the following graph, the rate of overshoot in PID controller has increased from 5% in a certain condition to 50% in uncertain condition. The rate of overshoot in PI^{2}D increased as well as PID controller from 0% in the certain condition to 7% in presence of uncertainty. The second parameters to the comparison between PID and PI^{2}D algorithm are rise time. The rate of rise-time in PID controller has increased from 0.36 second to 1.3 seconds in presence of uncertainty. However, the activation time in PID controller has been changed but PI^{2}D controller has the steady stable in this factor.

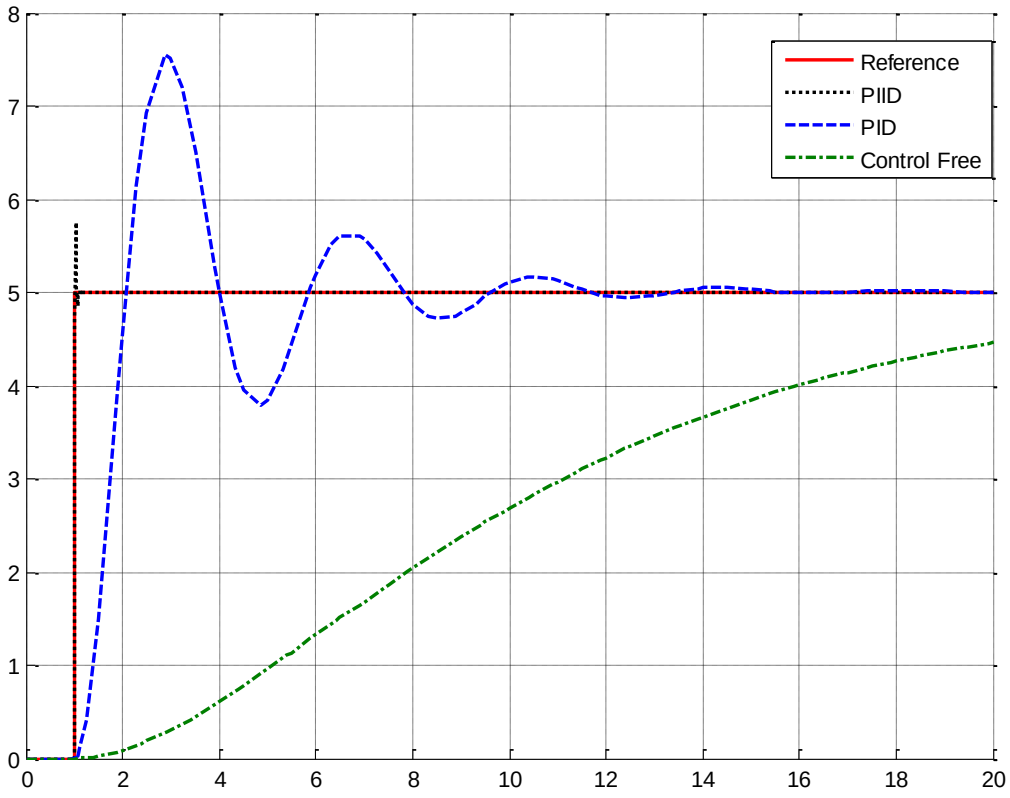

Figure 2. Disturbance Rejection: PID Controller, PI^{2}D and Control Free

3. FPGA-Based Algorithm

The following formulation shows the derivative algorithm [1-2]:

$$d(e) = \frac{Din(t) - Din(t-1)}{\Delta t} = \big(Din(k+1) - Din(k)\big) \times sample\ time \tag{17}$$

$$Din = q_d - q_a \tag{18}$$

However $\boldsymbol{q_d}$ **and** $\boldsymbol{q_a}$ are 30 bits but Din is 40 bits. In derivative algorithm, delay time is the main challenge. In this research the value of sample time is"01010". To design $\boldsymbol{Din(k+1)}$**,** design a register has the main role. The vast majority of modern commercial systems are built with registers using positive edge-triggered D flip-flops. The following formulation shows the derivative algorithm [1-3]:

$$I(out)_{(K)} = I(out)_{(k-1)} + (Ki \times e(k) \times sample\ time) \tag{19}$$

The Z formulation of PID controller is design as follows [4-5]:

$$U[k] = U[k-1] + K_1 \times e[k] + K_2 \times e[k-1] + K_3 \times e[k-2] \tag{20}$$

Figure 3, shows the HDL synthesize report for PID algorithm.

```
---------------------------------------------------------------------
HDL Synthesis Report

Macro Statistics
# Multipliers                                      : 4
 40x5-bit multiplier                              : 1
 40x8-bit multiplier                              : 3
# Adders/Subtractors                               : 5
 40-bit adder                                     : 3
 40-bit subtractor                                : 2
# Registers                                        : 9
 1-bit register                                   : 2
 40-bit register                                  : 7
```

Figure 3. HDL Synthesis Report: PID Algorithm

Figure 4, shows advanced HDL synthesis report in PID algorithm.

```
Advanced HDL Synthesis Report

Macro Statistics
# Multipliers                                      : 4
 40x5-bit multiplier                              : 1
 40x8-bit multiplier                              : 2
 40x8-bit registered multiplier                   : 1
# Adders/Subtractors                               : 5
 35-bit adder                                     : 2
 40-bit adder                                     : 1
 40-bit subtractor                                : 2
# Registers                                        : 224
 Flip-Flops                                       : 224
```

Figure 4. Advanced HDL Synthesis Report: PID Algorithm

Figure 5, shows the device utilization summary in PID algorithm.

```
Device utilization summary:
---------------------------

Selected Device : xa3s1600efgg400-4

 Number of Slices:                      219  out of  14752     1%
 Number of Slice Flip Flops:            153  out of  29504     0%
 Number of 4 input LUTs:                264  out of  29504     0%
 Number of IOs:                          98
 Number of bonded IOBs:                  98  out of    304    32%
    IOB Flip Flops:                      60
 Number of MULT18X18SIOs:                12  out of     36    33%
 Number of GCLKs:                         2  out of     24     8%
```

Figure 5. Device Utilization Summary: PID Algorithm

Figure 6, shows the timing summary in PID algorithm.

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 15.716ns (Maximum Frequency: 63.629MHz)
   Minimum input arrival time before clock: 4.683ns
   Maximum output required time after clock: 22.296ns
   Maximum combinational path delay: No path found
```

Figure 6. Timing Summary: PID Algorithm

Regarding to Figure 6, the Maximum frequency in this design is **44.85 MHz**. however the rate of clock is 63.629 MHz but in PID algorithm the maximum frequency is 44.85MHz.

The FPGA-based PI^{2}D formulation is:

$$U[k] = U[k-1] + K_1 \times e[k] + K_2 \times e[k-1] + K_3 \times e[k-2] \times e[k-3] \quad (21)$$

Figure 7, shows the HDL synthesize report for PI^{2}D algorithm.

```
HDL Synthesis Report

Macro Statistics
# Multipliers                                      : 5
 40x5-bit multiplier                               : 1
 40x8-bit multiplier                               : 3
 48x35-bit multiplier                              : 1
# Adders/Subtractors                               : 5
 40-bit adder                                      : 3
 40-bit subtractor                                 : 2
# Registers                                        : 9
 1-bit register                                    : 2
 40-bit register                                   : 7
```

Figure 7. HDL Synthesis Report: PI^{2}D Algorithm

Figure 8, shows advanced HDL synthesis report in PI^{2}D algorithm.

```
Advanced HDL Synthesis Report

Macro Statistics
# Multipliers                                      : 5
 40x5-bit multiplier                               : 1
 40x8-bit multiplier                               : 2
 40x8-bit registered multiplier                    : 1
 48x35-bit multiplier                              : 1
# Adders/Subtractors                               : 5
 35-bit adder                                      : 2
 40-bit adder                                      : 1
 40-bit subtractor                                 : 2
# Registers                                        : 224
 Flip-Flops                                        : 224
```

Figure 8. Advanced HDL Synthesis Report: PI^{2}D Algorithm

Figure 9, shows the device utilization summary in PI^{2}D algorithm.

```
Device utilization summary:
---------------------------

Selected Device : xa3s1600efgg400-4

 Number of Slices:                      264  out of  14752     1%
 Number of Slice Flip Flops:            153  out of  29504     0%
 Number of 4 input LUTs:                350  out of  29504     1%
 Number of IOs:                         140
 Number of bonded IOBs:                 140  out of    304    46%
    IOB Flip Flops:                      60
 Number of MULT18X18SIOs:                17  out of     36    47%
 Number of GCLKs:                         2  out of     24     8%
```

Figure 9. Device Utilization Summary: PI^{2}D Algorithm

According to Figure 9, and compared with Figure 5; the numbers of slices are increases from 219 in PID technique to 264 in PI^{2}D. The numbers of LUTs are increases from 264 in PID technique to 350 in PI^{2}D. The numbers of IOs are increases from 98 in PID technique to 140 in PI^{2}D. The rates of bounded IOs are increase from 32% in PID to 46% in PI^{2}D. The rates of multipliers are increase from 33% in PID to 47% in PI^{2}D.

Figure 10, shows the timing summary in PI^{2}D algorithm.

```
Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 15.716ns (Maximum Frequency: 63.629MHz)
   Minimum input arrival time before clock: 4.683ns
   Maximum output required time after clock: 32.880ns
   Maximum combinational path delay: No path found
```

Figure 10. Timing Summary: PI^{2}D Algorithm

Regarding to Figure 10, the Maximum frequency in this design is **30.4 MHz**. However the rate of clock is 63.629 MHz but in PI^{2}D algorithm the maximum frequency is 30.4MHz. According to comparison between PID and PI^{2}D, the maximum output required time in PID is 22.29 ns but in PI^{2}D is 32.88 ns and the maximum output frequency in PID controller is 44.85 MHZ but in PI^{2}D algorithm is 30.4 MHZ.

5. Conclusion

In this paper, FPGA-based PI^{2}D (nonlinear) controller for delay system is design and analysis. In rise time point of view, the rise time in PI^{2}D is better than PID algorithm in certain as well as uncertain condition. In robustness and stability point of view, PI^{2}D is more stable than PID algorithm (Figure 2). In uncertain condition PID controller has oscillation which caused to instability in delay system. According to comparison between FPGA-based PID and FPGA-based PI^{2}D controllers, the maximum output required time in PID is 22.29 ns but in PI^{2}D is 32.88 ns and the maximum output frequency in PID controller is 44.85 MHZ but in PI^{2}D algorithm is 30.4 MHZ.

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Iranian center of Advance Science and Technology (IRAN SSP) is one of the independent research centers specializing in research and training across of Control and Automation, Electrical and Electronic Engineering, and Mechatronics & Robotics in Iran. At IRAN SSP research center, we are united and energized by one mission to discover and develop innovative engineering methodology that solve the most important challenges in field of advance science and technology. The IRAN SSP Center is instead to fill a long standing void in applied engineering by linking the training a development function one side and policy research on the other. This center divided into two main units:

- Education unit
- Research and Development unit

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Dr. Nasri Sulaiman advisor and supervisor of several high impact projects involving more than 150 researchers from countries around the world including Iran, Malaysia, Finland, Italy, Germany, South Korea, Australia, and the United States. Dr. Nasri Sulaiman has authored or co-authored more than 80 papers in academic journals, conference papers and book chapters. His papers have been cited at least 3000 times by independent and dependent researchers from around the world including Iran, Algeria, Pakistan, India, China, Malaysia, Egypt, Columbia, Canada, United Kingdom, Turkey, Taiwan, Japan, South Korea, Italy, France, Thailand, Brazil and more.

Dr. Nasri Sulaiman has employed his remarkable expertise in these areas to make outstanding contributions as detailed below:

Design of a reconfigurable Fast Fourier Transform (FFT) Processor using multi-objective Genetic Algorithms (2008-UPM)

Power consumption investigation in reconfigurable Fast Fourier Transform (FFT) processor (2010-UPM)

Crest factor reduction And digital predistortion Implementation in Orthogonal frequency Division multiplexing (ofdm) systems (2011-UPM)

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