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Low Power with Minimal Delay Phase Frequency Detector

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Abstract

Phase frequency detector is the main component that is used in almost all high speed communication system especially in sensors. With the improving technology it is important for phase frequency detector to meet the requirement of modern communication system. Such requirements can be improved delay and less power consumption. With this idea this paper presents the Phase Frequency Detector having less power consumption and minimal delay. Conventional latch based phase frequency detectors are most commonly used, therefore we propose an enhanced phase frequency detector which can meet the requirement of modern circuits and will reduce the shortcomings of conventional circuit. In this paper standard D flip flop is simulated and then a comparison is made between conventional and proposed model .The proposed model uses two extra transistors to reduce the blind zone, dead zone which ensures improved device characteristics. Simulations are done using tanner v14.11 tools with .35 µm CMOS technology.

Keywords*: PFD, CMOS, PLL, LPF*

1. Introduction

An ideal PD is a digital circuit whose output value is linearly proportional to the difference between the phases of the two inputs signals. Typically, the width pulse is equal to the time difference between consecutive zero crossings of the two inputs.

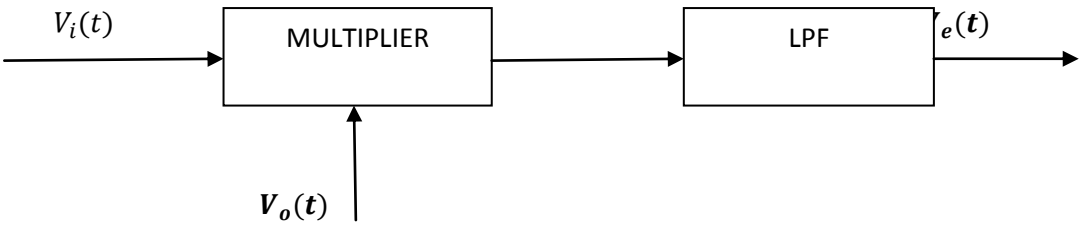

Figure 1. Implementation of PD

Phase detector can be realization a multiplier followed by a low pass filter. Multiplier will multiply input signal x_r and output of Voltage control oscillator e_o and then low pass filter is used which will filter out unwanted frequencies. When we multiply two signal, we will get a sine function of a sum frequency component and a difference frequency component. The sum frequency component will be low pass signal filtered out by LPF and output will contain difference of $\emptyset(t) - \theta(t)$(insatntaneos phase error).
Let output of phase detector is e_d (output of LPF) and is given by the equation:

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$$e_d = \frac{1}{2} A_c A_v k_d \, Sin \, [\emptyset(t) - \theta(t)] \quad (1)$$

k_d is associated with multiplier.

Phase Frequency Detector

These special detectors are allowed to detect both phase and frequency difference proves extremely useful because it significantly increases the acquisition range and lock speed of PLLs.

Unlike multipliers and XORs, sequential phase/frequency detectors (PFDs) generate two outputs that are not complementary.

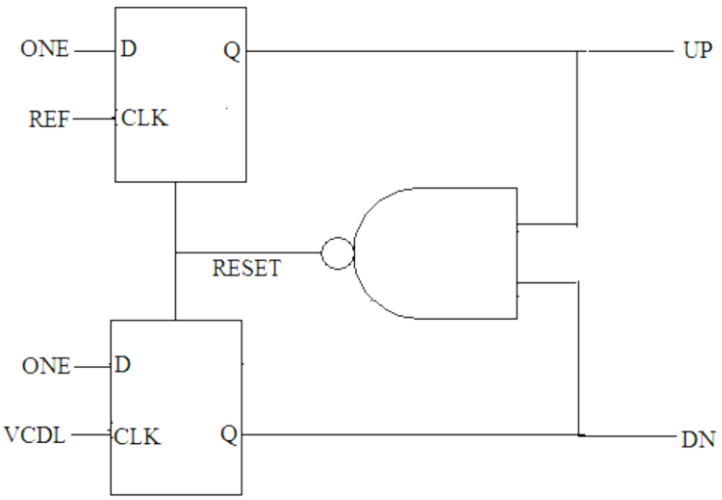

Figure 2. Standard PFD

Phase frequency detector diagram is shown in Figure 2, It has two inputs REF and VCDL and D is given V_{dd} and having two outputs UP and DN (Up and Down). Working of PFD can be clearly explained with the help of state diagram shown in Figure 3.

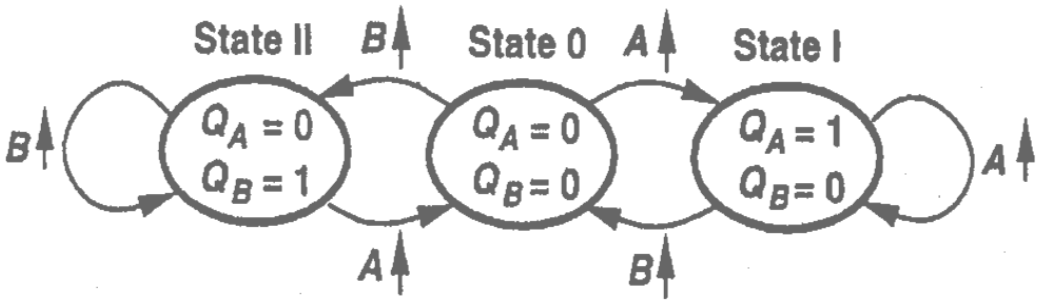

Figure 3. State Diagram of PFD

PFD is known as a tristate device because it has three states of operation: Reset state(State 0), Up state(state I) and Down state (state II) as shown in Figure 3.If both inputs Q_A and Q_B is low then the output will at state 0 which is reset state. If Transition occurs in Q_A then it will go to stage 1 that is output is Up. In this state Q_B remains low. If at state 1 transition occurs at Q_B making it high then both the inputs are high making the pfd to reset state PFD will move to state 0 again. If transition occurs at Q_B making it high

then PFD will move to state and if transition occurs at Q_A then both the inputs become high moving the output to reset state that is state 0.

2. Conventional PFD

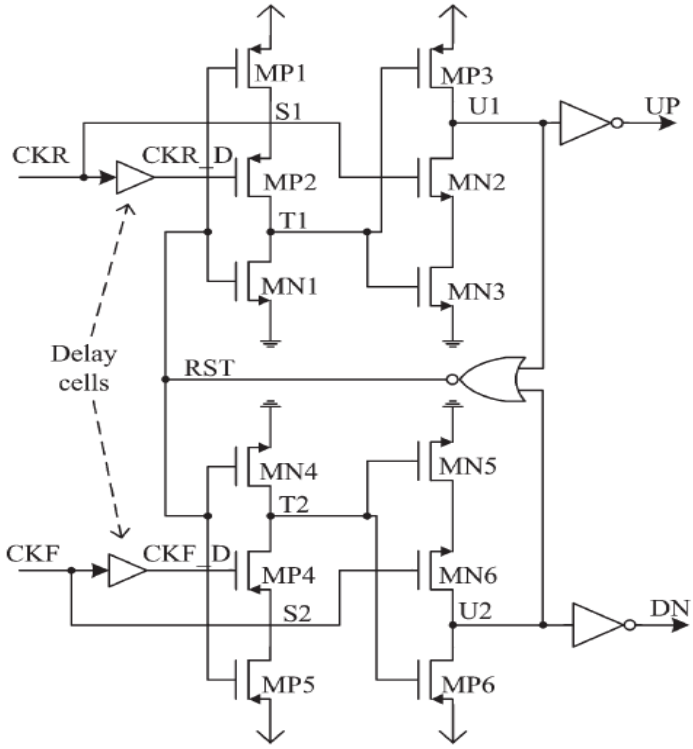

Figure 5. Conventional PFD with Delay Cell

Conventional PFD circuit consists of two PFDs whose output are latched to a Nor gate.The biggest problem faced by a conventional PFD is high power consumption, dead zone and blind zone. Power consumption can be reduced by proper reduction of dead zone and blind zone. Dead zone is the minimum pulsewidth of the PFD output that is needed to turn on the charge pump completely.

To mitigate the dead-zone issue, the reset signal inside the tristate PFD can be designed to trigger pulses with a constant width at the PFD outputs when the phases of the inputs are aligned.

However, since the circuits cannot work during the reset process, a blind zone, where the PFD cannot react to any transitions on the input signals, is inherent in the circuits. If the phase difference falls into the blind zone during the frequency acquisition, the PFD delivers incorrect phase information to the charge pump and shifts the phase toward the opposite direction, which aggravates cycle slips and elongates the frequency pulling time, as proven in [5-7]. The increased chance of cycle slips adversely affects the PLL frequency acquisition time and is undesirable in systems that require fast frequency transition, such as the multiband orthogonal frequency-division multiplexing system.

The chance that phase difference will fall in blind zone is completely random and to remove the cycle slips we need to simply reduce the blind zone. Earlier research tells us the effect of delay cells to reduce blind zone and therefore we had added an extra delay cell in the conventional PFD. It improves the performance of PFD but pull ups problems are the same.

3. Enhanced PFD

Enhanced PFD combines the high-speed PFD proposed in [3] with a delay cell and two extra transistors. The two extra transistors MP7 and MP8 are added to turn on the pull-up paths at the falling edges of the inputs. Comparing the operating waveforms in Figures 4 and 7, explains the role of the two extra transistors. Without MP7 and MP8, the half-charged node *T*1 pulls node *U*1 high at the falling edge of the inputs and causes an undesired transition at the output. The added MP7 and MP8 pull *T*1 to high immediately at the falling edges of the inputs and prevent the output from erroneously changing states. Note that MP7 and MP8 do not affect the function of the delay cells because the delay cells are mainly designed to delay the rising edges of the input, where the phase relationship is compared with, whereas the two added transistors are used to remove the delay at the falling edges of the input, where the partially charged nodes could cause problem.

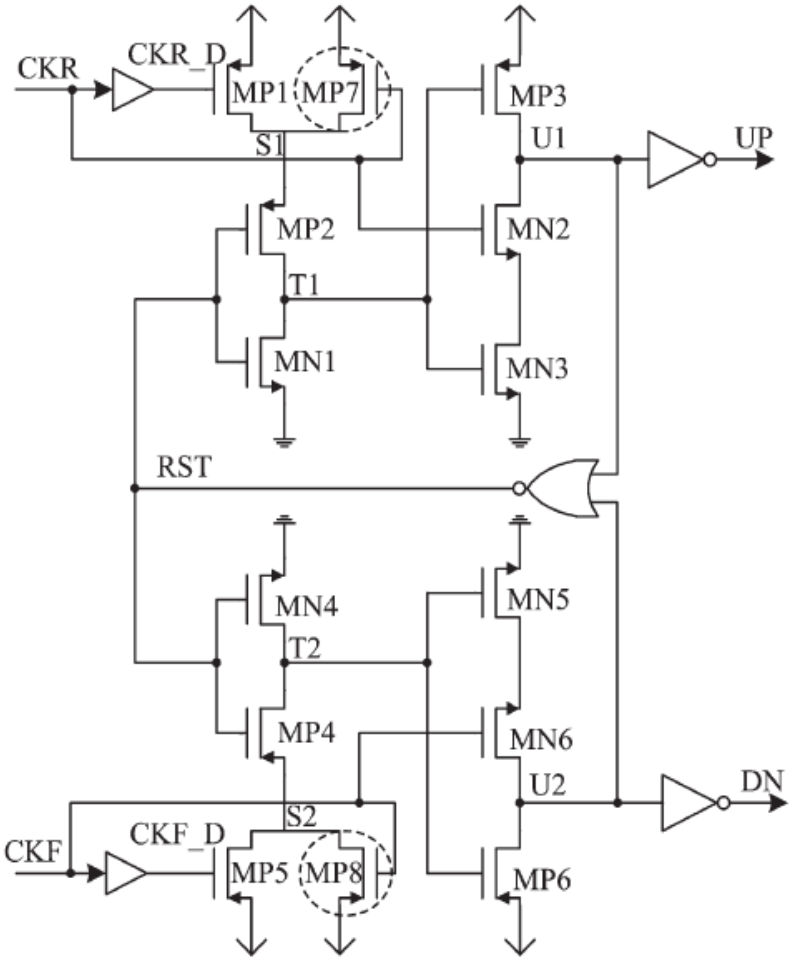

Figure 6. Enhanced PFD

4. Simulations and Results

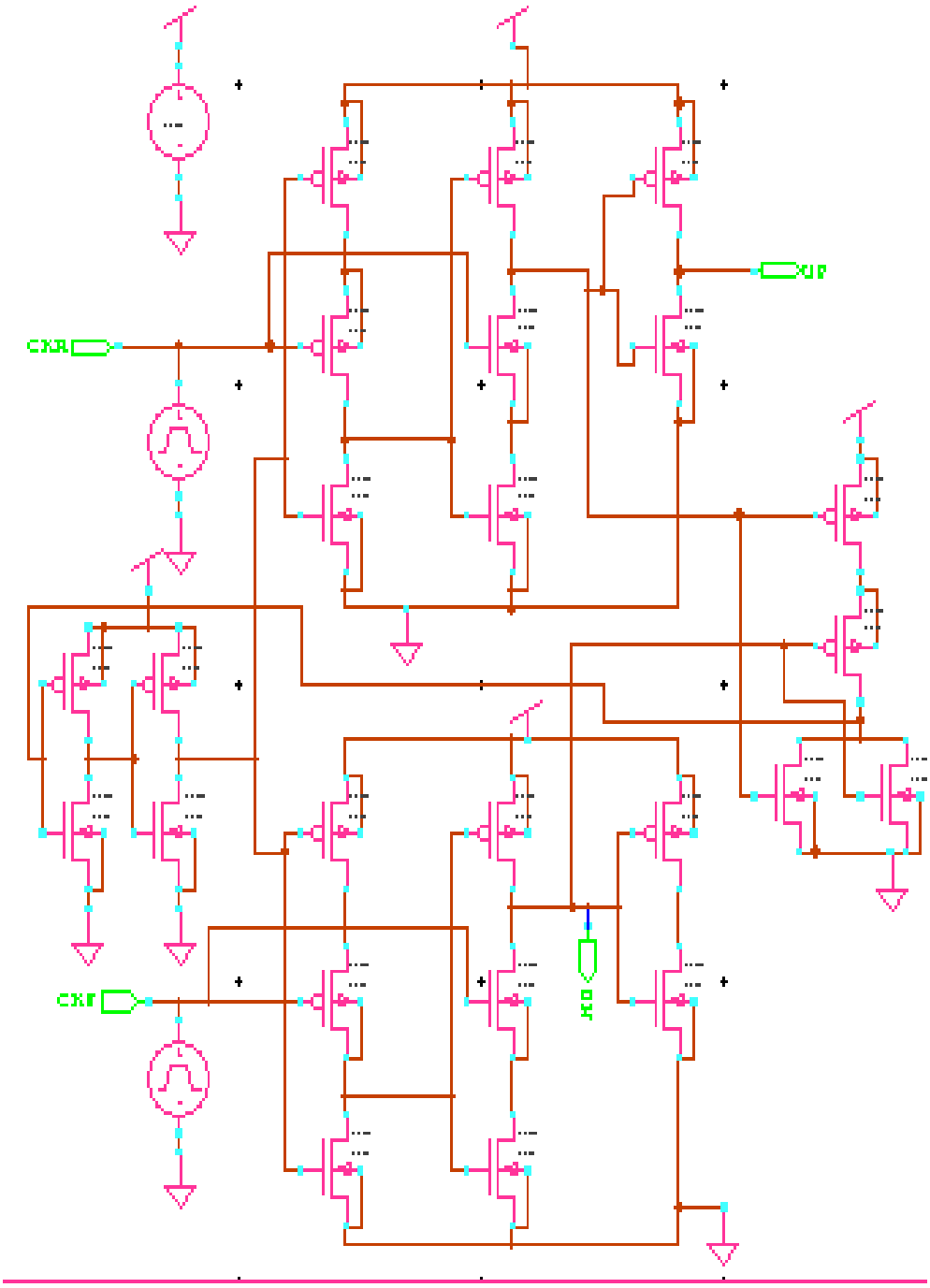

Figure 7. Implementation of Conventional PFD

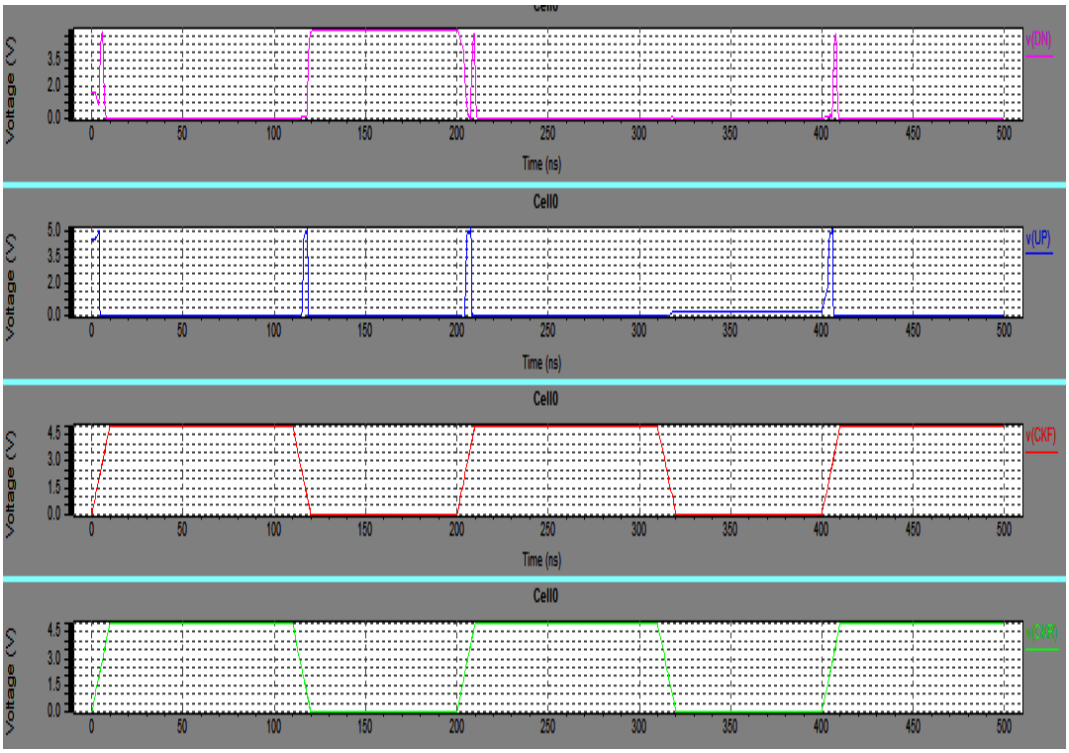

Figure 8. Simulated Waveform of PFD When Inputs are Locked

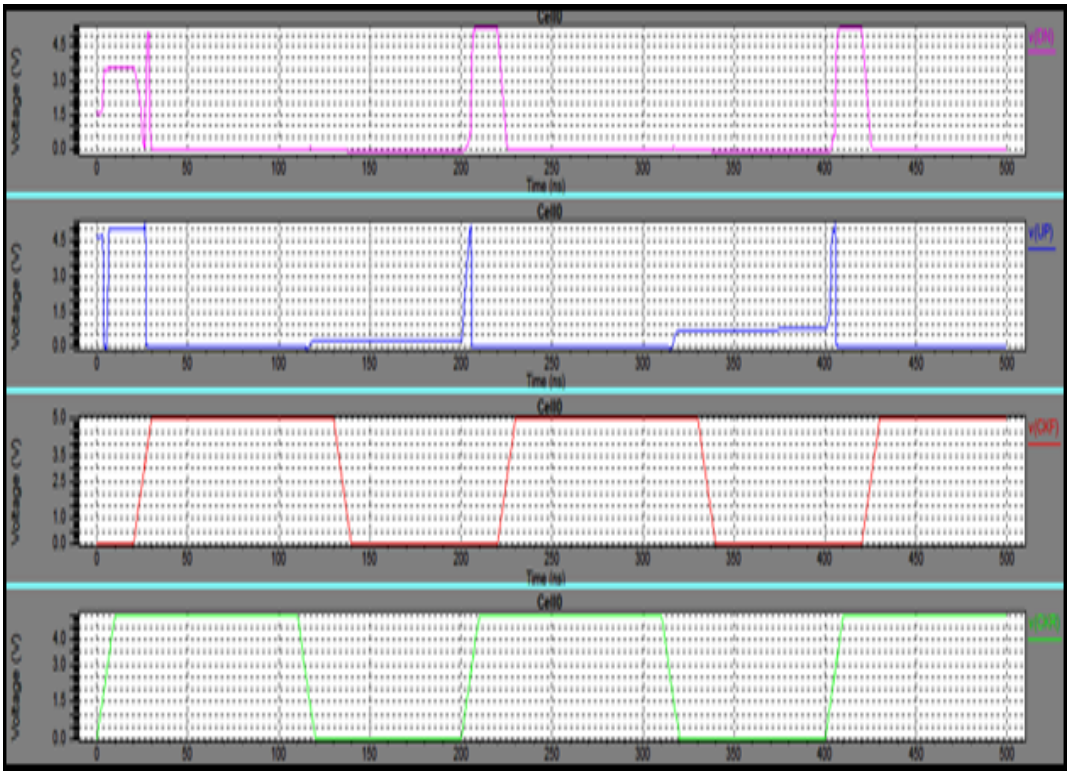

Figure 9. Simulated Waveform of Phase Frequency Detector When Input CKR(Clock Reference is Leading)

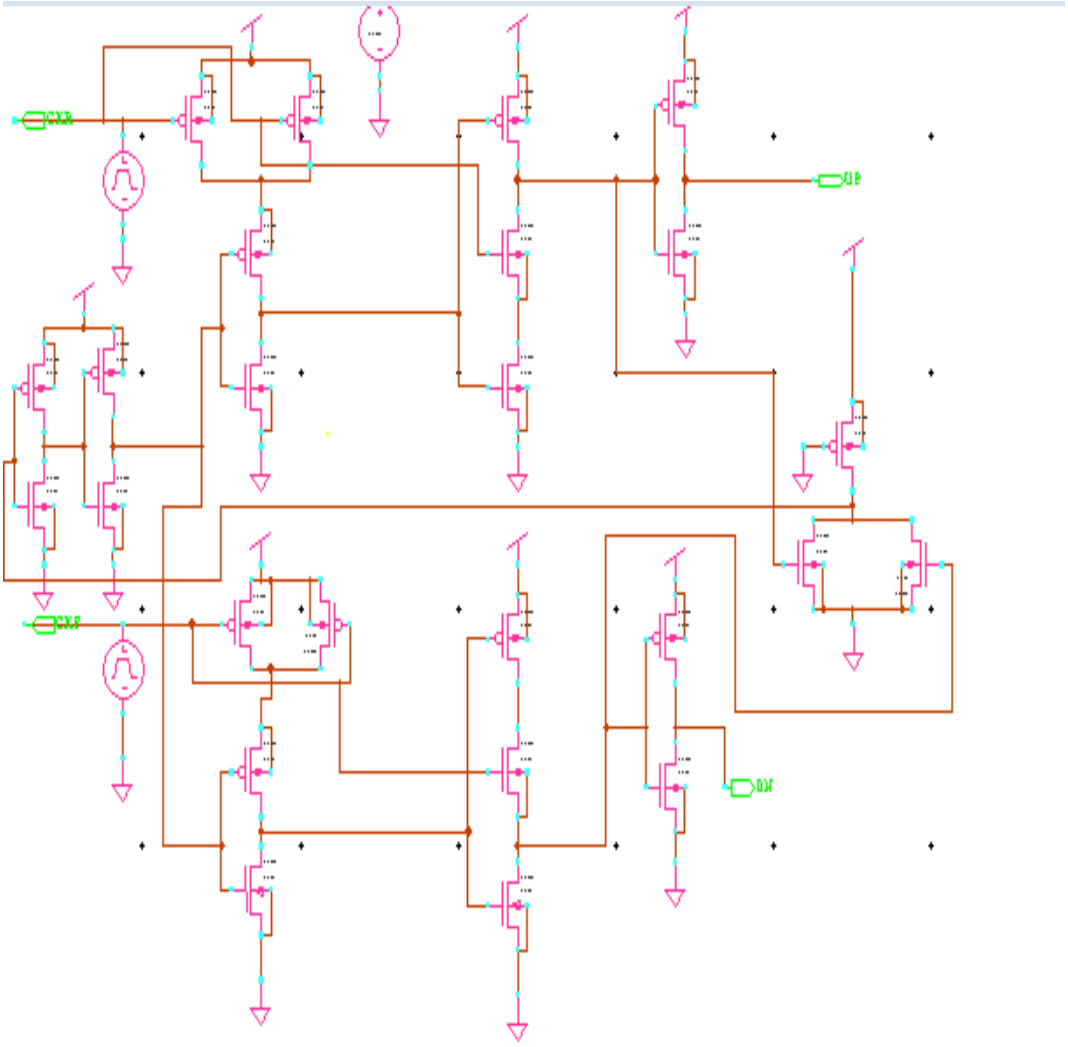

Figure 10. Implementation of Enhanced PFD

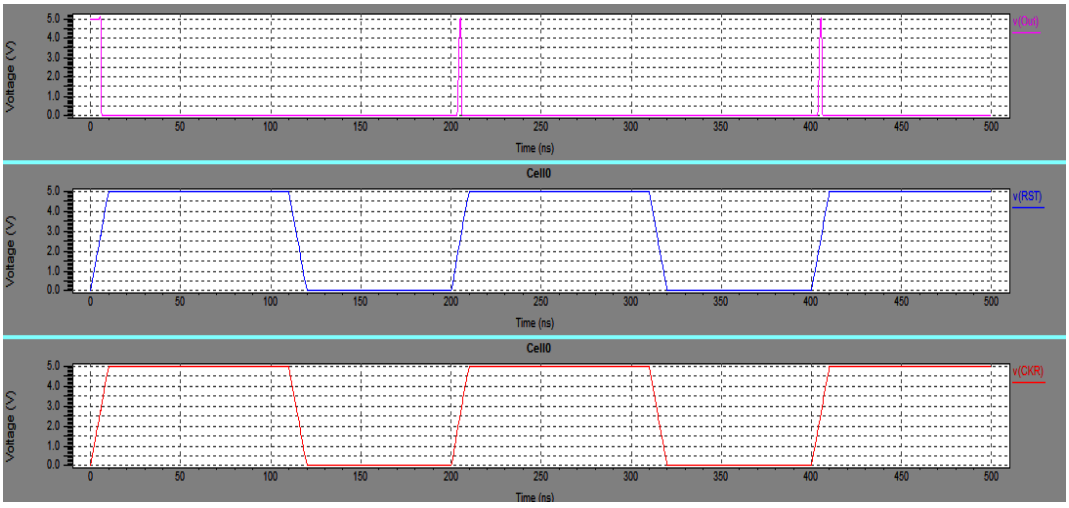

Figure 11. Simulated Waveform of Enhanced PFD When Inputs are Locked

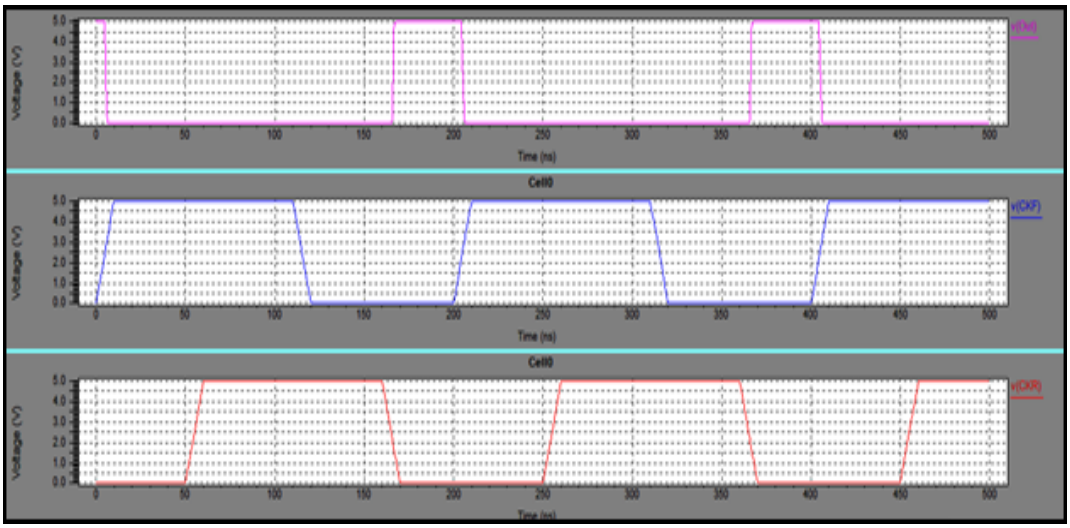

Figure 12. Simulated Waveform of Enhanced PFD When Input CKR (Clock Reference is Leading)

The simulations mentioned above were done using Tanner tools 14 version. With the help of S-EDIT, W-EDIT, L-EDIT net list was generated and SPICE commands were used to obtain various parameter. Results of conventional and enhanced PFD is then compared and it is found that delay parameter of the Enhanced PFD is reduced to 1.8996 ns which was 2.4372ns for conventional PFD.

Parameters	Conventional PFD	Enhanced PFD
Technology	350nm	350nm
V_{dd}	3.5V	3.5V
Power Dissipation	1.428458µW	1.159374µW
Delay	2.4372nsec	1.8996nsec
Dead zone	Zero	Zero

4. Conclusion

From the above results we can conclude that the proposed model is more power efficient and having less delay between the input and output, when it was compared with Conventional PFD. Power dissipation is reduced to approx 1.15µW from 1.42µW which can considered as an advantage in microwave applications and sensors. Paper is also emphasized on reducing delay which is minimized from 2.43nsec to 1.89nsec.Reduced delay will lead to fast switching response of the device and hence we can conclude that this device is suitable for modern technology systems.

We have done device analysis on various technologies and choosing the best results we kept the technology to be 350nm.

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