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Design and Implementation of a High-frequency Signal Generator using the DDS Mixing Principle

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Abstract

Signal generator is a kind of electronic devices that generate repeating or non-repeating electronic signals which are generally used in designing, testing and so on. Under a certain reference frequency, it is able to control the output main signal frequency by selecting the suitable mixed signal at the output with bandwidth filter. This paper introduces a design and implementation of a high-frequency signal generator based on the DDS mixing principle. The generator uses the characteristics of D/A convertor as DDS output frequency spectrum. Experiments show that using the bandwidth filter, most of the spurious signals are removed and the main frequency is confined, thus, signal of 101MHz could be achieved significantly. Additionally, it is observed that the Sine wave is finally obtained from the figure and the filter circuit is able to confine the signal bigger than 30dB for the frequency over 101MHz.

Keywords*: Signal Generator; High-frequency; DDS; DSP*

1. Introduction

Signal generator is a kind of electronic devices that generate repeating or non-repeating electronic signals which are generally used in designing, testing, troubleshooting, and repairing electronic or electroacoustic equipment [1]. There are many different types of signal generators analog signal generators, vector signal generators, and logic signal generators [2]. High frequency is a designation for the range of radio frequency electromagnetic waves between 3 and 30 MHz, which are widely used in aviation communication, government time stations, weather stations, amateur radio and citizens band services, among other uses [3]. The high frequency signal generator is very important since it could be used for testing some advanced equipment and carrying out teaching & learning activities in college or universities.

Direct digital synthesis (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock, which could be used for signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop [4-6]. While in the real application, if the high frequency is synthesized with the 100MHz, the clock of the DDS should be higher than 250MHz. Then the cost is high. Since the output frequency of DDS includes rich sub-frequency, except the components of the spurious frequency, various mixed signals are existing. The mixed frequency of main signal and reference clock signal is $f = nf_r \pm f_0$, where f_0 is the main signal frequency and f_r is the reference clock frequency. When n is the integer bigger than zero, the frequency from the equation is the mixed signal frequency. In order to reduce the cost, it is possible to use the simple principle to generate a high frequency source.

Under a certain reference frequency, it is able to control the output main signal frequency. By selecting the suitable mixed signal at the output with bandwidth filter, the signal could be amplified, then the outputted signal with higher frequency

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could be obtained. In real-life application, AD9850 is widely used and it is a programmable chip that has 40 bit control character [7]. The frequency control character with 32 bit can realize the output frequency accuracy of 0.029Hz when the input reference frequency of 125MHz [8]. The relationship between output sine wave's frequency and control character is $f_o = (\Delta Phase \times f_c)/2^{32}$, where $\Delta Phase$ is the value of frequency control character with 32 bit; f_c is the output reference frequency; f_o is the output basic wave frequency. Thus, it is possible for the applications that the AD9850 could be used for design and develop the signal generator to capture and collect the data [9-11]. When the voltage is 5V, the maximum input reference frequency of this chip is 125MHz. It could be observed that the output sine wave frequency can reach the maximum value 62.5MHz.

According to the analysis above, we can use the output reference frequency of main signal whose frequency is 21MHz obtained from AD9850 with 80MHz. Then, the bandwidth filter with central frequency of 101MHz could be used for removing the primary signal with 21MHz and other spurious frequency. Finally, the 101MHz signal will be obtained. This paper introduces a design and implementation of a high-frequency signal generator using the DDS mixing principle. Such signal generator is based on the series of several bandwidth filter in low power amplification operation so as to get better signal curbing ratio.

The rest of this paper is organized as follows. Section 2 reports on a high-frequency signal source based on the DDS AD9850. Section 3 illustrates the bandwidth filter in terms of the design considerations and circuit implementation. Section 4 demonstrates the program from the DSP F2812. Section 5 presents the experiments and discussions. Conclusions and future research directions are finally concluded in section 5.

2. High-frequency Signal Generator

The high-frequency signal generator is based on several main components. Figure 1 shows the architecture of the high-frequency signal generator (HFSG).

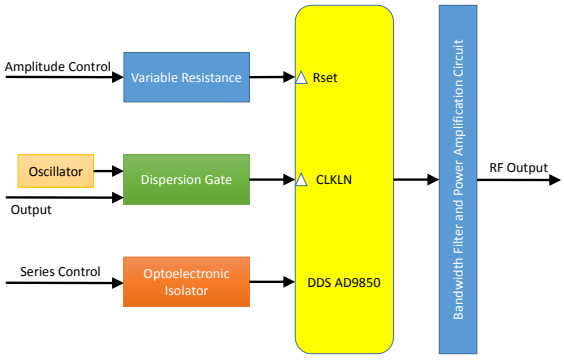


Figure 1. Architecture of HFSG

From Figure 1, in the HFSG, controller manages the DDS AD9850 through series approach. All the series control use optoelectronic isolator since the data is transferred in single direction with high speed. Thus, there is no feedback affect and the anti-disruption is high as the reliability is strong due to the excellent characteristics of optoelectronic isolator [10-12]. Along with the rising edge of W_CLK, a data string from No. 25 pin (D7) is input. After moving 40 bit, a pulse of FQ_UD could update the output frequency and phase. Figure 2 shows the time sequence chart of the series control character.

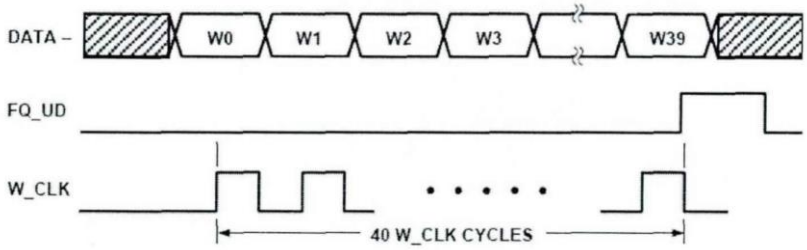


Figure 2. Control Sequence Chart of Series Character

DDS uses the crystal oscillator with temperature compensation to provide the clock signal. External crystal oscillator's output frequency is 80MHz and the frequency stability is ±2ppm. The controller's RF Enable is output through a dispersion gate, which controls the crystal oscillator's clock. When RF Enable is high level, the clock signal from oscillator will be sent to AD9850 [13-15]. When RF Enable is low level, the output will be confined by the dispersion gate. DSS then stops working. When the cyclotron has some emergency, the controller is able to stop the high frequency output so as to protect the whole system. The output current I_o of the DAC in AD9850 is connected to the pin 12 and adjusted by the external resistance R_{set} . The relationship of I_o and R_{set} is: $I_o = 32 \times (1.248V / R_{set})$, where the unit of I_o is A, the unit of R_{set} is Ω, they typical value is 3.9 $k\Omega$.

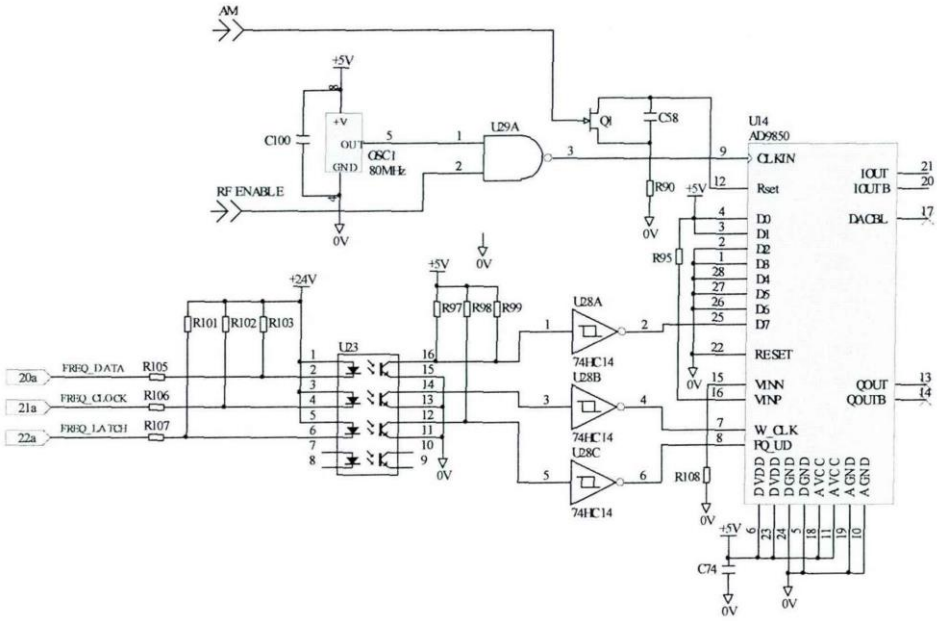


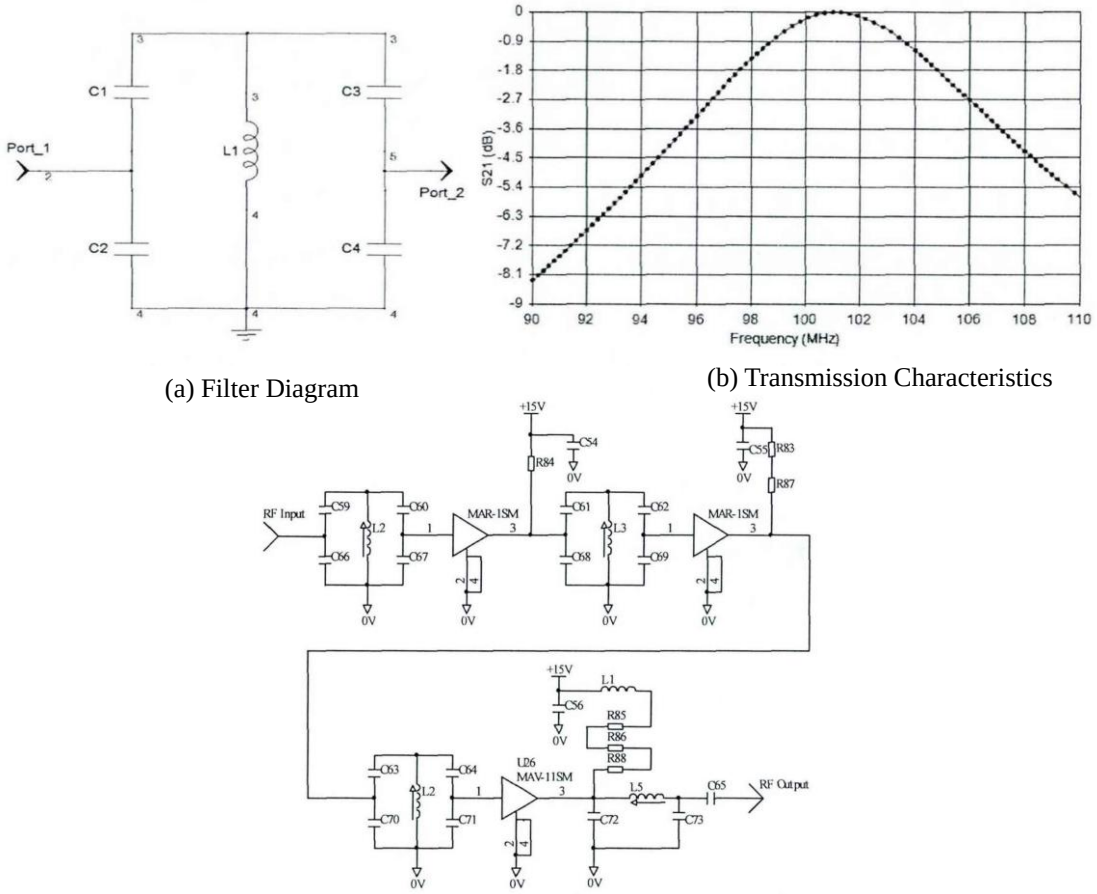
Figure 3. The Circuit of Generator based on AD9850

In the high-frequency signal generator, a voltage controlled rheostat is connected to the pin of R_{set} . An AM from the closed-loop output is used for control the rheostat so as to realize the easy management. The rheostat uses a 2N7000 and a 2.2 $k\Omega$ resistance. AM is connected with 2N7000. Figure 3 shows the designed circuit of the generator based on AD9850.

From the output of AD9850, since the main frequency signal is not the required while the mixed one $f_c + f_o$ is exact the required, the bandwidth filter should be connected to confine the basic wave and other spurious frequency signal.

3. Design and Implementation of the Bandwidth Filter

The central frequency of the bandwidth filter is 101MHz and frequency bandwidth is 10MHz. The bandwidth filter is shown in Figure 4.



(a) Filter Diagram

(b) Transmission Characteristics

(c) Connection of Filter and Amplifier

Figure 4. Bandwidth Filter

Figure 4 (a) shows the diagram of the filter with the parameters are: $C1 = C3 = 22pF$, $C2 = C4 = 68pF$ and $L1 = 72nH$. Figure 4 (b) displays the transmission characteristics of the filter. Figure 4 (c) shows the alternant5 series of the filter and power amplification module. In real circuit testing, the inductance parameter greatly influences the performance of the filter. From the simulation, when the inductance changes based on $L = 72nH$, the central frequency changes 1MHz, the value of inductance changes 1.5nH. Thus, in this design, a changeable inductance with a metal shell and low temperature in a real circuit. In designing the PCB circuit, the impact of lead inductance and distributed capacitance of the spurious parameters. The capacitance encapsulated by the patch and the layout of the circuit should be compacted.

4. Main Programs

After the design of the circuit, the processor is based on TMS320F2812 DSP from TI company's C2000 to carry out the program in AD9580. The external crystal oscillator F2812 with the frequency is 30MHz, which is used for closing the PLL circuit. The I/O E0~E2 of DSP is set as output mode and AD9850 is series loading mode. Under this setting, the control character with 40 bits is sent to AD9850 register through D7, from which the first 32 bits are frequency control character and the rest is 2 bits for controlling the loading mode, 1 bit for power saving mode control, as well as 5 bits for phase control. During the increasing of W_CLK, the control characters are loaded to DDS. When all the control characters (40 bits) are loaded, a positive pulse is given to FQ_UD so as to update the output frequency and phase. When AD9850's reference frequency is 80MHz, the associated frequency control characters is 0x43333333 according to the output main frequency 21MHz. The main programs from DSP F2812 is as follows.

```
#define FREQ_DATA GpioDataRegs.GPEDAT.bit.GPIOE0
#define FREQ_CLOCK GpioDataRegs.GPEDAT.bit.GPIOE1
#define FREQ_LATCH GpioDataRegs.GPEDAT.bit.GPIOE2
Void delay_loop (void);
Main ()
{
    unsigned long keyword1=0x43333333;
    unsigned char keyword2=0x00;
    unsigned int keyword_bit=0;
    FREQ_CLOCK=0;
    FREQ_LATCH=0;
    delay_loop ();
    FREQ_CLOCK=1;
    delay_loop ();
    FREQ_CLOCK=0;
    delay_loop();
    FREQ_LATCH=1;
    delay_loop ();
    FREQ_LATCH=0;
    delay_loop ();
    for (keyword_bit=0;keyword_bit<35;keyword_bit++)
        {
            if (keyword_bit<32)
                {
                    if (keyword1&0x00000001) FREQ_DATA=1;
                    else FREQ_DATA=0;
                    keyword1=keyword1>>1;
```

```
                        }
                else {FREQ_DATA=0;}
        delay_loop ();
        FREQ_CLOCK=1;
        delay_loop ();
        FREQ_CLOCK=0;
        }
FREQ_LATCH=1;
delay_loop ();
delay_loop ();
FREQ_LATCH=0;
keyword1=0x43333333;
FREQ_CLOCK=0;
FREQ_LATCH=0;
delay_loop ();
for (keyword_bit=0;keyword_bit<40;keyword_bit++)
{
        if (keyword_bit<32)
        {
                if (keyword1&0x00000001) FREQ_DATA=1;
                else FREQ_DATA=0;
                keyword1=keyword>>1;
        }
        else
        {
                if (keyword2&1) FREQ_DATA=1;
                else FREQ_DATA=0;
                keyword2=keyword2>>1;
        }
delay_loop ();
FREQ_CLOCK=1;
delay_loop ();
FREQ_CLOCK=0
}
FREQ_LATCH=1;
delay_loop ();
```



```
        delay_loop ();
        FREQ_LATCH=0;
}
void delay_loop ()
{
        short i=0;
        for (i=0;i<3000;i++) {;}
}
```

5. Experiments and Discussion

In order to test the design of signal generator, experiments are carried out. The DDS output, the output waves from first to third bandwidth filter are shown in Figure 5.

The first wave on the top is the output from AD9850 with the frequency is 21MHz. Since it has large number of spurious signal, the wave is chaotic. The second wave is the output wave from the first bandwidth filter. And the third and fourth waves are from the second and third bandwidth filter. It could be observed that using the bandwidth filter, most of the spurious signals are removed and the main frequency is confined. The signal of 101MHz could be achieved significantly.

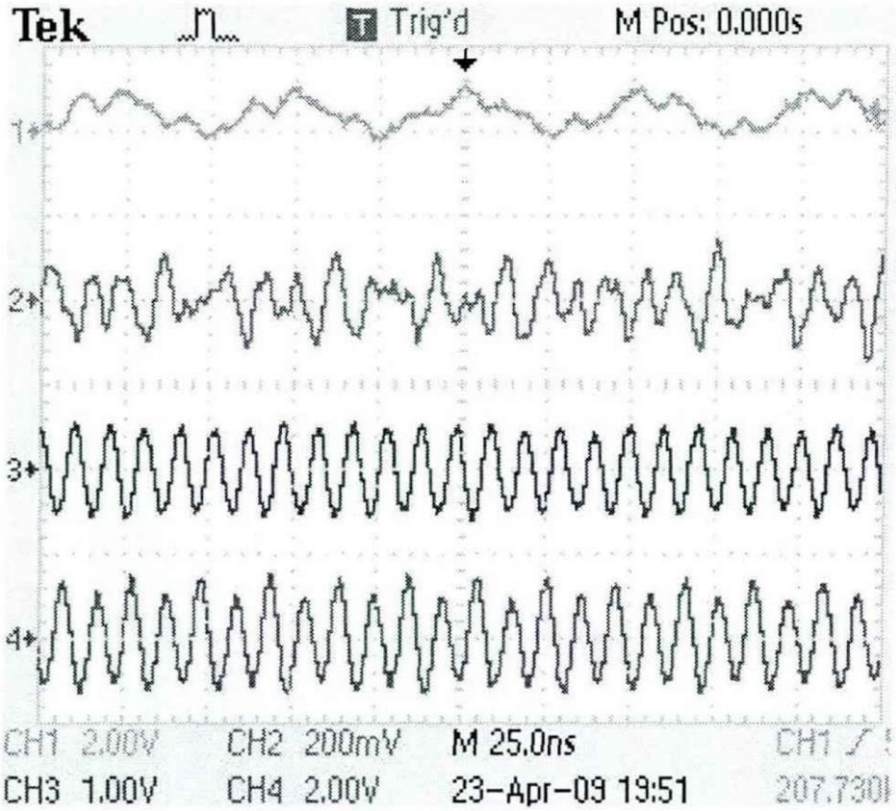


Figure 5. Output Waves from DDS and Filters

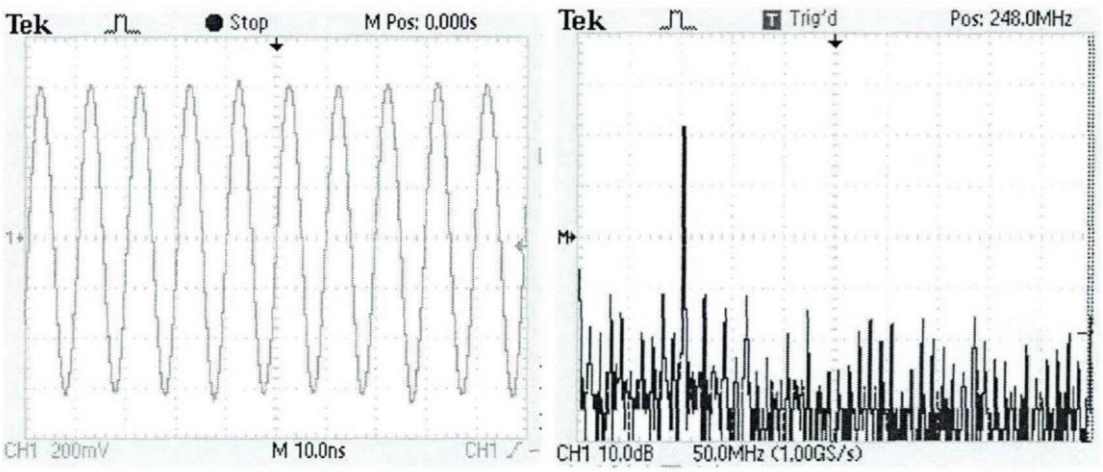


Figure 6. FFT Frequency Spectrum and Output Waves from Generator

After the third bandwidth filter, MAV-11SM is used for amplifying the power. When the frequency $f = 100MHz$, the increase will reach 12.7dB. The output power is 17.5dBm under 1dB. The output wave from the high-frequency signal generator and FFT frequency spectrum are shown in Figure 6. It could be observed that the Sine wave is finally obtained from the figure and the filter circuit is able to confine the signal bigger than 30dB for the frequency over 101MHz.

6. Summary

This paper introduces a design and implementation of a high-frequency signal generator based on the DDS mixing principle. The generator uses the characteristics of D/A convertor. The DDS output frequency spectrum is based on the frequency component $f = nf_r \pm f_0$. Using the DDS chip AD9850 as the frequency synthesizer, the output 21MHz main frequency signal is achieved under the 80MHz reference clock. The mixed signal of $f_r - f_0$ is the required 101MHz signal. The output of DDS is connected by several layers of filter with the central frequency is 101MHz, which is able to remove the spurious signal and central signal of 21MHz, outputting the final required signal. In the experiments, three layers bandwidth filter are series connected for enlarging the signal. After then, a lowpass is used for adjusting the sine signal so that an ideal 101MHz signal could be obtained.

Future research will be carried out as follows. Firstly, the control of Rset pin will greatly influence the voltage circuit. How to change the voltage controller so that the DAC electricity from DDS could be supervised will be investigated. Secondly, when two high frequency has the phases of 180^0 differences, the relationship of the differences and output voltage will be interesting that the trends will be linear. How to examine the influence of this trends on the output frequency so that the 101MHz signal could be more reliable could be further studied.

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