Investigations on Z-Source Based Cascaded Five Level Inverter

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Abstract

The Z source inverter is a novel power conversion topology that can buck and boost the given input voltage. Voltage source inverter (VSI) and current source inverter (CSI) have some common problems. The proposed work eliminates the limitations of both voltage source inverter and current source inverter by replacing multilevel inverter. This paper presents the new inverter topology based on combination of Z Source Inverter (ZSI) and Multi Level Inverter (MLI). The Z source inverter employs a unique impedance network to couple the main circuit to the power source. The basic structure includes one DC voltage source, Z network and multilevel inverter. Thus providing unique features that cannot be provided in both traditional voltage source and current source inverter. The cascaded MLI composed of eight switches to generating five voltage levels. The presence of multilevel inverters provide high output voltages with low harmonics without the use of transformers. The Z source concept can be applied to ac-dc, dc-ac, ac-ac and dc-dc power conversions. This work observes the rms (Root Mean Square) output voltage and presence of THD (Total Harmonic Distortion) in the output waveform by simulating the Z source based multilevel inverter using MATLAB/simulink.

Keywords: ZSI, VSI, CSI, MLI, RMS, THD

1. Introduction

The Z source inverter is used to reduce the line current harmonic, improves the input power factor and to achieve high reliability. The traditional Z source inverter consists of an impedance network having two split inductors L_1 and L_2 and capacitors C_1 and C_2. The main circuit is coupled with the DC source using impedance network in Z source inverter. The DC voltage source can be a battery, diode rectifier, fuel cell and capacitor. Both the voltage source and current source inverter have the common problems. They are either buck or boost the given voltage and they are affected by Electromagnetic interference (EMI). In additional the main circuits of both VSI and CSI cannot be interchangeable. To eliminate the above problems Z source inverter is implemented in this paper. The reliability of ZSI is much higher than the traditional inverter reliability. Multilevel inverters are composed of a number of power electronics switching devices and DC voltage sources. Multilevel inverters increase the voltage levels in the output, provide higher quality of power in its output and reduce the harmonic contents.

Dong Cao *et. al.,* in [1] familiarize the low cost semi-Z-source inverter for single phase photovoltaic system. Different from traditional Z source inverter with an extra shoot through state two achieve the boost function, the two switches of semi Z source inverter are controlled. Input DC source and output Alternative Current (AC) voltage share the common ground to eliminate the leakage current caused by (PV) Photo Voltaic panel.

Banaei *et. al.,* in [2] proposed about Z source based multilevel inverter. The basic unit based on cascaded units and H bridge unit. A Dynamic voltage restorer (DVR) is controlled voltage injected between the supply voltage and load. In this paper modeling and simulation of a DVR with novel multilevel based Z source inverter have been

presented. F.X.Edwin Deepak in [3] analyzed the performance of cascaded H Bridge multilevel inverter based on multicarrier PWM techniques. This paper has investigated a Z source cascaded multilevel inverter which gives a higher output voltage and Boost operation is achieved by shoot through state. From the results maximum boost control method is the most suited control. Ganesh Pashikanti *et. al.,* in [4] designed a closed loop Control system using PI controller in order to maintain load voltage constant for under voltage and Over voltage conditions. The triggering pulses to Cascaded H-Bridge (CHB) MLI is given using multi carrier phase shifted technique and MATLAB simulations have been carried out. Mohit Tyagi *et. al.,* in [5] described about the Z source is a novel power conversion topology that can buck and boost the given input voltage using passive components. In this paper MATLAB/SIMULINK model of a Z source inverter has been developed and harmonic analysis is carried out. That has a wide range of obtainable value at different pulse width.

Sangeetha DebBarman *et. al.,* in [6] proposed different types of PWM techniques analysis for Z source inverter. This paper proposed a Simple Boost Control (SBC) and Maximum Bosst Control (MBC) as well as its implementation with third harmonic and triplen harmonic injection. Simulation results showed the MBC technique with triplen harmonic injection is better than other. Vinayaka B.C *et. al.,* in [7] designed a five level cascaded H Bridge multilevel inverter with DC/DC boost converter. From the simulation results overall efficiency of the developed inverter is 95%. The developed topology in this paper is well suited for industrial drive applications. R.shalchi Alishah *et. al.,* in [8] developed a new structure for multilevel inverter with reduced number of IGBTs and gate drivers, anti parallel diodes was presented. Fundamental frequency switching method was applied to the new topology for controlling the output voltage. Ramalingam SEYEZHAI in [9] proposed a phase shifted sinusoidal pulse width modulation with simple boost control, maximum boost control and constant boost control. Fengjiang et al in [10] considered about calculation of switching loss and also current total harmonic distortion of cascaded multilevel inverter. An European efficiency enhancement scheme with adjusting carrier frequency in real time is proposed. Different from the exiting efficiency improvement schemes, the aim of this paper is the issue of European efficiency enhancement.

C.R.Balamurugan *e.t al.,* in [11] designed a single phase symmetrical multilevel inverter for various loads. This proposed topology has less number of switches than the conventional one. Totally four switches reduced from the conventional one. It is designed to produce a seven level output. In this paper simulation results of single phase seven level cascaded multilevel inverter with R load, RL load and Induction motor load are analysed. Sarala in [12] detailed about improved Z source inverter fed induction motor for wind applications. The operating modes of Z source induction motor is studied using this paper. Mahmoudi *et. al.,* in [13] schemed about control of a filter less Z source inverter. This Z source inverter does not require filter at the output side to generate smooth AC voltage. It also provides control strategy based on the concept of Model Predictive Control (MPC).This system can generate various range of frequency voltages. The inverter has fast dynamic response when operated by MPC method. Malathy and Ramaprabha in [14] designed about new single phase multilevel inverter with less number of switches. The proposed topology in this paper utilizes lesser number of components to generate specific number of output voltage. In addition seven number of scheme is used to determine the amplitude of DC sources is proposed to generate all the voltage levels avoiding redundant switching states. Mahmooda Mubeen in [15] proposed hardware of a basic Z-source inverter which demonstrates the boosting capability. In this circuit a three-phase induction motor of fractional hp is connected as a load and with the help of a toggle switch the boosting up of voltage is observed. Thus the

designed circuits are working satisfactorily and are delivering the required performance.

2. Z - Source Inverter

The Z-Source Inverter is a buck–boost inverter. Z source inverters are used to overcome the limitations of conventional voltage source and current source inverters. Figure 1, represents the conventional Z source inverter. In this figure an impedance network having two capacitors and two inductors, which are arranged in X shape. Six switches are used in main circuit. Each switch composed by a power transistor and an anti parallel diode to provide bi-directional current flow and voltage blocking capability.
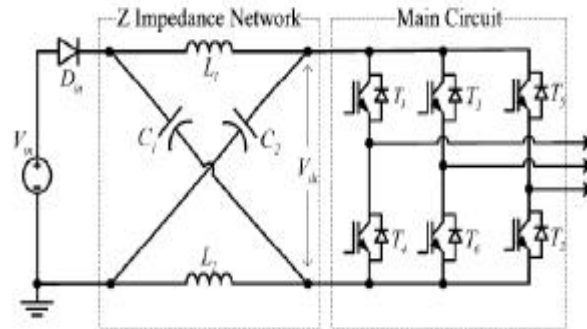

Figure 1. Conventional Z-Source Inverter

2.1. Shoot Through State

Figure 2, shows the shoot through state of the conventional Z source inverter. In three phase ZSI has nine switching states unlike three phase VSI that has eight. ZSI has one extra zero state when the load terminals are shorted through both the upper and lower devices of any one phase leg, any two phase leg or all three phase leg.
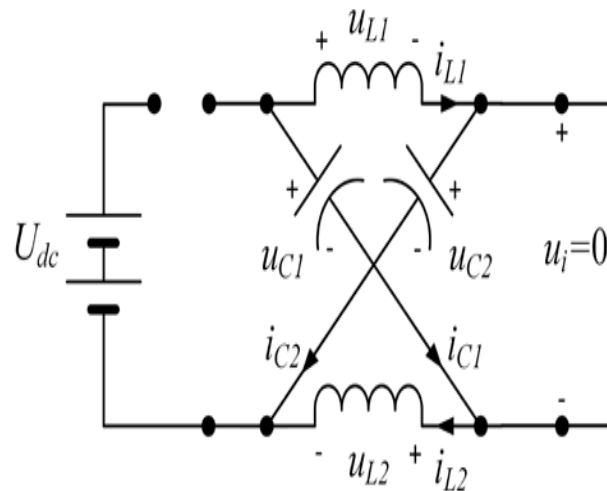

Figure 2. Shoot Through State

During this state, the diode connected in series with the DC source is reverse biased and disconnect the supply from the impedance network. So the inverter DC side voltage is zero.

2.2. Non -Shoot Through State

Figure 3, displays Non-shoot through state of the conventional Z source inverter. During this state the diode is forward biased and the impedance network is connected with the DC source. The capacitors in the impedance network are being charged and the inductors act as an additional current source. So the inverter side voltage is boosted.

$$i_{C1}=C_1 du_{c1}/dt \qquad (1)$$

$$u_{L2}=L_2 di_{L2}/dt \qquad (2)$$

i_{C1} - Capacitor current
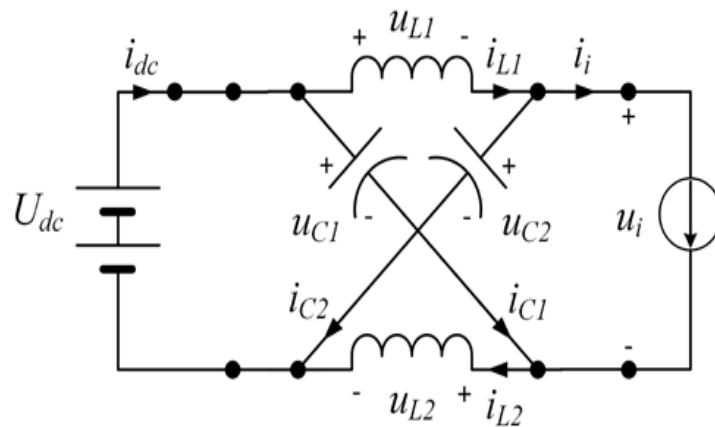u_{L2} – Inductor voltage

Figure 3. Non Shoot Through State

3. Multilevel Inverter

The function of a MLI is to synthesize a desired AC output voltage from several DC voltage sources with low distortion. The main feature of a MLI is its ability to reduce the voltage stress on each power device due to the utilization of multiple DC sources. Multilevel inverter has the advantages like reduced switching frequency, reduced dv/dt, and reduced electromagnetic interference.

Figure 4, Showing the cascaded multilevel inverter. The cascaded MLI can be used as compensator in power system because it does not present unbalance problem in DC source. The output voltage is equal to the summation of the output voltages of the respective modules.

$$V_0=V_{11}+V_{12} \qquad (3)$$

V_{11} - output voltage of module 1
V_{12} - output voltage of module 2

Each module has its own DC source and consists of four power devices. Each module can generate three levels of output $+V_{dc}$, 0 and $-V_{dc}$.
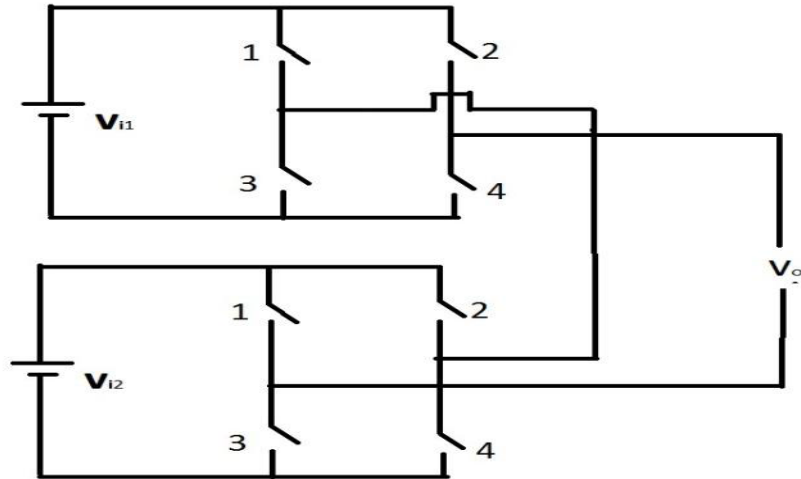
Figure 4. Cascaded Multilevel Inverter

This cascaded configuration formed by cascading more than one H bridge inverter in the series. Its builds required output voltage from various DC sources.

The number of output voltage levels L is defined as N = (2*M+1). M represents the number of DC voltage supply. This multilevel inverter can create an output near sinusoidal waveform. This topology does not require any transformer or clamping diodes or flying capacitors.

Among all types of MLI configurations cascaded MLI is more preferable because it require reduced number of components to obtain the same number of voltage levels among the conventional multilevel inverter.

Table 1, shows the output voltage with the corresponding switching states of upper power devices of two modules of the five level inverter. The voltage across each device is V_{dc}.

Table 1. Switching States and Voltage Levels of Five Level Cascaded Inverter

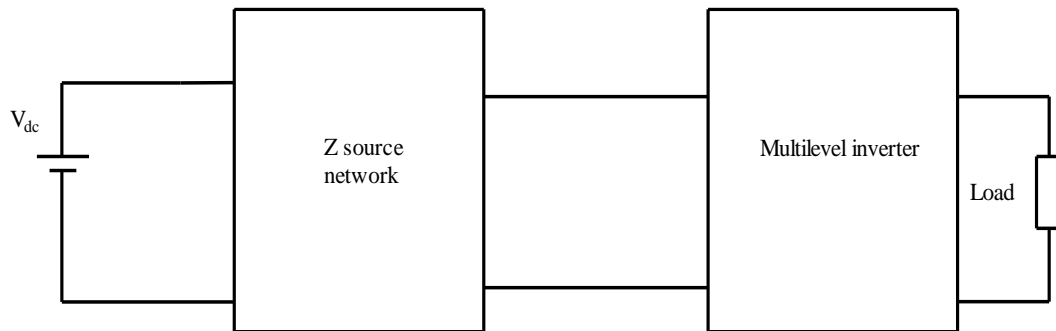| S_{11}	S_{12}	S_{21}	S_{22}	Output(V_0)
1	0	1	0	$+2V_{dc}$
1	0	0	0	$+V_{dc}$
1	0	1	1	$+V_{dc}$
0	1	1	0	$+V_{dc}$
1	0	1	0	$+V_{dc}$
0	1	0	0	0
1	0	1	1	0
1	1	0	1	0
0	0	1	0	0
0	1	1	1	0
1	1	0	0	0
0	1	1	1	$-V_{dc}$
0	1	0	0	$-V_{dc}$
1	1	0	1	$-V_{dc}$
0	0	0	1	$-V_{dc}$
0	1	0	1	$-2V_{dc}$

4. Z source Based Multilevel Inverter

Figure 5. Z Source Based Multilevel Inverter

Figure 5, shows the basic view of Z source based multilevel inverter. The choice of multilevel inverter depends on the applications. Multilevel inverters are well suited for applications induction motor drives, renewable energy, power quality *etc.*

Z source multilevel inverter composed of DC source, Z network and multilevel inverter. Figure 6, displays the power circuit of Z source based multilevel inverter. Voltage stress problem in conventional Z source inverter is overcome by Z source multilevel inverter. Voltage source and current source inverters can either buck or boost the voltage but Z source based multilevel inverter can able to both buck and boost the given voltage.
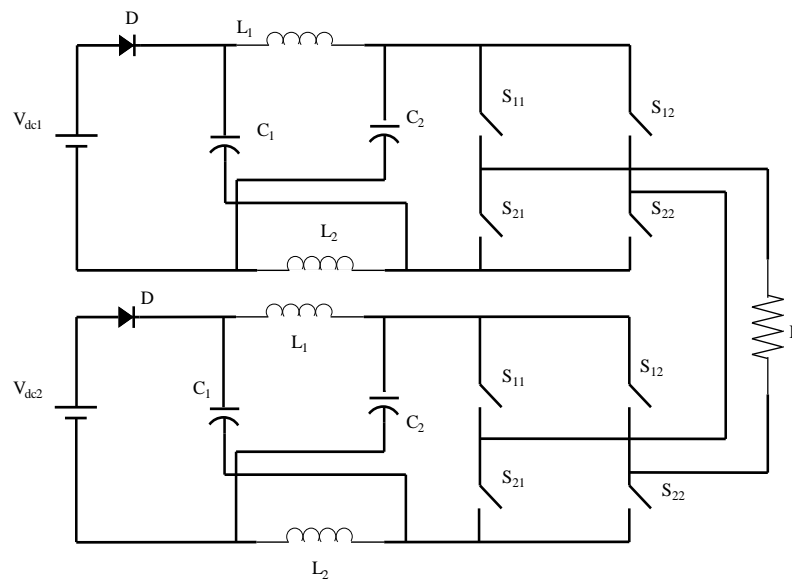

Figure 6. Power Circuit of Z Source Based Multilevel Inverter

The performance of Z source MLI has been analyzed and simulation results are presented using MATLAB/simulink. Presence of RMS voltage and THD in the output waveform is measured for various L and C values by using simulation. In this paper Z source MLI is controlled by sinusoidal, TAR (Trapezoidal Amalgamated reference), THI (Third Harmonic Injection), Step and Trapezoidal references. Variation of RMS output voltage and THD in the output voltage is observed for various modulation indices. The modulation index controls the output voltage. The variation of modulation index from 0 to 1 varies the RMS output voltage.

Table 2. Chosen L and C Values

S.No	Inductance(H)	Capacitance(F)
1	3mH	4700µF
2	3mH	470µF
3	160 µH	1000 µF
4	250 µH	500µF

5. Modulation Strategies for MLI

There are many control methods employed for multilevel inverter. For controlling the output voltage, one of the methods is sinusoidal pulse width modulation method. In this method of modulation, several pulses per half cycle are used as in case of multiple pulse width modulation. Instead of maintaining the width of all pulses same as in the case of multiple pulse modulation, the width of each pulse is varied proportional to the amplitude of a sine wave. By comparing a sinusoidal reference signal with a carrier wave of frequency, the gating signals are generated. The area of each pulse corresponds approximately to the area under the sine wave between the adjacent midpoints of off periods on the gating signals. These strategies have more than one carrier option that can be triangular, inverted sine, saw tooth, *etc.* Different types of references are taken for modulation strategies of MLI such as sinusoidal, Third Harmonic Injection (THI), TAR, Trapezoidal and stepped wave reference. Different types of multicarrier PWM methods are phase disposition (PD), phase opposition and disposition (POD), Alternative phase disposition and opposition (APOD).

In PDPWM strategy, all the carrier waves have same amplitude, frequency and phase. Since all carriers are selected with same phase. All carriers are having amplitude as 1. PODPWM method is same as PDPWM but carrier arrangement should be different. The carriers are equally divided into two groups based on positive/negative average levels. In this type the two groups are opposite in phase with each other while keeping in phase within the group. APODPWM method also same as PDPWM but one of the main different in APODPWM by comparing to PDPWM is that the alternate carriers are phase shifted by 180 degree with each other.

In this paper phase disposition PWM technique is implemented using different types of references such as sinusoidal reference, TAR reference, THI reference, stepped reference and trapezoidal reference. This process present the triangular carriers above zero level and below zero level are in phase. The formula described can be also used for PWM strategies such as PD, POD and APOD.

Modulation index of frequency

$$M_f = \quad f_c/f_m \tag{4}$$

f_c - Carrier signal frequency
f_m - Reference signal frequency
Modulation index of amplitude

$$M_a = 2A_m/(N-1)A_c \tag{5}$$

A_c - Carrier signal amplitude
A_m - Reference signal amplitude

6. Simulation Results

The present works simulate the Z source MLI with filter using MATLAB/simulink. The Z source MLI simulated by sinusoidal, THI, TAR, Trapezoidal and stepped

references. The Power circuit of Z source based MLI consist of R load with resistance of 10Ω. The source voltage considered as 100V for each module. The present LC filter has the values 160µH and 1000µF.Increase in modulation index from 0 to 1 increase the peak value of output voltage.

Figure 7-11, Showing the carrier arrangement with various references such as sine, THI, Trapezoidal, TAR and step. For example output voltage across multilevel inverter for sine, stepped and trapezoidal reference is displayed in the Figures 12, 13, and 14.
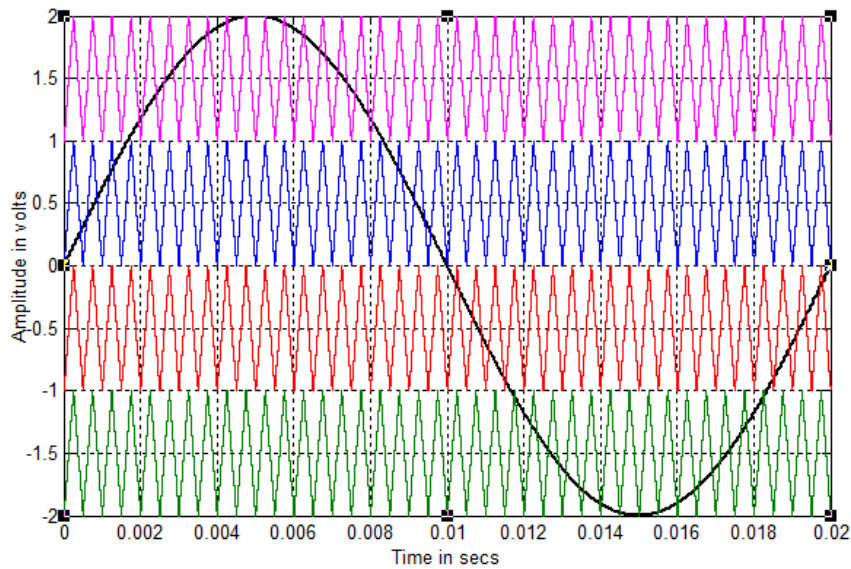

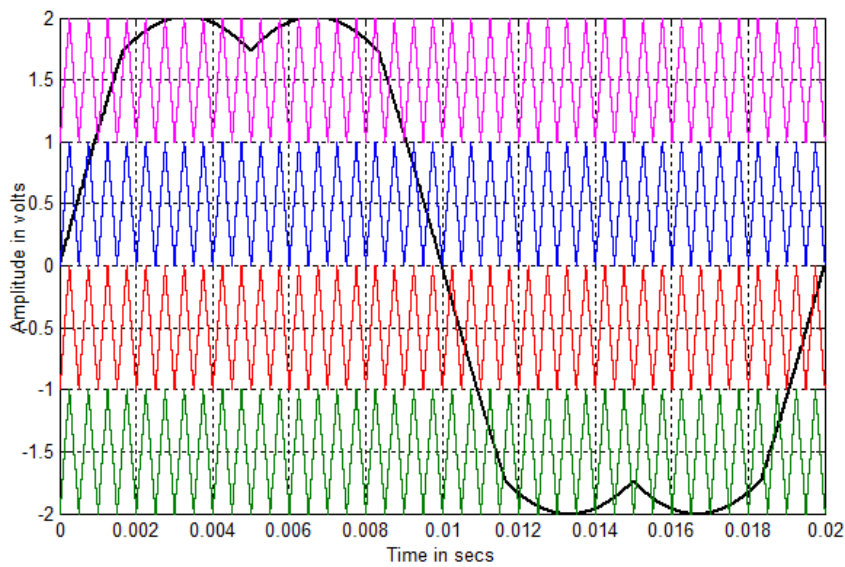**Figure 7. Carrier Arrangement with Sine Reference**
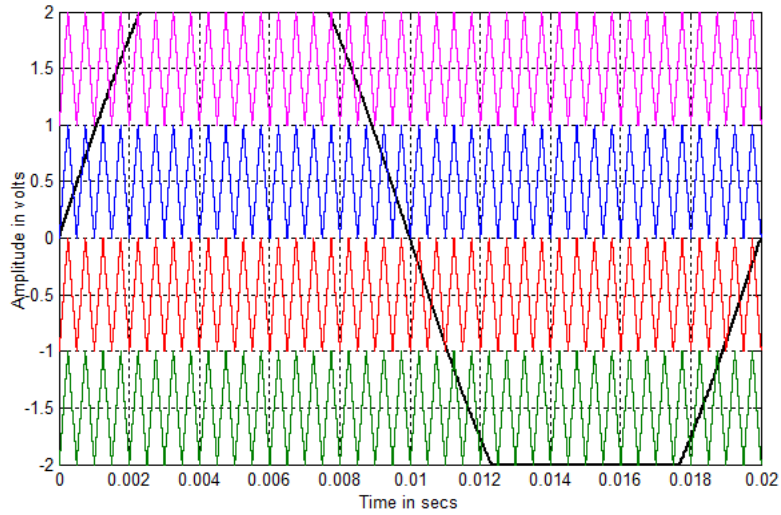

Figure 8. Carrier Arrangement with THI Reference

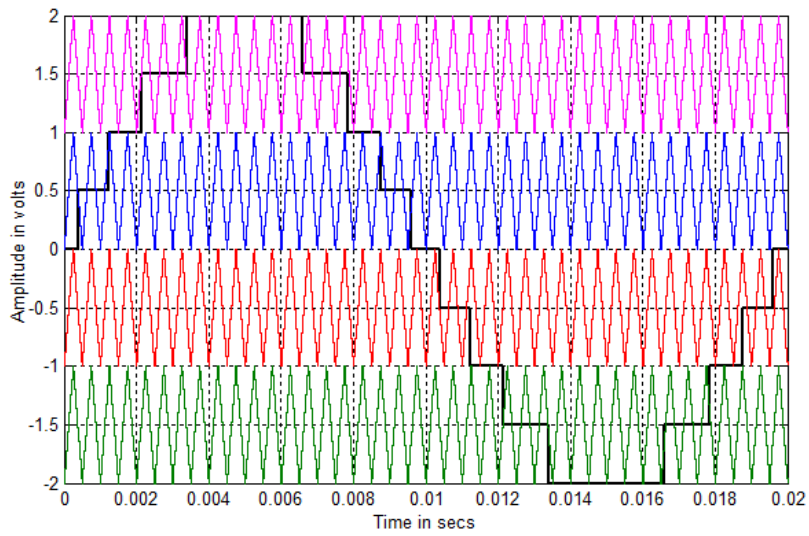**Figure 9. Carrier Arrangement with Trapezoidal Reference**

Figure 10. Carrier Arrangement with Stepped Reference
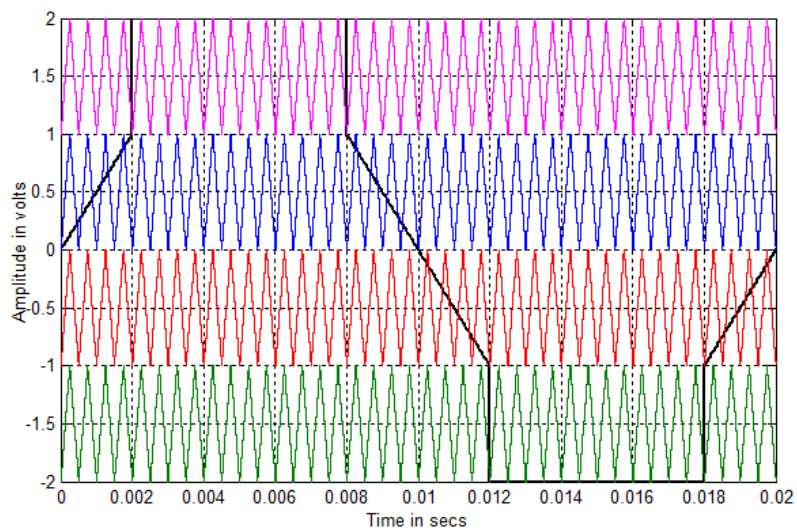

Figure 11. Carrier Arrangement with TAR Reference
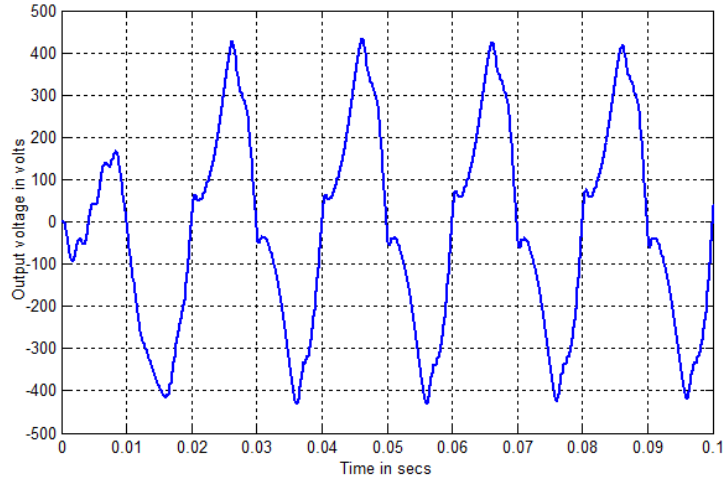
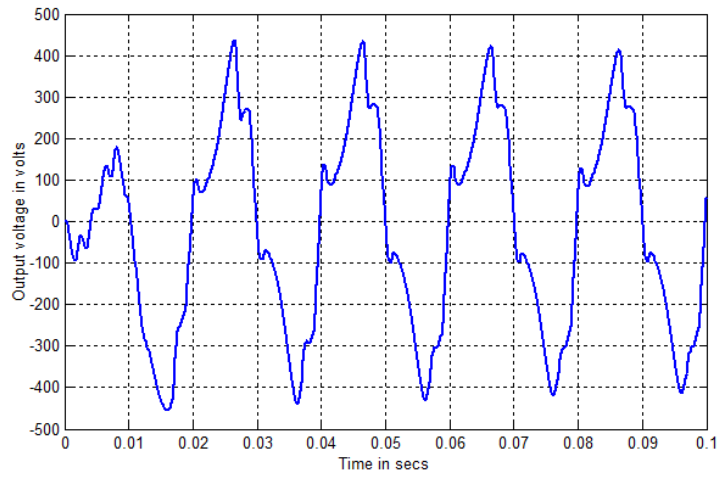**Figure 12. Output Voltage Across Multilevel Inverter (Sine ref.)**

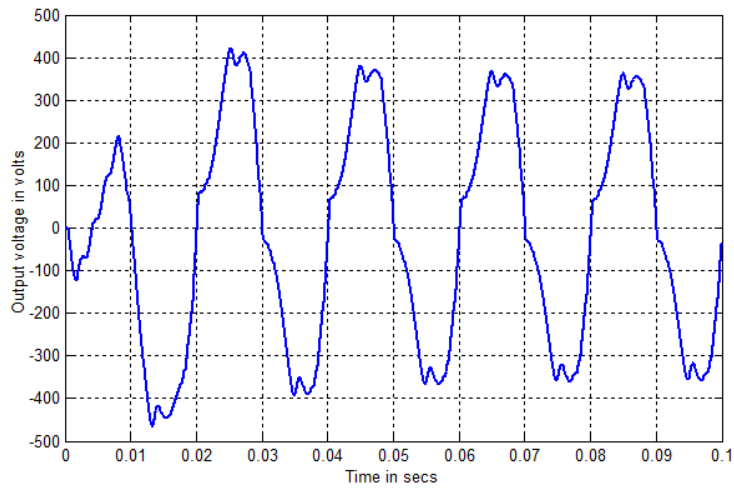**Figure 13. Output Voltage Across Multilevel Inverter (Step ref.)**

Figure 14. Output Voltage Across Multilevel Inverter (Trapezoidal ref.)
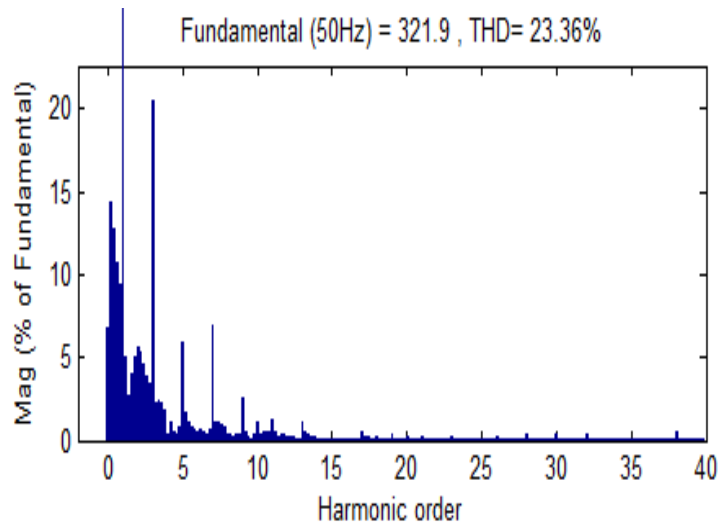
Fundamental (50Hz) = 321.9 , THD= 23.36%

Figure 15. Sample FFT Plot (Sine ref.)

The harmonics present in the inverter system lead to some disadvantages. Presence of harmonics currents will lead to excessive heating. Harmonic current cause losses in the AC system and can even produce resonance in the system. On critical loads, torque pulsation produced by the harmonic current can be harmful. In this paper the amount harmonics present in the waveform is observed by using FFT analysis. The following tables display the RMS output voltage and THD for various reference signals with four types of L and C values. Inductor and capacitor requirement must be smaller than traditional inverter.

Table 3. Measurement Across Multilevel Inverter for L=3mH and 4700μF

m_a	Sine reference		Step		TAR		THI		Trapezoidal	
	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)
1	227.6	23.36	227.1	26.81	262.3	29	242.1	19.30	249.7	16.18
0.	205.4	23.27	209.8	26.61	240.1	31.48	224.5	19.04	231.2	17.14
90	166.4	21.66	171.6	24.87	212.1	33.92	185.8	20.78	202.6	19.65
.8	132.8	18.44	137.7	22.44	150.9	32.66	134.2	22.07	146.9	20.22
0.	123.9	20.40	123.3	22.08	120.1	31.57	125.1	18.54	126.6	17.59
70										
.6										

Table 4. Measurement Across Multilevel Inverter for L=3mH and 470µF

m_a	Sine reference		Step		TAR		THI		Trapezoidal	
	V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)
1	214.7	14.82	204.3	20.36	269.7	15.23	225.9	21.18	228.9	20.28
0.90	199	13.94	198.8	19.01	258.6	16.59	210.5	21.04	216.7	18.42
.8	163.1	13.25	169.1	18.39	239.8	17.91	192.4	20.11	207.1	17.58
0.70	126.5	12.63	125.6	16.39	144.7	18.18	131.2	18.10	139.1	15.79
.6	120.1	15.25	118.9	16.94	115.6	21.09	118.1	13.75	120.5	12.43

Table 5. Measurement Across Multilevel Inverter for L=160µH and 1000µF

m_a	Sine reference		Step		TAR		THI		Trapezoidal	
	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)
1	163.1	8.66	169.1	10.54	190	12.41	181.1	29.24	180.1	22.73
0.90	152.5	8.82	156.2	9.73	178.5	15.50	170.3	27.08	170.8	20.79
.8	139.1	8.27	142.6	8.21	163.4	17.45	157.7	25.85	158.1	20.77
0.70	123.1	7.59	126.7	6.56	142.8	18.19	140.8	25.67	141.7	20.32
.6	101.8	6.64	106.8	6.45	120.9	19.38	118.4	25.86	120.1	19.89

Table 6. Measurement Across Multilevel Inverter for L=250µH and 500µF

m_a	Sine reference		Step		TAR		THI		Trapezoidal	
	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)	V_{rms} (v)	THD (%)
1	163.5	12	168.8	14.63	187.8	8.89	186.7	27.56	181.3	21.59
0.90	153.4	12	156	12.89	181.2	11.58	173.6	27.17	173	21.64
.8	139.5	11.67	143.9	11.92	168.4	13.46	159.2	26.41	159.7	21.81
0.70	122.4	10.29	126.6	9.83	146.1	14.61	140.1	26.36	140.8	21.38
.6	101.5	8.80	106.4	8.35	121	15.46	118	25.82	119.3	20.24

7. Conclusions

This paper has presented an impedance source inverter with multilevel inverter. The Z source network employs an impedance network to couple the main circuit to the power source. The Z source inverter can produce an output voltage that is greater than the ac input voltage by controlling boost factor. The presence of MLI increases the output voltage levels in the output and also reduces the harmonic contents in the output waveform. In this section, simulation is performed for proposed Z source based multilevel inverter using MATLAB. The Z-source network is the energy storage/filtering element for the Z-source inverter.

The Z-source network provides a second-order filter and is more effective to suppress voltage and current ripples. Therefore, the inductor and capacitor requirement should be smaller than the traditional inverters. From this analysis as per voltage concern higher RMS output voltage is achieved by using TAR reference. The presence of THD in the output waveform is reduced up to 6.45% by using Stepped reference for L=160mH and C= 1000μF. In order to obtain a lower amount of DC component THI reference is preferable.

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