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Implementation of Area and Power Efficient Pulse Shaping FIR Interpolation Filter for Multi Standard DUC

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Abstract

The multiplier occupies more area in the design of FIR filter, which is the basic element of any filter. The low complexity and power architecture of pulse shaping FIR filter for multi standard digital up converter was designed. In the existing system, a 2-bit binary common sub expression (BCS) elimination algorithm and shift and add method are used to design an efficient multiplier in the pulse shaping filter. In this paper, two different types of adders are used in accumulation unit of the filter to reduce power consumption and delay compared to the existing system. Adders plays vital role in Digital signal processing applications and also used in the digital integrated circuits. With the advances in technology, several researchers have contributed towards designing adders with either high speed, less power consumption, low area or the combination of them. In this Paper, we describes the analysis of speed, power and delay of two different types of adders like carry select adder and carry save adder for accumulation unit of root raised cosine (RRC) filter. The number of additions are reduced by using these adders and succeeded in reducing the delay, power and area. The designed pulse shaping FIR interpolation filter is simulated and synthesized using Xilinx tool for Spartan 3E family devices and simulation results are presented.

Keywords: *Digital up converter (DUC), Finite Impulse Response (FIR) interpolation filter, Reconfigurable hardware architecture, Software Defined Radio (SDR) system*

1. Introduction

The FIR filters are most widely used in the mobile communication systems for pulse shaping, channel equalization and matched filtering due to their properties of linear phase and stability. The telecommunication industry releases the concept of software defined radio (SDR). SDR refers to a single terminal device that is capable of supporting multiple wireless communication standards [1]. However, different standards have different channel bandwidths, sampling rates and carrier to nose ratios. To meet all these specifications one reconfigurable digital up converter is required for multiple communication standards. Because, using digital up converter for the baseband signal it leads to aliasing effect. Hence some pulse shaping filter is required to shape this baseband signal to reduce aliasing. Among the available pulse shaping filters, root raised cosine filters (RRC) are mostly used because they have high inter symbol interference rejection ratio. To support multiple standards in a single device, a reconfigurable RRC filter is required.

Researchers are trying to design a low power, low area and low complexity reconfigurable channel filter in SDR system. M.Thenmozhi [4], designed the reconfigurable FIR filter architecture with low area and power. Canonical Signed Digit (CSD) based representation of the common sub expression elimination algorithm was used to reduce the number of adders in multipliers. The Constant Shift Method (CSM)

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and Programmable Shift Method (PSM) reconfigurable architectures offer low power and good area improvement in reconfigurable FIR filter architecture implementations.

R.Mahesh [5], reviewed the architecture of FIR filter using Binary based Common Sub expression Elimination Algorithm (BCSE) in place of canonical signed digit (CSD) based common sub expression elimination algorithm. The binary based common sub expression elimination algorithm used for reducing the number of logical operators than the CSD based CSE algorithm. As number of logical operators is reduced, critical path is reduced. So, it produces less delay.

The paper is organized as follows. In Section 2, the details of the RRC filter and BCSE method are reviewed. Section 3 presents our reconfigurable architectures. The simulation results of architectures are presented in Section 4. In Section 5, comparison results of the existing method and proposed method are presented. Finally, this brief is concluded in Section 6.

2. The Reconfigurable Root Raised Cosine FIR Filter

2.1. Issues in Designing the Reconfigurable RRC FIR Filter for Multi Standard DUC

As a design example of multi standard digital up converter, we have considered three standards, namely wide band code division multiple access, mobile telecommunication system, and digital video broadcasting. These three standards have adopted root-raised-cosine (RRC) filter as the pulse shaping filter [14] has ability to reduce inter symbol interference and to generate the excess channel band widths. Efficient hardware implementation of a reconfigurable root raised cosine (RRC) FIR interpolation filter specifications are mentioned below.

1) For a filter of N tap with interpolation factor of R, [N/R] equivalent multipliers (to perform the convolution operation between the filter coefficients and the inputs), and Structural adders (to implement the final addition operation for generating the output) are needed. Design of three different filter lengths of L, M, and N with three different interpolation factors P, Q, R would require L/P+M/Q+N/R number of multipliers and structural adders. Now, if the RRC filter parameters (roll-off factors) are different, the number of multipliers and adders will increase with the number of parameters considered for implementing the filter. For a constant propagation delay, more number of multipliers and adders are used for implementing the higher order filter in single device architecture.
2) Amongst several techniques proposed for implementing an efficient constant multiplier, the binary common sub expression elimination algorithm is the recently proposed popular method. In BCSE method, a coefficient of m-bit word length can form 2m-(m+1) binary common sub expressions amongst themselves. The length of the BCS is an important factor to avoid the extra hardware.
3) In BCSE method [5], the critical path logical depth (LD) mainly depends upon the number of addition operations. Propagation delay of the filter is calculated by required time of (LD+1) additions operations. Proper use of the BCS method reduces the critical path.
4) Constant Multiplications are implemented through shift and add operations. In this, main aim is to reduce the number of adders. By reducing the number of adders the desired filter is implemented.

2.2. The BCSE Method for Solution

The binary common sub expression elimination algorithm consists of the following steps.

1) In the first coding pass block, the two RRC filters with different parameters and same length are passed through one 2:1 multiplexer, where the control parameter selects the desired filter.
2) In the second coding pass block, the output of the FCP block is passed through another multiplexers set. The control parameter selects the desired filter based on the interpolation selection factor [9]. Combination of first coding pass block and second coding pass block reduces the number multiplications per input samples and additions per input samples.
3) In any filter, the multiplication operation is done between the inputs and filter coefficients. Considering the 2-bit BCSE method, the number of logical operators is reduced and hardware is also reduced.

3. Methodology

The reconfigurable architecture of RRC filter is as shown in Figure.1. The reconfigurable RRC filter architecture consists of major blocks. T hey are data generator (DG), a coefficient generator (CG), a coefficient selector (CS) and accumulation unit block. The input signal is sampled based on the interpolation factor. The coefficient generator block generates the multiplication operation between the input and filter coefficients. Coefficient selector sends the proper data to the accumulation unit. Finally, the accumulation unit will add all the outputs of the CS block.

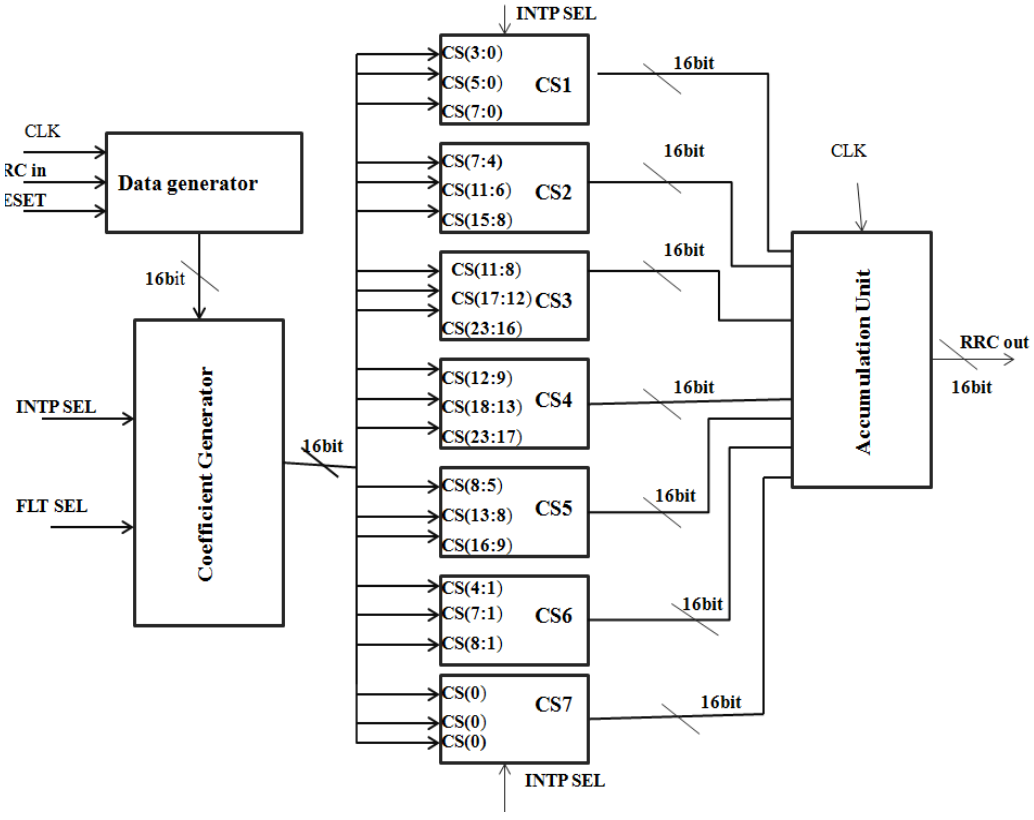

Figure 1. Architecture of RRC Filter

3.1. Data Generator Block

When the clock signal is given to the data generator the input signal is sampled based on the interpolation selection value. The sampled data is given to the coefficient generator as input. From the design point of view, it has been observed that 25-, 37-, and 49-tap

filters with interpolation factors of four, six, and eight constitute a branch filter of seven taps;
25/4 = 37/6 = 49/8 = 7. This indicates that to produce the full filter response, seven sub filters are required for multiplication of the filter coefficients with the input sequence

3.2. Coefficient Generator Block

The coefficient generator block performs the multiplication operation between the input and filter coefficients. The coefficient Generator consists of following blocks. They are First Coding Pass (FCP) block, Second Coding Pass (SCP) block, Partial Product Generator (PPG) block, multiplexer unit and addition unit. Every block in the coefficient generator is implemented using the multiplexer.

3.2.1. First Coding Pass Block: The output of the data generator is given as the input of the first coding pass block. In one FCP block, two sets of 25-, 27-, and 49-tap filter coefficients [13] differing only by roll-off-factor are the inputs. Inside the FCP block, three coding pass (CP) blocks are running in parallel for three different interpolation factors The outputs of the first coding pass block are produced based on selection line value of the multiplexer. The architecture of the first coding pass block is shown in Figure 2.

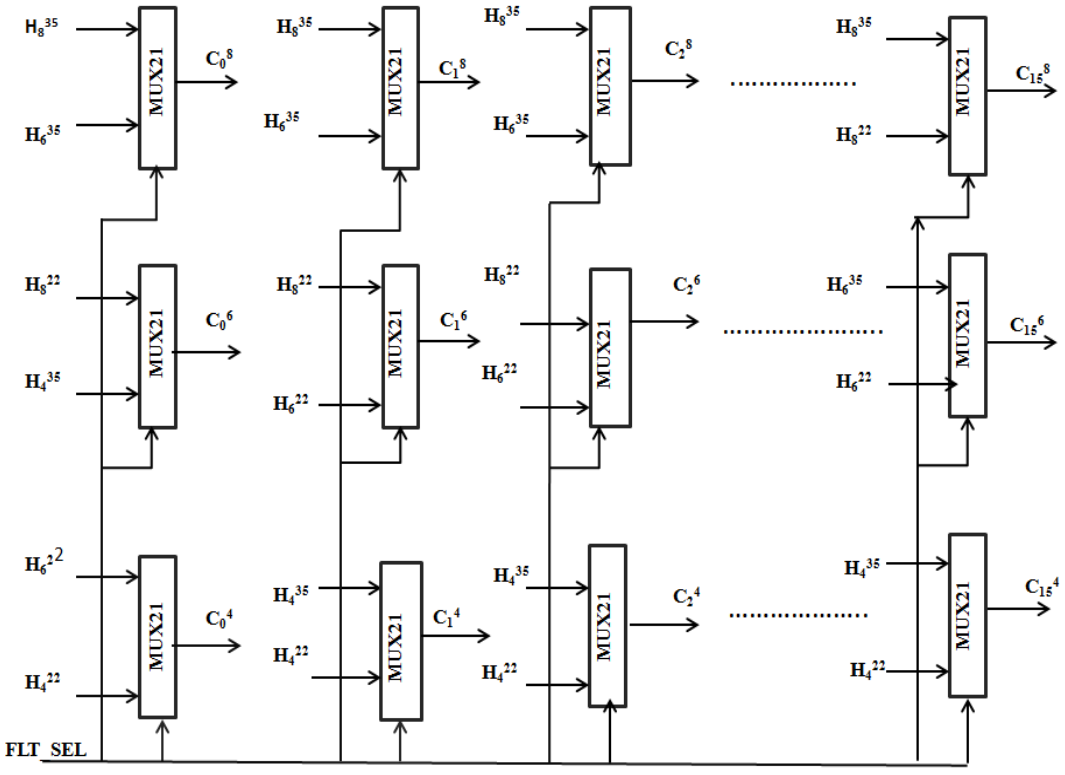

Figure 2. Architecture of FCP Block

3.2.2. Second Coding Pass Block: The operation of the first coding pass block and second coding pass blocks are similar. The output of the first coding pass block is given as the input of the second coding pass block. The outputs from FCP block are three sets of coded coefficients that are 13, 19, and 25 in number and pass through another CP block to get the final coefficient set.The output of the second coding pass block depends on the control parameter of the multiplexer. The architecture of the SCP block is illustrated in Figure 3.

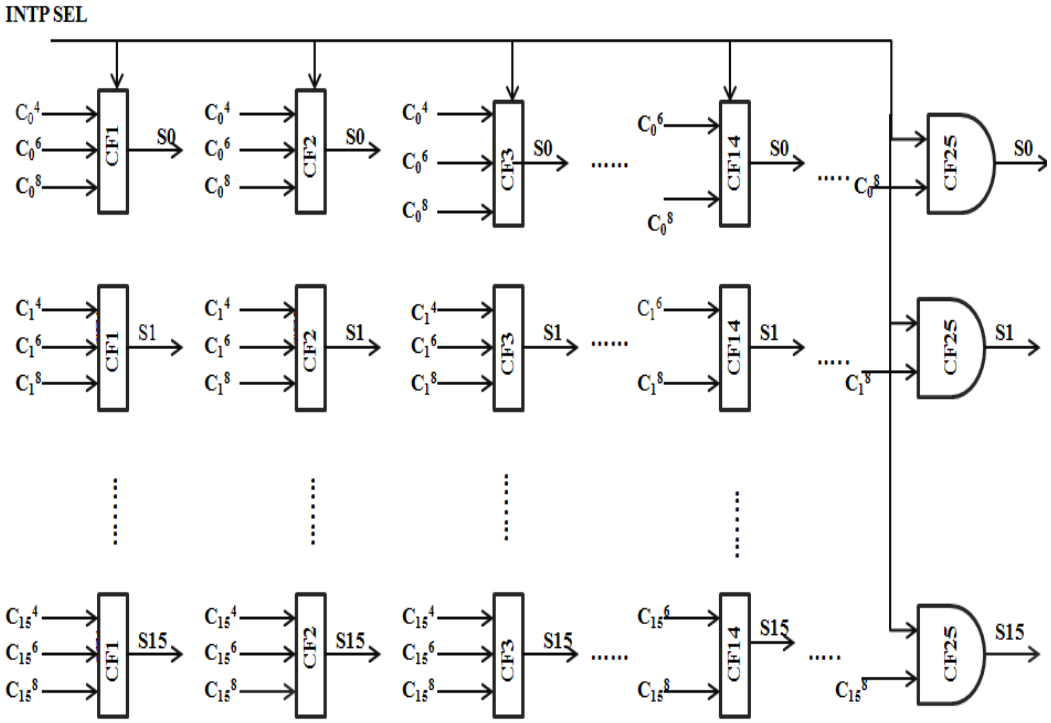

Figure 3. Architecture of SCP Block

3.2.3. Partial Product Generator: During the multiplication operation between the input and the filter coefficients partial product are obtained by using the shift and add method. In BCSE technique, realizations of the common sub expression using shift-and-add method eliminates the common term present in a coefficient. In this architecture, 2-bit BCSs ranging from 00 to 11 have been considered. Within four of these BCSs, an adder is required only for the pattern 11. This produces low complexity hardware and improvement in speed while performing the multiplication operation .The architecture of the PPG block as shown in Figure 4.

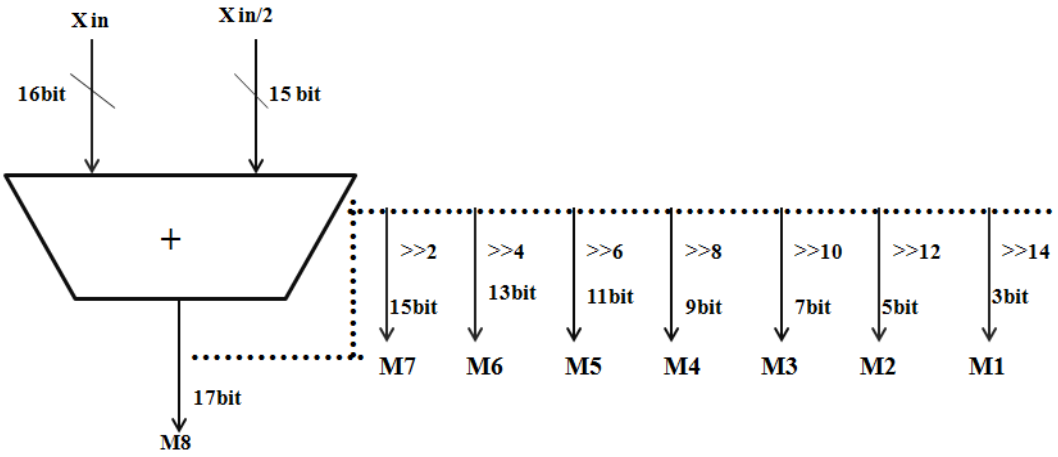

Figure 4. Block Diagram of PPG Block

3.2.4. Multiplexer Unit: The architecture of the multiplexer and final addition unit shown in below Figure 5. The multiplexer unit selects the appropriate data from the partial product unit, depending on coded coefficients. In the multiplexer unit, eight 4:1

multiplexers are used and the coded coefficients are given as the selected lines of the multiplexers. The multiplexers and simple arithmetic adders are producing the output of the multiplexer unit. The inputs p1 to p16 are 2- bit right shifted inputs.

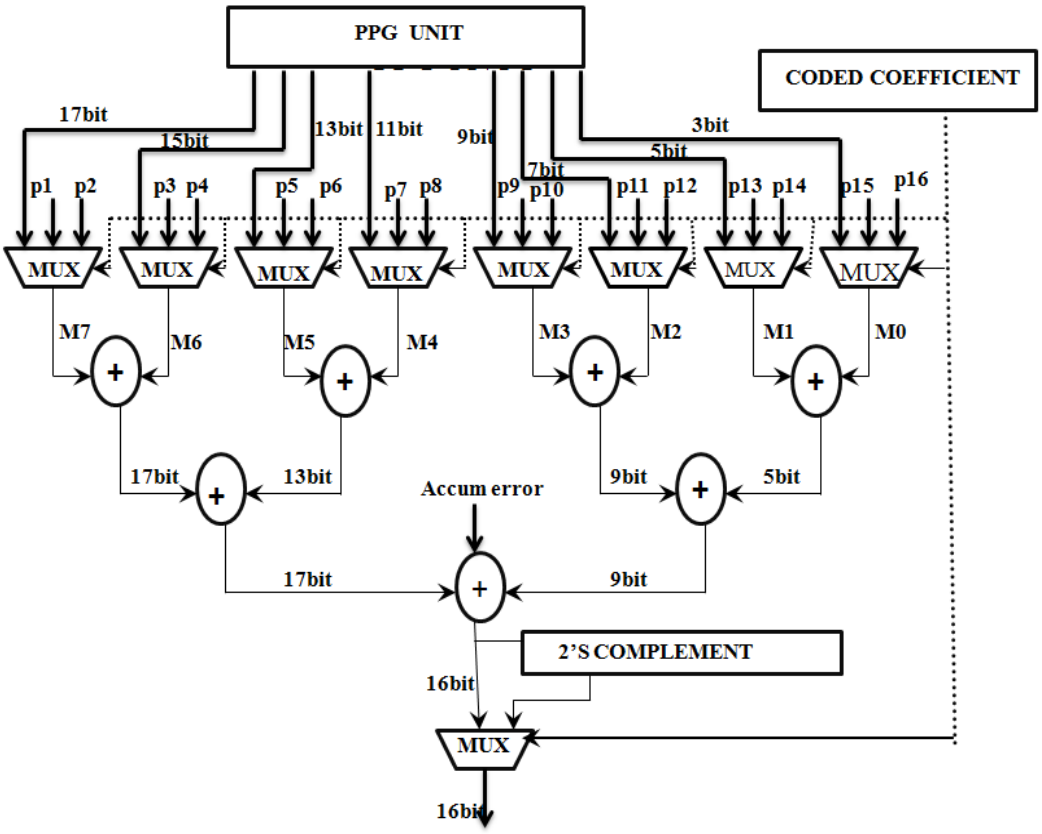

Figure 5. Block Diagram of Multiplexer and Final Addition Unit

3.2.5. Addition Unit: It is used for summing all the outputs of the PPG unit followed by eight multiplexers. Here we have to use Different word length adders for different binary weights. The outputs from the eight multiplexers viz M7–M0 are added together. All the outputs of the multiplexers are added together and the final adder output is passed through the 2's complement circuit. In the addition unit, the final output from this addition unit depends on the sign magnitude bit of the coded coefficient set.

3.3. Coefficient Selector

The inputs of the coefficient selector are taken from the coefficient generator block. This block is used to send proper data to the accumulation block depending on the interpolation factor of the multiplexer's selection line.

3.4. Final Accumulation Unit

In the final accumulation unit, the carry select adders are used for summing all the outputs of the data generator, coefficient generator and coefficient selector. Finally the FIR filter output was produced.

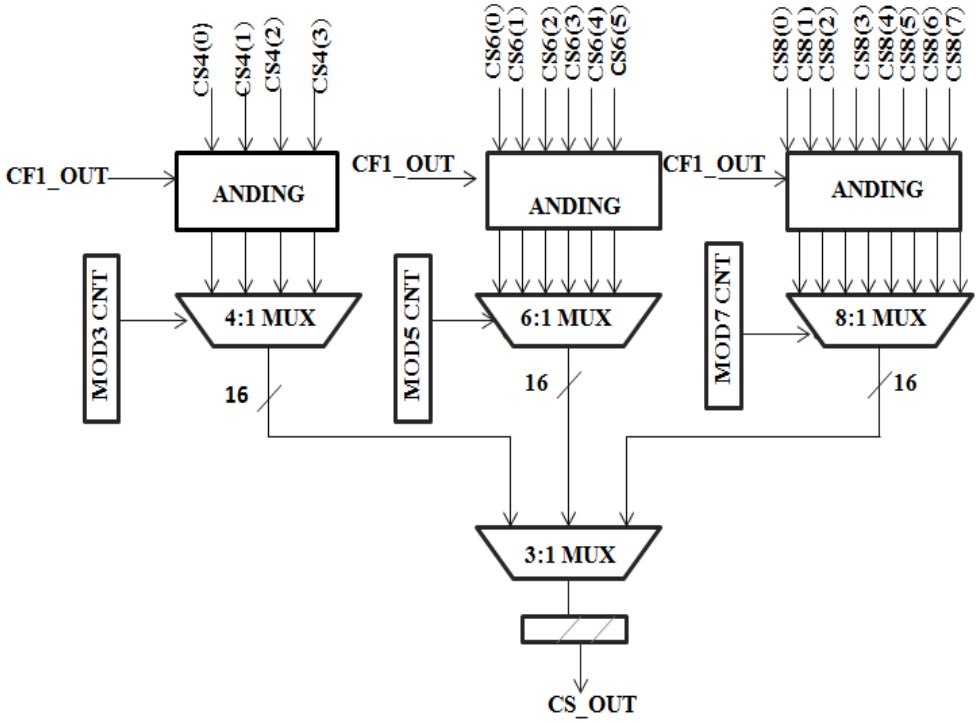

Figure 5. Architecture of CS Block

4. Results and Discussion

The low area and power architecture of pulse shaping FIR filter for multi standard digital up converter has been designed and simulated using Xilinx. The parameters considered for the designed architecture are area, power and delay. The serial input data is passed to the data generator to sample the input which are processed and then produced the output based on the selection line value of the multiplexer. In coefficient generator, the modules are: first Coding pass block, second coding pass block, partial product generator, multiplexer unit and addition unit. These modules process the inputs and produce the output. For coefficient generator, the inputs are taken from the output of the data generator. Each section of the coefficient generator produces the 16-bit output. Then coefficient selector takes the input from the output of the coefficient generator and it will send the proper data based on selection lines. Finally, the final accumulation unit produces the filter output by summing up all the outputs.

In the first coding pass (FCP) block, the coefficient sets of the two RRC filters of the same length differing only by the filter parameters are multiplexed through one 2:1 multiplexer, where one control parameter (FLT_SEL) selects the desired filter. The filter selection value ‘000’ one type of the filter coefficients are obtained and these 16bit out puts are stored as c4,c6and c8 .This multiplexing technique helps in decreasing the requirement of the multiplier by 50%.The two different sets of filter coefficients are the inputs of the first coding pass block. The first coding pass block simulation result is shown in Figure 6.

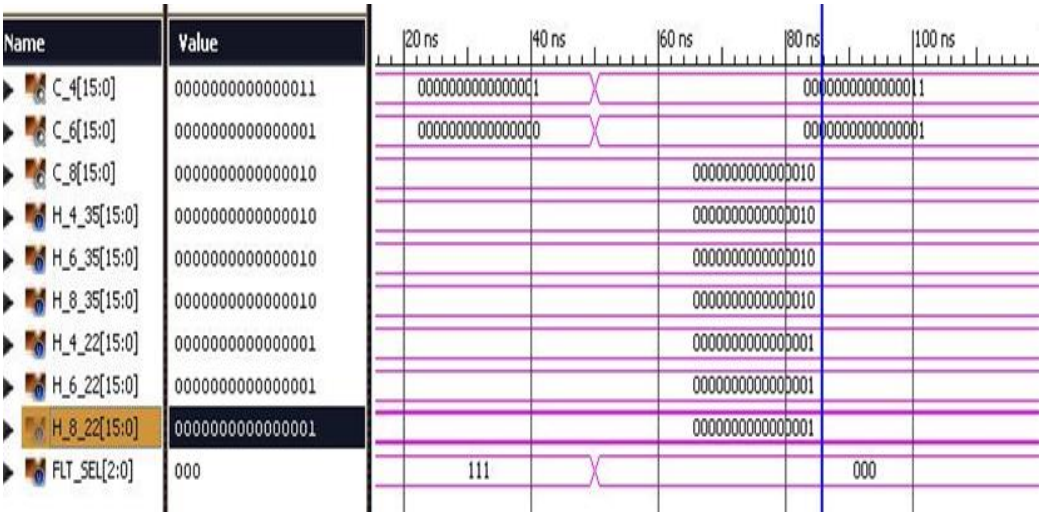

Figure 6. Simulation Result of FCP Block

Now the output obtained from the FCP block is given as the input to the second coding pass block. The SCP block is used to get the final coefficient set. Here three sets of coded coefficients are obtained based on the interpolation selection value. If the interpolation selection value is '001', then the set of 13 coefficients are obtained. The interpolation selection value is '100' then the set of 25 coded coefficients are obtained based on our selection. The simulation result obtained for SCP block is shown in Figure 7.

Figure 7. Simulation Result of SCP Block

In the PPG block, shift and add method is used to generate the partial product. The two bit right shift operation is performed up to possible extent and output will be stored in M8-M1 registers. The simulation result of PPG block as shown in Figure 8.

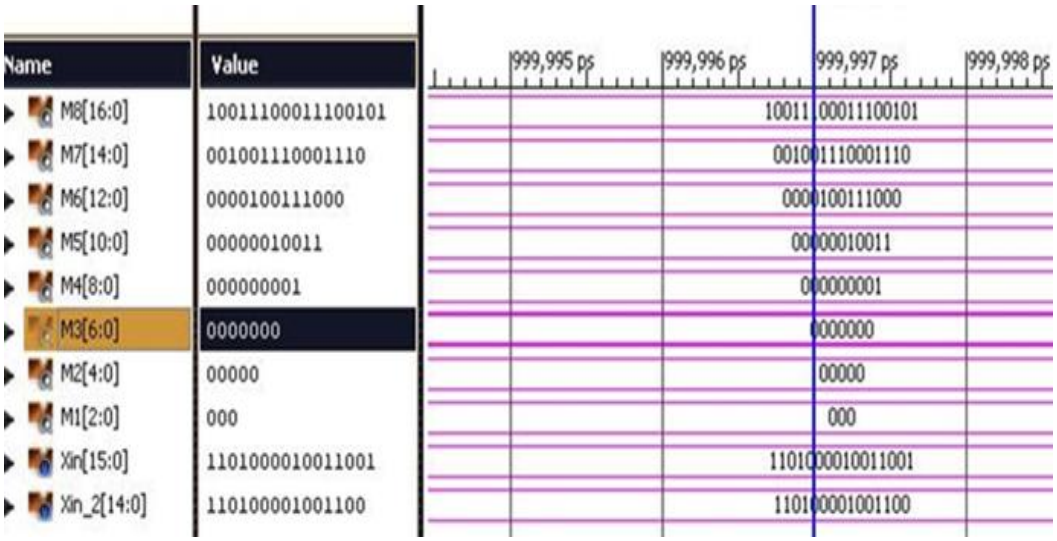

Figure 8. PPG Block Simulation Result

Now the output obtained from the PPG block is given as input to the multiplexer and addition unit. The coded coefficients obtained from the SCP block are given as the control parameters of the multiplexers. Here different word length adders are used for adding different binary weights. The simulation result of the multiplexer and addition unit is as shown in Figure 9.

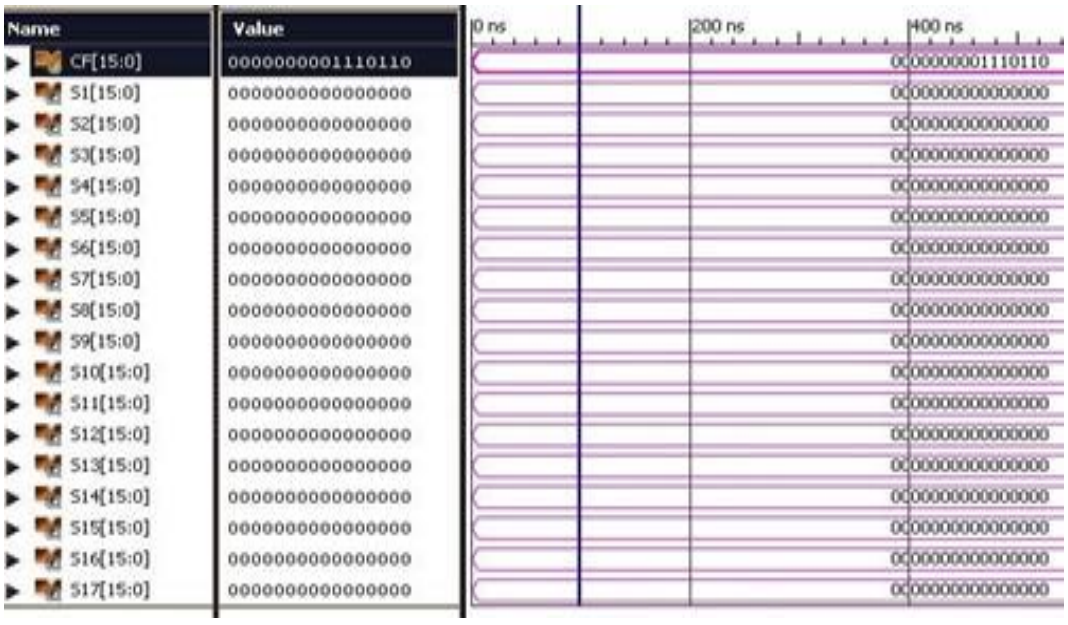

Figure 9. Multiplexer and Addition Unit Simulation Result

Coefficient selector takes the input from the coefficient generator block. The CS block is used to send the proper data to the final accumulation unit depending on the interpolation factor. Three different types of the multiplexers are used based on interpolation value multiplexer is selected. The output of the CS block is 16 bits. The simulation result of the CS block as shown in below Figure 10.

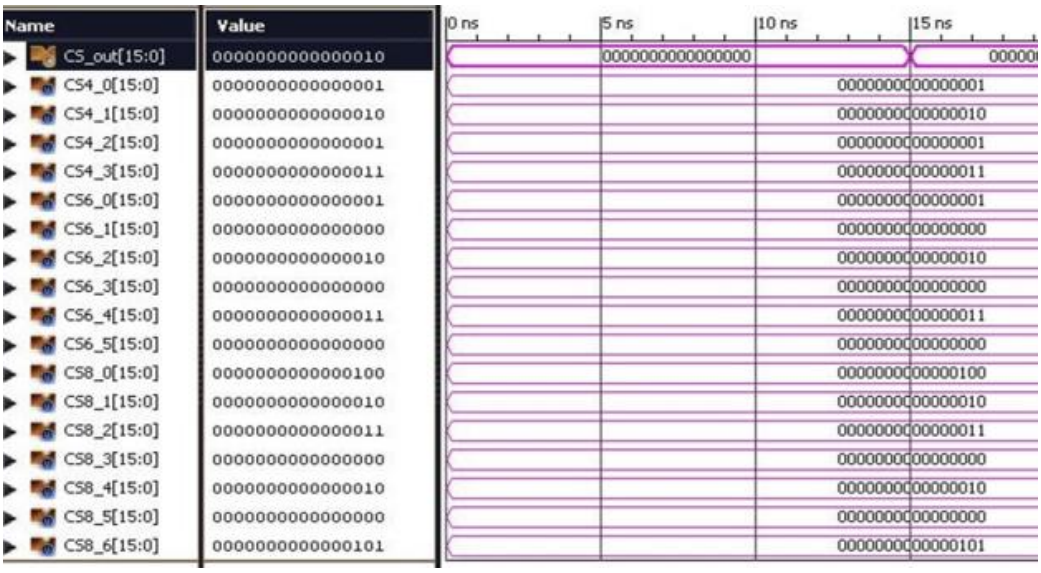

Figure 10. Simulation Result of CS Block

Now finally the output of the reconfigurable RRG filter obtained from the accumulation unit. Here carry select adder and carry save adders are used to add all the outputs of the coefficient selector block. The simulation result of the RRC filter is as show in Figure 11. After HDL synthesis process, the schematic representation of RRC filter is obtained. The detailed view of the RTL schematic is show in Figure 12.

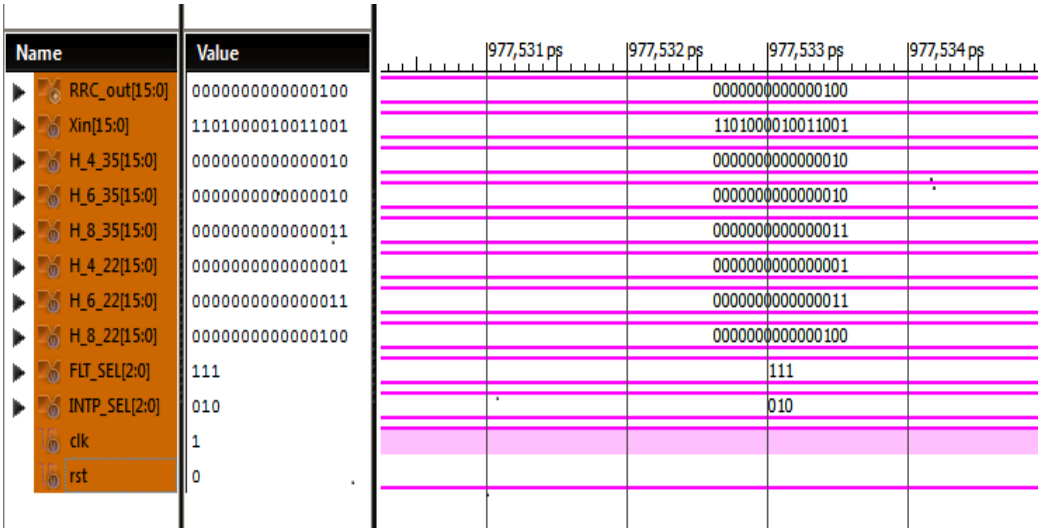

Figure 11. Simulation Result of RRC Filter

5. Comparison of Existing Method and Proposed Method

Comparisons have been done considering the 16-bit width of the input and the width of the coefficient varying by 8, 12, and 16 bits. Based on the trade off between area and delay, in Table 1, we have considered the area, delay and power product for fair comparison. In the existing system, two bit BCSE algorithm [9] and Ripple Carry Adder (RCA) is used in the accumulation unit of the RRC filter. It occupies less area but it is slowest adder among all the other adders. In the existing method delay is 25.88ns and power is 93 mW. For better performance, Carry Select Adder (CSLA) is used instead of

ripple carry adder. It gives low power and minimum delay. In proposed method 1 power and delay parameters are reduced but it occupies more area. The power of the propose method 1 is 82mW and delay is 23.31ns.We have to reduce the area by using Carry Save Adder(CSA) in place of carry select adder in the proposed method1 and it also provides low power when compared to the carry select adder. In proposed method 2 power is79mW and delay is 24.52ns .Area and power of the proposed method2 is reduced but delay is increased. The increased delay of the proposed method 2 is better than the delay of the existing method. Trade off occur between the parameters area, delay and power. If we require less delay and low power carry select adder is used in the accumulation unit of the RRC filter .Carry save adder is used in the accumulation unit of the RRC filter, when minimum area is required.

Table 1. Different Types of the Adders Used in RRC Filter Comparison Result

S.N0	Parameters	Existing method	Proposed method 1	Proposed method 2
1	Power(w)	0.093	0.082	0.079
2	Delay(ns)	25.88	23.31	24.52
3	Area(no. of slices)	460	592	527

6. Conclusion

In this paper, reconfigurable pulse shaping FIR filter for multi standard digital up converter was designed. This filter is important component of the software defined radio/cognitive radio. The proposed filter architecture reduces the number of additions compared with the existing system. The existing method is implemented with 2bit BCSE algorithm.

It is observed that in the proposed architecture the power consumption is reduced. The power consumption in the existing system is 93mW while that of proposed architecture is 82mW. This indicates that the proposed architecture could effectively reduce the power consumption. Similarly, the delay of the existing method is 25.88 ns while the delay of our architecture is 23.31 ns. This proves the efficiency of our architecture both in terms of delay and power. In the proposed method, adders which are used in accumulation unit replaced by carry select adder and carry save adder to achieve the low power, minimum delay and minimum area. The minimum delay is obtained when the carry select adder is used in the accumulation unit of the RRC filter and low power is obtained when the carry save adder is used in the accumulation unit of the RRC filter. The designed pulse shaping FIR filter is simulated and synthesized by using Xilinx. The future scope is different types of other adders are used instead of adders used in the accumulation unit of the RRC filter to achieve less delay and low power. The proposed design seems to be remarkably suitable for next generation multi standard reconfigurable DUC of SDR system where power and area need to be optimized

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