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A Comprehensive Approach for Modeling and Diagnosis of Various Faults in Analog VLSI Circuits

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Abstract

As the advancement in technology the number of application per chip is increasing and chip area remain same. If number of application per chip is increasing so the difficulty level of analog circuit becomes more and more complex. So there are various fault occur in analog VLSI circuits during manufacturing of any analog circuit. If these faults cannot diagnose and remove at initial stage then it will lead to various changes in output of system, which increase the overall cost. In this article we focused on modeling, analysis and diagnosis of various faults which occur in analog VLSI circuit. We describe new approach to diagnose parametric and catastrophic fault in analog circuits with the help of signal flow graph technique. This technique is very simple and structural in nature. It is applicable to various linear analog VLSI circuits. In this paper we implement this approach on MIMO (Multi Input Multi Output Circuit).All the equation and model for MIMO circuit and simulation are done with the help of MATLAB/Simulink tool.

Keywords: *Parametric, Faults, Modeling, MIMO, Diagnosis, Signal Flow Graph*

1. Introduction

If we design any product, fabricate and test it and then it fails in the test then there must be a cause for the failure. Either the test was wrong, or the fabrication Process was faulty, or the design was incorrect, or the specification had a problem. Anything can be wrong as discuss in above. The role of testing is to detect whether something went wrong and the role of diagnosis is to determine exactly what went wrong, and where the process needs to be altered. Therefore, correctness and effectiveness of testing is most important for quality products.

If the test process is good and the product fails, then we suspect on fabrication process, the specification or the design. If all students in a class fail then it is often considered the teacher's failure. If only some fail, we assume that the teacher is competent, but some students are having difficulty. To select students likely to succeed, teachers may use prerequisites or admission tests for screening. Distributed testing along a product realization process catches the defect-producing causes as soon as they become active, and before they have done much damage [1-2].

Due to wide range of application of analog VLSI circuit. The need of analog VLSI circuit testing is the crucial part of any device for proper functioning. For proper understanding the concept of analog VLSI testing. A simple example is taken here. If you are a student now, or were in the past, you are quite familiar with the word test, and probably hate it. Understanding the teacher's point of view will help. The teacher sets a domain of knowledge for testing, called the course syllabus. It may be the contents of a book, class notes, lectures, combination of all those. Next, comes the testing method. The teacher asks questions and analyses the response, perhaps by matching answers to correct ones from the book. If the answer is correct then student qualify the test and test coverage depends upon the number of answer are correct. In similar way, in analog VLSI testing,

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we should know about the circuit parameter and specification before test the analog circuit. And then analog circuit is tested if its output response meets the expected response then test is passed.

With increasing integration level in modern VLSI chips, the difficulty of testing them also increases. This is due to internal module of analog VLSI chips are very difficult to access. Testing cost of any circuit become significant part of total manufacturing cost of any device. Hence there is need to overcome this cost. The major factor that impact the testing cost is the time required to test any device. This time can be reduced if number of test required to test device is reduced. So we need test technique which required less number of test, consume less time and cost effective [3].

2. Fault Modeling of Analog Circuits

The conventional fault models for analog circuits are catastrophic or hard faults, where an analog component becomes open or shorted, and the parametric or soft faults, where an analog R, L, C, or transistor trans-conductance value changes sufficiently that it moves outside its tolerance box and causes unacceptable performance degradation of the analog circuit. Sometimes the additional faults stuck-at- and stuck-at- are also included in the catastrophic faults [4]. Catastrophic faults are easy to test, and parametric faults are difficult to test.

Single parametric faults are interesting in multi-chip module interconnects, as they will be termination resistances or important components such as precision off chip inductors used in RF circuits. Linear analog ICs are designed so that the analog performance depends on ratios of components, so multiple parametric faults are most interesting in such chips. Many analog circuits are designed using Block's negative feedback principle, where an OPAMP is configured with an input impedance and a feedback impedance. Generally, it is the ratio of these two impedances that determine whether the OPAMP circuit is an integrator, a differentiator, or a buffer. Therefore, a multiple parametric fault model is the most useful fault model in this situation.

3. Example of SFG Technique

Let us consider a simple example of forward signal flow graph. Let us take a equation which is represented through SFG.

$$y = a\,x\,. \tag{1}$$

The forward signal flow graph of this equation is given below.

Figure 1. Example of SFG

3.1. Algorithm for SFG Inversion

This approach describe step by step procedure for SFG inversion.
Here example of equation and their signal flow graph.

$$X_2 = aX_1 + bX_3 \tag{2}$$

$$X_4 = -\,cX_2 \tag{3}$$

The signal flow graph for equation (2) & (3) is given below.

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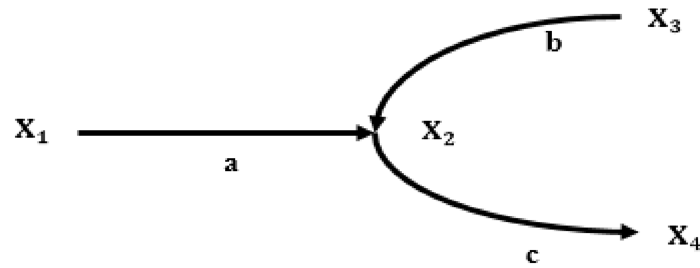

Figure 2. Signal Flow Graph of Above Equation (2) & (3)

Step1.Select path in signal flow graph from PI X_1, through intermediate nodes X_2 through X_{n-1} to PO X_n.

Step2. Start from PI X_1, a source node which contain only outgoing edges.

Step3. Reverse the direction of the outgoing edge from X_1 to X_2, and the new weight 1/a is the reciprocal of the old weight (a). X_1 becomes a sink node.

Step4. Redirect all edges incident on X_2 to X_1, multiply the original weights by the new weight 1/a on the reversed edge from x_2 to x_1, and change the sign of edges weight.

Step5. Repeat Steps 3 and 4 for all source nodes x_i on the path from PI x_1 to PO x_n, until x_n becomes a source node. When the entire graph edges point towards the input, the graph is inverted.

4. Analysis of Fault in MIMO Circuit

Figure 3, shows circuit diagram of MIMO circuit. Circuit diagram of MIMO circuit contain five op amp, eleven resistors and two capacitor. The nominal value of resistor R=10kΩ and C=.01μF. the frequency used for testing is 1 kHz [5-6].

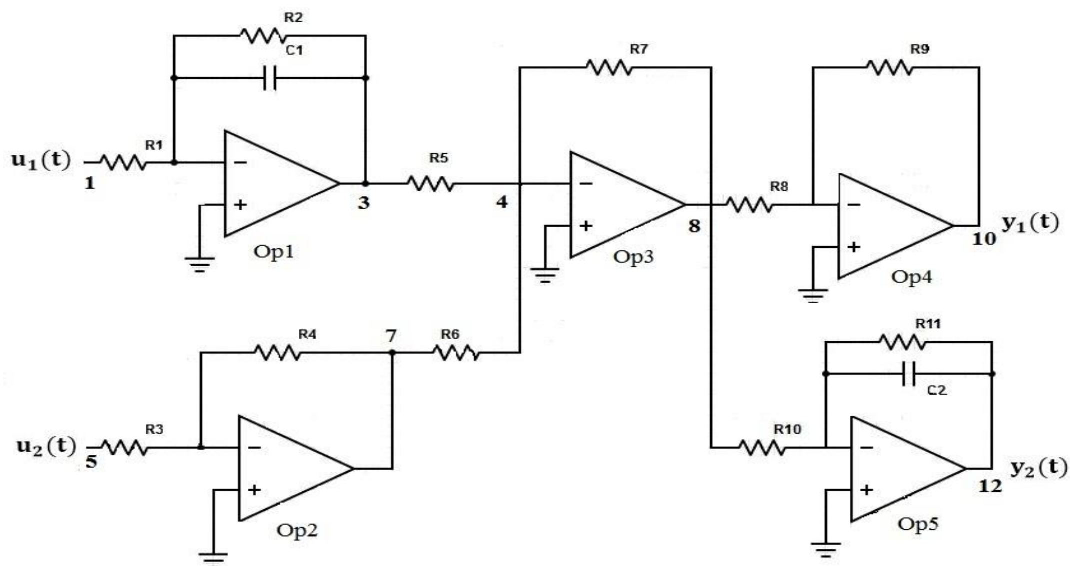

Figure 3. Circuit Diagram of MIMO Circuit

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MIMO circuit takes two input from $u_1(t)$ and $u_2(t)$ and provide two output at $y_1(t)$ and$y_2(t)$. The nominal values of component in MIMO circuit are R=10kΩ and C=.01μF. Here calculated y_1 to be 4V sinusoidal and assumed u_2 as 2V sinusoidal both are in phase. One can calculated using analog back trace 7V sinusoidal is out of phase with u_2. multiple input multiple output circuit is tested by inverting the path between one of PI to PO [7-8]. Assumed the signal at PI is good and the signal at PO is bad to calculate the test signal PI. In MIMO circuit path between $y_2$to u_1 is inverted only. The inverted signal flow graph is shown in Figure 4.

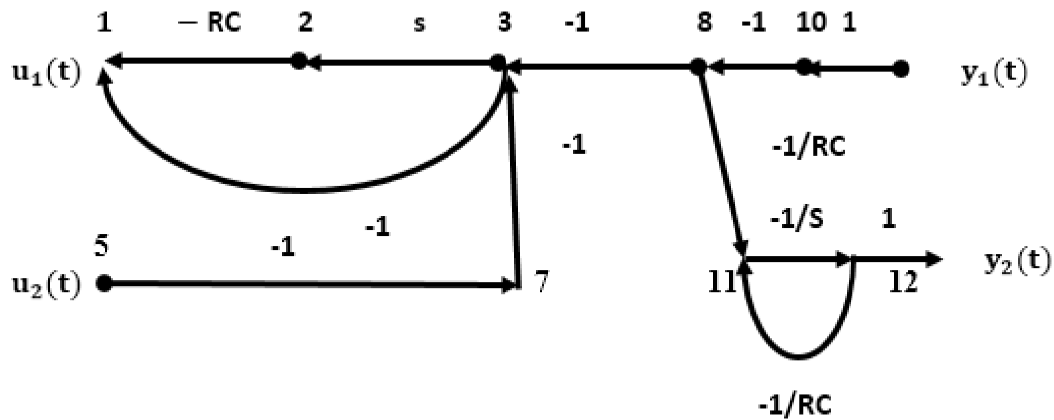

Figure 4. SFG of MIMO Circuit

Assume set of test waveform sample for $u_2(t)$ .here traverse the following edges of above signal flow graph. In forward signal flow graph the order of good signal values are (10,y_1), (8,10),(3,8),(2,8),(1,3),(1,2),(8,11),(11,12) and (12, y_2). Now apply equation (1) to the edges without s operator.

Now to calculate good values using nominal value of component at every node of signal flow graph. The forward signal flow graph model of MIMO circuit was discussed. Figure 5, shows response of MIMO circuit, which help us to calculate component deviation.

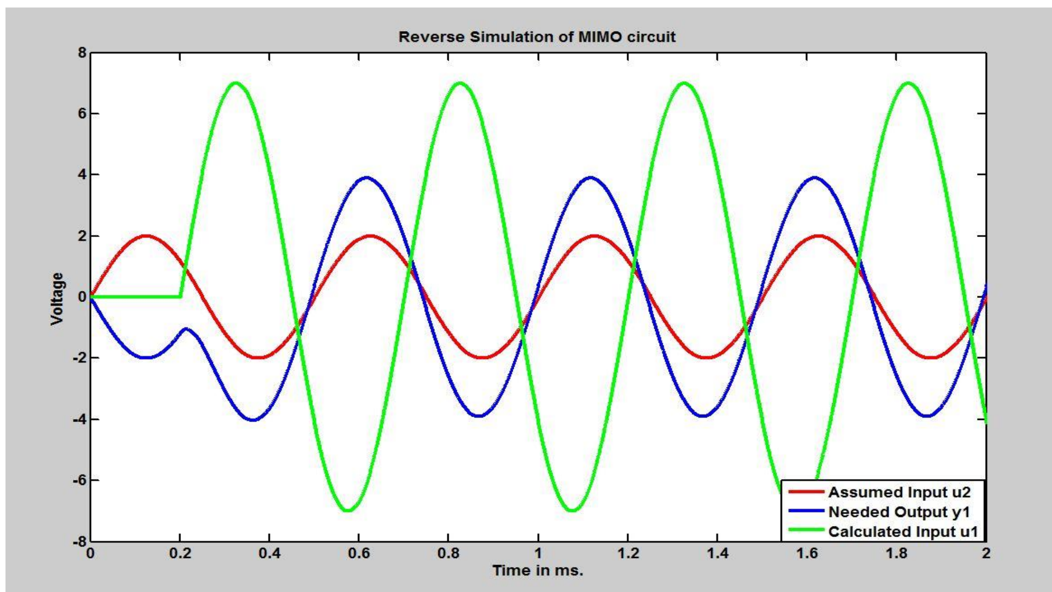

Figure 5. Response of MIMO Circuit

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In Figure 6, by using reverse signal flow graph algorithm reverse the whole graph. Here one can specifies faulty values for positive 10% tolerance. So after calculating all good values at Nodes of signal flow graph. Here increase the output by 10% so that one can calculate the deviation of component. By increase output voltage amplitude to 10%, calculate all bad values at every Node of signal flow graph. The calculation of faulty value is given below.

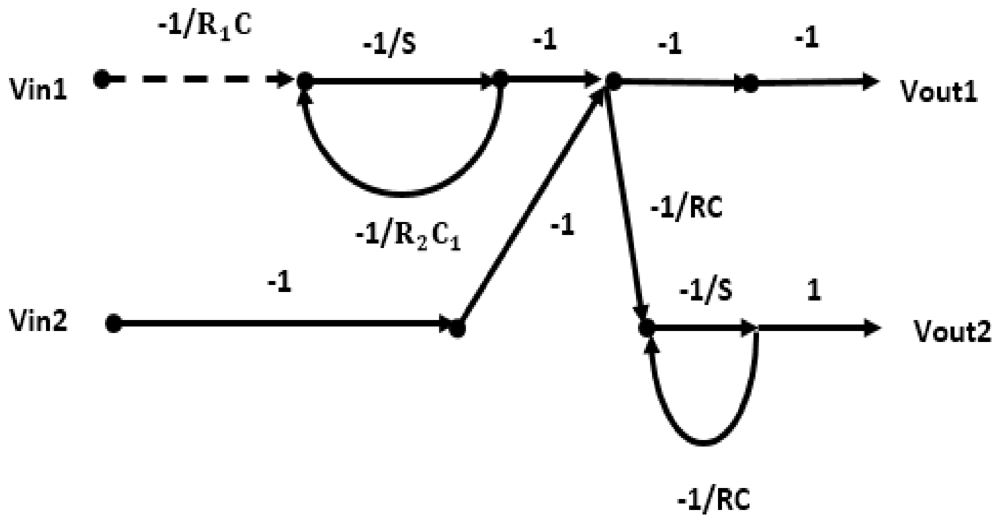

Figure 6. Signal Flow Graph of MIMO Circuit with Faulty R_1

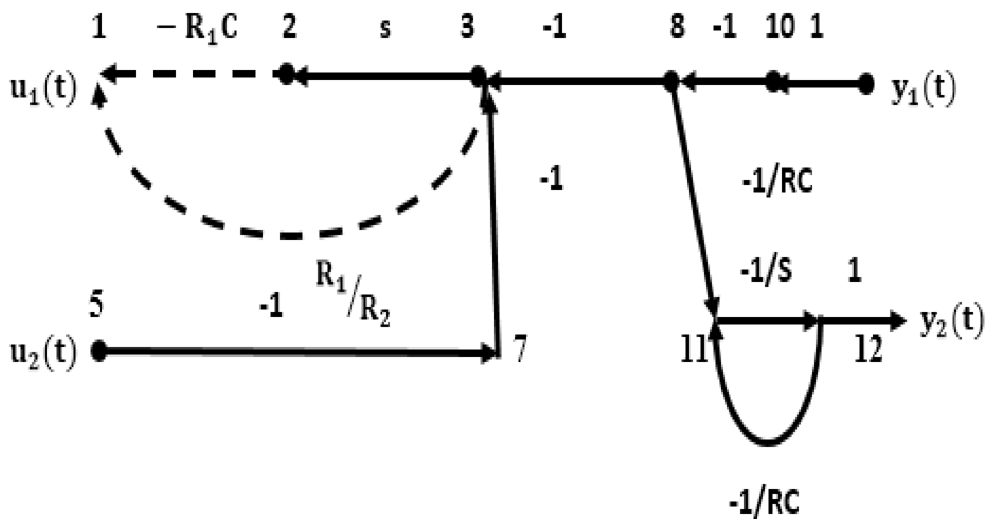

Figure 7. Inverted Signal Flow Graph of Faulty R_1

In above signal flow graph R_1 is consider as fault in circuit. So here placed a dotted line where R_1 exist in the circuit. Due to $R_1$the input of reverse signal flow graph will change out of its nominal value. So calculate the component deviation by increasing output to 10%. The equation derived to calculate the R_1 from above circuit is given below.

$$\text{Good value (1)} = -R_1 C \text{ Bad value (2)} - \frac{R_1}{R_2} \text{ Bad value (3)} \qquad (4)$$

Bad value (3) =Good value (5) − Bad value (8)

Good value (1) = $-R_1C$ Bad value (2)$-\frac{R_1}{R_2}$ (Good value (5) − Bad value (8))

Good value (1) = $R_1(-C$ Bad value (2)$-\frac{1}{R_2}$ (Good value (5) − Bad value (8))

$$\text{Bad value of } R_1 = \frac{\text{Good value (1)}}{(-C\text{ Bad value (2)}-\frac{1}{R_2}(\text{Good value (5)} - \text{Bad value (8)})} \quad (5)$$

$$\text{Good value of } R_1 = \frac{\text{Good value (1)}}{(-C\text{ Bad value (2)}-\frac{1}{R_2}(\text{Good value (5)} - \text{Good value (8)})} \quad (6)$$

$$\text{Tolerance of } R_1 = \text{Good value of } R_1 - \text{Bad value of } R_1 \quad (7)$$

Thus by calculating the tolerance of R_1 one can compute the maximum excursion permissible at output of analog circuit due to fault. Calculated this by symbol edge weights, good node value and bad node values.

4.1. Mathematical Calculation for Faulty Resistor R_2

In this section we will describe the mathematical calculation for resistor $\mathbf{R_2}$. As it is clear that from Figure 8, the doted line represent fault in signal flow graph. Because it contain R_2 resistor.

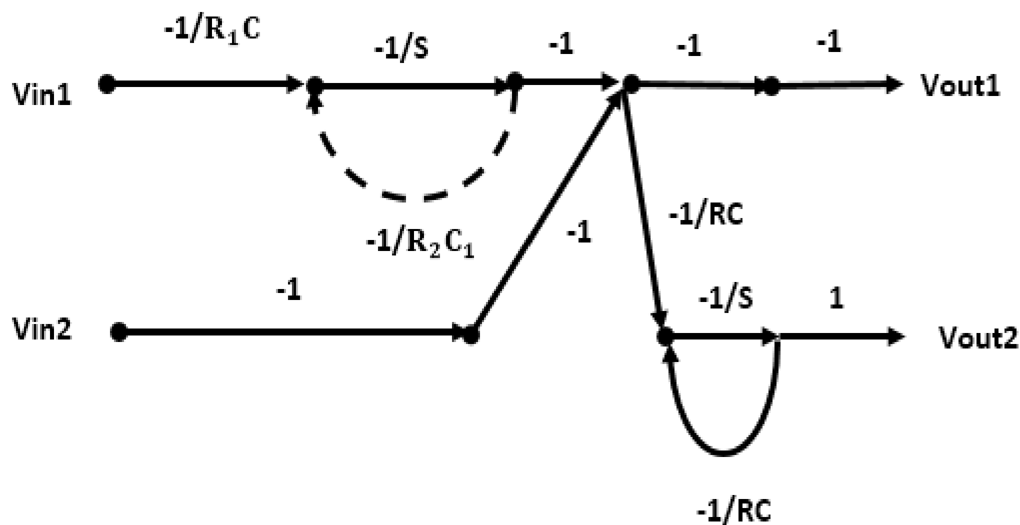

Figure 8. Original Signal Flow Graph of MIMO Circuit with Faulty R_2

Figure 9, represent inverted signal flow graph for MIMO circuit. With the help of Figure 8, and Figure 9, signal flow graph we can calculate resistor $\mathbf{R_2}$ tolerance. Which will help us to diagnose parametric fault in analog VLSI circuit?

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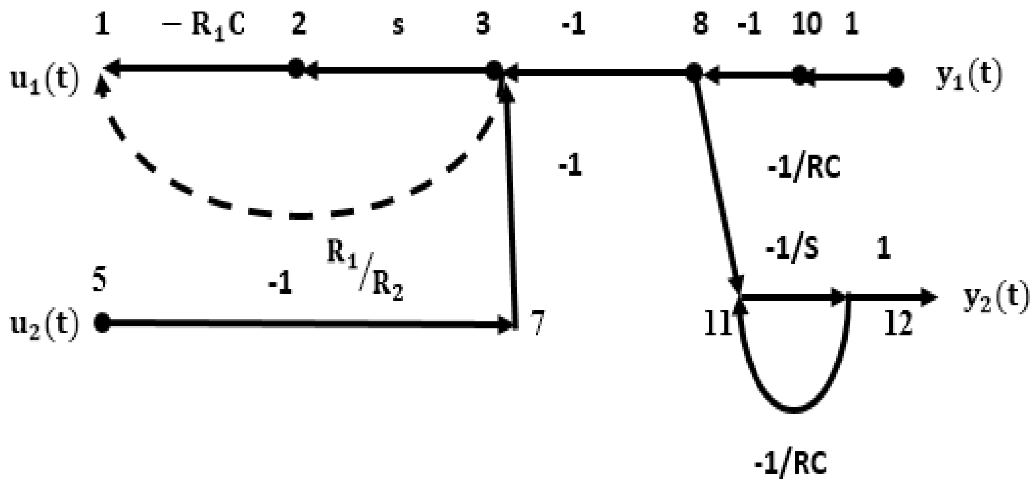

Figure 9. Inverted Signal Flow Graph of Faulty R_2

For calculation of faulty element in analog circuit (MIMO circuit). Here consider nominal value of all components. For calculation of fault exist in path between $y_1(t)$ to $u_1(t)$ and between $u_2(t)$ to $u_1(t)$ there is no need of path between node 8 to node 12. So neglect this path for calculation of faulty component in other path [28].

$$\text{Good value }(1) = -R_1C\text{ Good value }(2) - \frac{R_1}{R_2}\text{Bad value }(3) \tag{8}$$

$$\text{Good value }(1) + R_1C\text{ Good value }(2) = -\frac{R_1}{R_2}\text{ Bad value }(3)$$

$$R_2(\text{Good value }(1) + R_1C\text{ Good value }(2)) = -R_1\text{Bad value }(3)$$

$$\text{Bad value of } R_2 = \frac{-R_1\text{ Bad value }(3)}{\text{Good value }(1) + R_1C\text{ Good value }(2)} \tag{9}$$

$$\text{Good value of } R_2 = \frac{-R_1\text{ Good value }(3)}{\text{Good value }(1) + R_1C\text{ Good value }(2)} \tag{10}$$

$$\text{Tolerance of } R_2 = \text{Good value of } R_2 - \text{Bad value of } R_2 \tag{11}$$

In a similar way one can calculate the value of capacitor in MIMO circuit.

4.2. Mathematical Calculation for Faulty Capacitor C

The faulty value of capacitor is calculated as discussed below. In this section we will describe the mathematical calculation for capacitor C. As it is clear that from Figure 10, the doted line represent fault in signal flow graph.

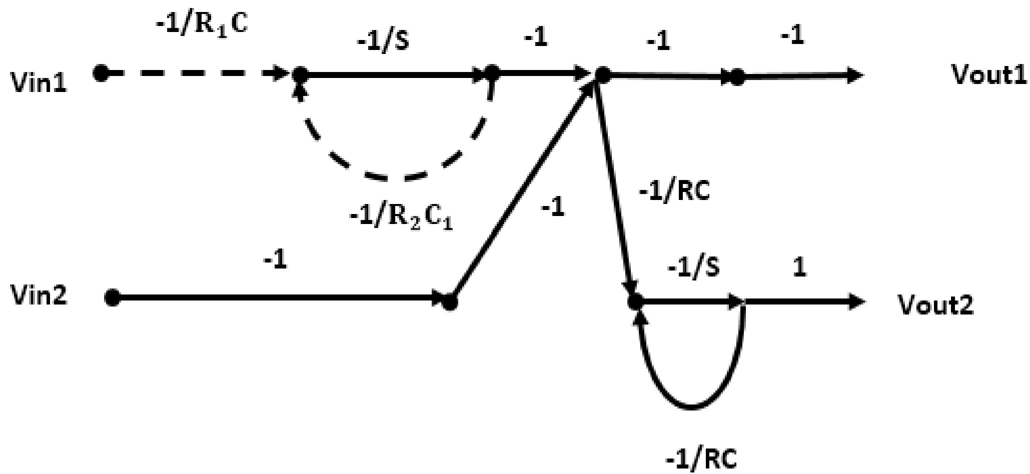

Figure 10. Original Signal Flow Graph of MIMO Circuit with Faulty C

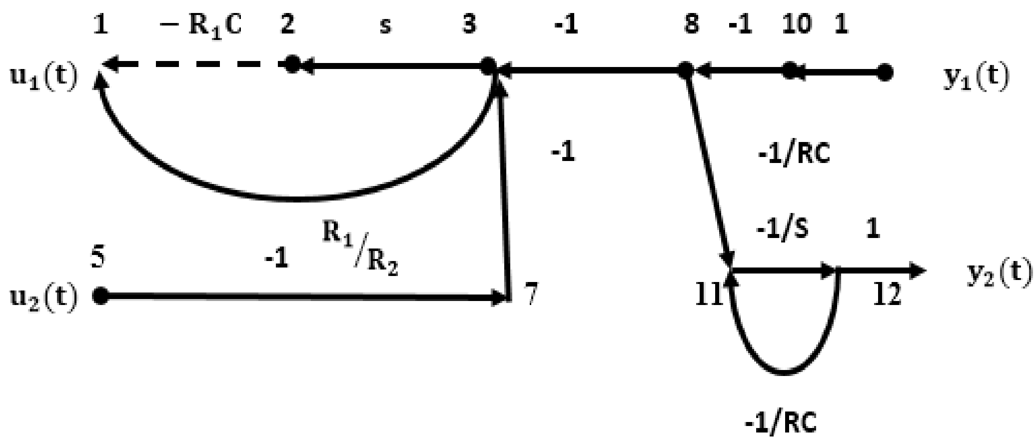

Figure 11. Inverted Signal Flow Graph of Faulty C

Figure 11, represent inverted signal flow graph for MIMO circuit with fault in capacitor C. With the help of Figure 10, and Figure 11, signal flow graph we can calculate resistor **C** tolerance. Which will help us to diagnose parametric fault in analog VLSI circuit? The mathematical calculation for tolerance of **C** is discussed below.

$$\text{Good value (1)} = -R_1C \text{ Bad value (2)} - \frac{R_1}{R_2} \text{ Good value (3)} \quad (12)$$

$$\text{Good value (3)} = \text{Good value (5)} + \text{ Bad value (8)}$$

$$\text{Good value (1)} = -R_1C \text{ Bad value (2)} - \frac{R_1}{R_2} (\text{Good value (5)} + \text{ Bad value (8)})$$

$$\text{Good value (1)} + \frac{R_1}{R_2} (\text{Good value (5)} + \text{ Bad value (8)}) = -R_1C \text{ Bad value (2)}$$

$$\text{Bad value of C} = \frac{\text{Good value (1)} + \frac{R_1}{R_2} (\text{Good value (5)} + \text{ Bad value (8)})}{-R_1 \text{ Bad value (2)}}$$

$$\text{Good value of C} = \frac{\text{Good value (1)} + \frac{R_1}{R_2} (\text{Good value (5)} + \text{ Good value (8)})}{-R_1 \text{ Good value (2)}}$$

$$\text{Tolerance of C} = \text{Good value of C} - \text{Bad value of C} \quad (13)$$

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With the help of equation 13 we can calculate the deviation in capacitance value of MIMO circuit. In a similar way compute all single parametric fault deviation for multiple input multiple output circuit.

Table 1. Computed Deviation for MIMO Circuit

Component	Allowed value	Deviation (%)
R_1	9.38 kΩ	6.25
R_2	10.68 kΩ	6.8
R_3	11 kΩ	10
R_4	7 kΩ	30
R_5	9.3 kΩ	7
R_6	11 kΩ	10
R_7	11 kΩ	10
R_8	9.09 kΩ	9.1
R_9	11 kΩ	10
C	0.008μF	20

Table 1, shows deviation of MIMO circuit with the help of deviation in every component we can diagnose parametric fault of that component. The deviation is calculated for ±10% tolerance.

5. Catastrophic Fault Diagnosis in MIMO Circuit

The test waveform single parametric fault can also use to detect catastrophic faults in analog circuit [9-10]. To verify this statement, a example of MIMO circuit here. The allowed output must be in the range of values V_{out} ×(1±Tolerence) Region 1 in Figure 12.

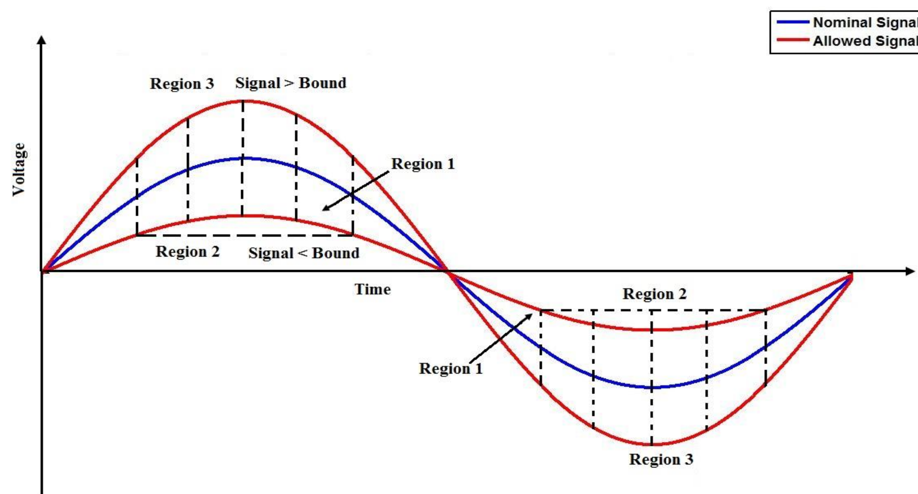

Figure 12. Good and Bad Output Signal Region in Analog Circuits

The single parametric fault model specify all deviation of the component that change the output for good and bad values of analog circuit. The test signal is designed in such a way that produce a faulty output if the parametric fault is present in the circuit. Then faulty output will be in the Region 2 or Region 3 [11-12]. There are four cases exist here.

1) If increase the component value then the cross ponding output will increase. Let's us increase the faulty component value to double. Since the analog circuit is linear. The output will further increase to the faulty region (that is in Region 3 in above Figure (12), further doubling the component value will leads the output to out off region 3. If increase the value very high (lets us say infinity). The output will lies beyond the region 3 and the fault will be detected.

2) If increase the component value then the cross ponding output will decrease. Double the component value leads to decrease the output that will go beyond the limit (lies in Region 2). And if this component value will be increase to infinity the output of circuit stay faulty and fault is detected.

3) If decrease the component value cross ponding output will increase. Since taken circuit is linear. By halving decrease the component value leads to output to lies in Region 3. And if decrease the faulty component value then V_{out} ×(1+Tolerence) and signal goes to region 2. If the component value decrease to zero then output of analog circuit remain in faulty region (Region 3). And fault is detected.

4) Decrease the component value leads to decrease the output amplitude of the analog circuit. By halving the component value decrease the output so that it goes beyond the limit into the V_{out} ×(1-Tolerence) to zero range and lies in Region 2. As the component decrease and tend to zero, the output stay in faulty region and fault is detected.

In reverse signal flow graph algorithm, consider 10% output voltage tolerance [13-16]. Nominal component values are R=10kΩ and C=0.01uF. Figure 4. 11 has test waveform for MIMO circuit used for single parametric faults. The nominal output of the MIMO circuit were 4V peak sinusoidal at Node 10 and 3V peak sinusoidal at Node 12. By fault simulation found all single catastrophic fault in this circuit were detected. For fault detection, use R=1000GΩ for open circuit resistance and R=.01Ohm for short circuit resistance. And capacitor values are C=0.0001pF for short circuit capacitance and C=100μF for open circuit capacitance [17-19]. The frequency used for calculation of catastrophic fault in multiple input multiple output circuit is 1 kHz. And simulation is performed at 5ms transient analysis. The simulation are performed on Or Cad Capture CIS version 16.6. By using this technique detect all catastrophic fault in MIMO circuit successfully and complete description about fault (open and short) is given below Table 2.

Table 2. Fault Simulation Results for MIMO Circuit

Component	Fault	Result
$\mathbf{R_1}$	Open	Very low voltage at Node 3
$\mathbf{R_1}$	Short	OPAMP 1 saturates
$\mathbf{R_2}$	Open	DC offset at Node 3
$\mathbf{R_2}$	Short	Very low voltage at Node 3
$\mathbf{R_3}$	Open	Very low voltage at Node 7
$\mathbf{R_3}$	Short	OPAMP 2 saturates
$\mathbf{R_4}$	Open	OPAMP 2 saturates
$\mathbf{R_4}$	Short	Very low voltage at Node 7
$\mathbf{R_5}$	Open	Very low voltage at output
$\mathbf{R_5}$	Short	OPAMP 3 saturates
$\mathbf{R_6}$	Open	Very low voltage at output
$\mathbf{R_6}$	Short	OPAMP 3 saturates
$\mathbf{R_7}$	Open	OPAMP 3 saturates

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$\mathbf{R_7}$	Short	Very low voltage at Node 8
$\mathbf{R_8}$	Open	Very low voltage
$\mathbf{R_8}$	Short	OPAMP 4 saturates
$\mathbf{R_9}$	Open	OPAMP 4 saturates
$\mathbf{R_9}$	Short	Very low voltage at Node 8
$\mathbf{R_{10}}$	Open	Very low voltage
$\mathbf{R_{10}}$	Short	OPAMP 5 saturates
$\mathbf{R_{11}}$	Open	OPAMP 5 saturates
$\mathbf{R_{11}}$	Short	Very low voltage
$\mathbf{C_1}$	Open	Node 12 =0
$\mathbf{C_1}$	Short	Node 10 output increase

6. Conclusion

The methodology developed in this article defined analog output faults in term of magnitude deviation and developed a fault definition strategy for analog circuit component. A new reverse simulation method has been developed for backtracking through analog circuits and shown it to be highly accurate in generating analog test. Backtracking does not increase test cost because this is done only for test wave form generation. It has potential to decrease test cost by generating more effective test waveform which cover analog component rather than DSP based testing We describe step by step signal flow graph approach for detection of faults and we implement our approach on multi input multi output circuit. This approach is structural in nature and applicable to linear analog VLSI circuits. In this article for simulation of faults we use 10% tolerance only. The tolerance can we specified by the designer. This approach is successfully implemented for MIMO circuit. In future researcher can implement this approach for analog and mixed signal devices.

References

[1] J. Cui and Y. Wang, “A novel approach of analog circuit fault diagnosis using support vector machines classifier”, Measurement, vol. 44, no. 1, **(2011)**, pp. 281-289.
[2] A. S. S Vasan, B. Long and M. Pecht, “Diagnostics and prognostics method for analog electronic circuits”, IEEE Transactions on Industrial Electronics, vol. 60, no. 11, **(2013)**, pp. 5277-5291.
[3] V. D. Plassche and J. Rudy, “CMOS integrated analog-to-digital and digital-to-analog converters”, Springer Science & Business Media, vol. 742, **(2013)**.
[4] L. Milor and A. L. S. Vincentelli, “Minimizing ProductionTest Time to Detect Faults in Analog Circuits”, IEEETrans. on Computer-Aided Design, vol. 13, **(1994)** June, pp. 796-813.
[5] N. B. Hamida and B. Kaminska, “Multiple Fault Analog Circuit Testing by Sensitivity Analysis”, Electronic Testing: Theory and Applications, vol. 4, **(1993)** November, pp. 331-343.
[6] L. Yuan, Y. He, J. Huang and Y. Sun, “A new neural-network-based fault diagnosis approach for analog circuits by using kurtosis and entropy as a preprocessor”, IEEE Transactions on Instrumentation and Measurement, vol. 59, no. 3, **(2010)**, pp. 586-595.
[7] J. Vineela, G. Praneetha, R. Harshad, K. Masrunnisa, M. Pruthvi Kumar and T. Sandeep, “A Complete Analysis of Tolerance of Component in Analog VLSI Circuits Using Sensitivity”, International Journal of Hybrid Information Technology, vol. 9, no. 7, **(2016)**, pp. 9-18.
[8] S. Thakur, K. V. V. Satyanarayana and K. C. M. Reddy, “Diagnosis of Parametric Faults in Linear Analog VLSI Circuits”.
[9] S. Thakur, “A Complete Analysis of Channel Estimation and Peak to Average Power Ratio in Wireless Communication Using Discrete Fourier Transform”, International Journal of Future Generation Communication and Networking, vol. 9, no. 1, **(2016)**, pp. 107-114.
[10] S. Thakur and N. Kumar, “Design and Analysis of Multi Input Logic Gates Based on Quantum Dot Cellular Automata”, IJRECE 3, no. 3, **(2015)**, pp. 70-73.
[11] K. Maggard, P. Karunaratna and C. Stroud, “Built-InSelf Test for analog circuits in Mixed Signal System”, Proc.IEEE Southeast Regional Conf., **(1999)**.
[12] A. Naithani and S. Thakur, “Performance Analysis and Simulation of Wind Turbine Using Doubly fed Induction generators for Various Voltage Sags at Grid”.

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[13] A. Chatterjee, "Concurrent Error Detection in Linear Analog and switched-capacitor state variable systems using continuous checksums", Pmc IEEE Intl. Test ConI., **(1991)**, pp. 582-591.
[14] A. Osseiran, "Analog and mixed-signal boundary-scan: A guide to the IEEE 1149.4 test standard", Springer Science & Business Media, vol. 16, **(2013)**.
[15] A. Chatterjee, "Checksum-based Concurrent Error Detection in Linear Analog Systems with second and higherorders", Pmc IEEE VLSI Test Symp., **(1992)**, pp. 286-291.
[16] J. Vineela, G. Praneetha, R. Harshad, K. Masrunnisa, M. Pruthvi Kumar and T. Sandeep, "A Complete Analysis of Tolerance of Component in Analog VLSI Circuits Using Sensitivity", **(2016)**.
[17] N. Balabanian, T. A. Bickart and S. Seshu, "Electrical Network Theory", John Wiley & Sons, Inc. (**1969**).
[18] B. Kaminska, K. Arabi, I. Bell, P. Goteti, J. L. Heurtas, B. Kim, A. Rueda and M. Soma, "Analogand Mixed-Signal Benchmark Circuits FirstRelease", IEEE International Test Conference,Washington DC,November, **(1997)**.
[19] A. Meixner and W. Maly, "FaultModelingfortheTestingofMixedIntegratedCircuits", Proc.oftheIEEEInt'l.TestConf., **(1991)** October, pp. 564–572.

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