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A 4th-Order Wideband Sigma Delta Modulator Using Linear System Theory Technique

Ming-yuan Ren, Yong-sheng Zhang, Wei-kun Wu, Zhen-xi Bao, Zi-wei Zhao, Chao Li and Hong-guo Zhang

School of Software,Harbin University of Science and Technology, Harbin, China
E-mail:zhg07@163.com

Abstract

A 4th-Order Wideband Sigma Delta modulator structure is proposed in this paper, which uses linear system theory technique. There are many implementation techniques to improve the performance of Sigma Delta ADCs, such as noise coupling, differential sampling and dynamic elements matching. An extra loop delay is needed to be added in the system. This paper explains how to make the modulator stable with the addition of feed-forward and feed-back branches which are used to compensate the extra loop delay. Next, we restore the signal and noise transfer functions. A 4th-Order Wideband delta-sigma modulator have been designed and simulated to verify the method.

Keywords: *sigma-delta, wideband, linear system theory*

1. Introduction

With the growth market for wired and wireless communication systems, various electronics and applications increase the demand for high resolution sigma delta modulator ADCs. For example, the global system for mobile communications (GSM) has become the most popular standard for mobile communications all over the world, and analog-to-digital converters (ADCs) are one of the key modules in a GSM system. There are two realizations of $\triangle\sum$ modulators. One is based on continuous-time (CT) circuitry. Due to their inherent anti-aliasing filtering performance and higher permissible frequency, CT sigma delta modulators are widely used to realize ADCs with 10MHz or wider bandwidths [1]. The other one is discrete-time (DT) switched-capacitor (SC) circuitry, which is used to achieve very high resolution with low bandwidth. In order to expand the bandwidth of DT SC sigma delta modulators, we have many to do with the structure.

There are many architectures and design topologies for $\triangle\sum$ ADCs. As for the topologies, cascaded architectures have displayed advantages in high-resolution and wideband applications, but more power and die area are consumed by more stringent matching and integrator leakage requirements. And continuous time implementations are appropriate due to their high speed, but clock jitter, excess loop delay and a large time constant shift restrict their available resolution [2]. For the purpose the high resolution requirements where some applications require the resolution of above 14 bits [3], we select discrete time sigma delta modulator. DT $\triangle\sum$ ADCs can also achieve 10 to 20MHz bandwidth [4] if some techniques such as double sampling [5] and extra loop delay could be used. The feed-forward structure with low distortion [6] has also been used in modulators because in those loop filter processes only the quantization for all integrators are relaxed, especially when using a multi-bit quantizer. For a high speed $\triangle\sum$ ADC in wideband applications, the time of feedback dynamic element matching becomes critical becomes only the non-inverting time between the sampling and holding period are used for feedback DAC. This paper is to solve the stability of $\triangle\sum$ modulator when added a

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extra delay and restore the signal and noise transfer function to retain low-distortion characteristics.

This paper is organized as follows: a design technique using linear system theory is proposed to solve stability issues for $\triangle\sum$ ADCs with extra loop delay in Section 2. Section 3 explains the procedure for loop filters with maximally flat noise transfer function (NTF) and for pole/zero optimized NTF of the 4th-order wideband sigma-delta modulator. The MATLAB model and the simulation results to verify the effectiveness are described in Section 4. Finally, conclusions are briefly given in Section 5 and Section 6 gives the acknowledgements.

2. Proposed Technique to Compensate the Introducing the Extra Delay

The conventional 4th-order feed-forward sigma-delta modulator is shown in Figure 1. It is so-called cascade of integrators feed-forward form (CIFF) [7]. From the Figure 1, we can see that there are obvious drawbacks in this structure. Although the feedback DAC timing constraint is greatly relaxed by using 1-bit DAC, in a high speed modulator, the additional long processing time of the signal in the quantizer would greatly alter the STF and NTF, resulting in a decrease in performance. Even if we do not use a multi-bit quantizer, we must introduce an extra delay in the modulator. If we use double-sampling $\triangle\sum$ ADCs, a delay phase in DAC feedback path means a full cycle extra delay in loop filters.

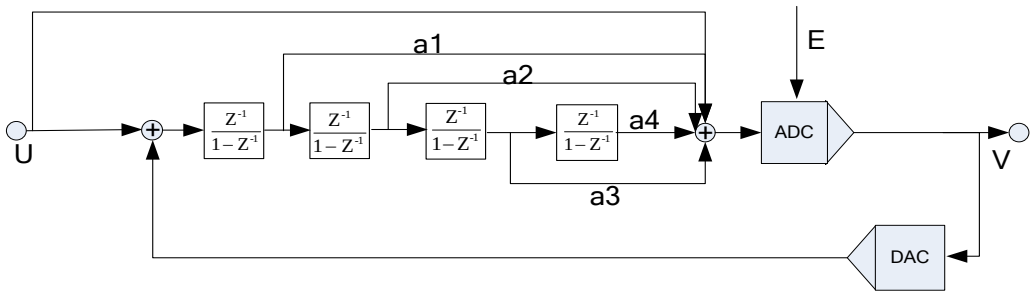


Figure 1. Block Diagram of a Conventional 4th-order Feed-Forward Sigma-Delta Modulator

For the $\triangle\sum$ ADC with a maximally flat noise transfer function, each integrator is a delay one. And the loop filter transfer function $H(z)$ in Figure 1 is given by

$$H(z) = \sum_{i=1}^{4} a_i \left(\frac{z^{-1}}{1 - z^{-1}} \right)^i \quad (1)$$

If we add a full-cycle delay in the feedback loop, which is also called the feedback DAC path, the order of the loop filter increase by one. And the resulting noise transfer function $NTF(z)$ becomes

$$NTF(z) = \frac{z(z-1)^4}{z(z-1)^4 + \sum_{i=1}^{4} a_i (z-1)^{4-i}} \quad (2)$$

In Figure 2 gives the pole/zero locations for a conventional 4th order $\triangle\sum$ ADC. Checking the pole/zero locations of the new $NTF(z)$ and compared with the conventional 4th order $\triangle\sum$ ADC with $NTF(z) = (1 - z^{-1})^4$, the additional zero is located at the origin while the four complex conjugate poles move out of the unit-circle. We can conclude that the extra delay induces instability in the $\triangle\sum$ ADC.

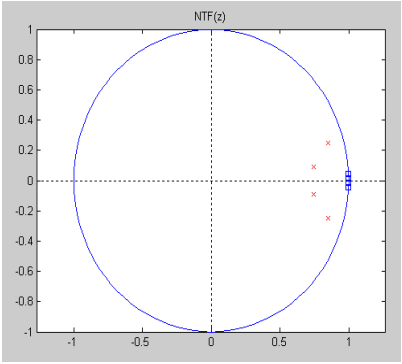


Figure 2. The Pole/zero Locations of the Conventional 4th Order CIFF Structure

The instability caused by the extra delay can be solved by some techniques. We can adjust the coefficients of the feed-forward paths after introducing the extra delay to make the system stable. From the equation (2), we can get that there are only four independent coefficients for the five order loop filter. So the system is not controllable, and it is impossible to adjust the coefficients to match the desired NTF unless an independent variable is added. For example, we add the extra delay in the feedback path, showed in the Figure 3. In order to match the output signal of the filter and other feed-forward signal, the value of the gain for the additional independent branch should be assumed reasonable. Next step is to how to decide that value and the instability issue can be explained using linear system theory [8].

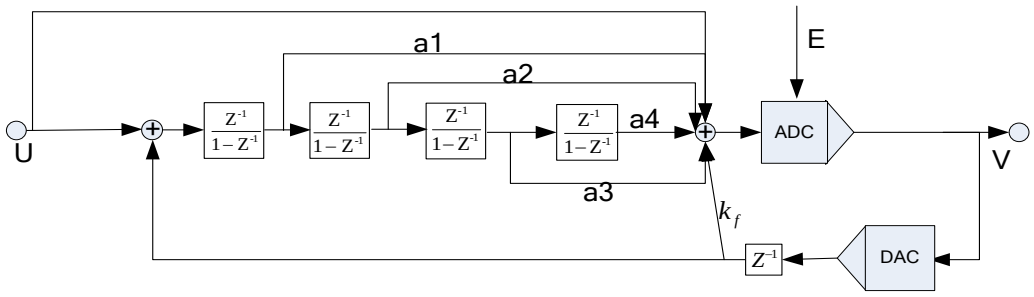


Figure 3.The Modified Structure with Addition of an Extra Delay

3. Procedure of the Loop Filter Design and Implementation of the Proposed Structure

3.1. Procedure of the Loop Filter Design

The instability issue of the additional extra delay can be solved by using linear system theory. In order match the coefficients of the conventional structure in Figure 1 and the modified structure in Figure, it requires

$$\sum_{i=1}^{4} a_i \left(\frac{z^{-1}}{1-z^{-1}} \right)^i = z^{-1} \left[k_f + \sum_{j=1}^{4} b_j \left(\frac{z^{-1}}{1-z^{-1}} \right)^j \right]$$

(3)

Here we assume that

$$I(z) = \frac{z^{-1}}{1-z^{-1}}$$

(4)

And hence

$$z^{-1} = \frac{I(z)}{1+I(z)}$$

(5)

Therefore, equation (3) can be re-arranged as

$$(I(z)+1)\left[\sum_{i=1}^{4} a_i I(z)^i \right] = I(z)\left[k_f + \sum_{j=1}^{4} b_j I(z)^j \right]$$

(6)

We can get a matrix notation as bellows:

$$\begin{bmatrix} a_1 \\ a_1 + a_2 \\ a_2 + a_3 \\ a_3 + a_4 \\ a_4 \end{bmatrix}^T \begin{bmatrix} I(z) \\ I^2(z) \\ I^3(z) \\ I^4(z) \\ I^5(z) \end{bmatrix} = \begin{bmatrix} k_f \\ b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}^T \begin{bmatrix} I(z) \\ I^2(z) \\ I^3(z) \\ I^4(z) \\ I^5(z) \end{bmatrix}$$

(7)

So we get the follow equations:

$$a_1 = k_f$$

(8)

$$a_i + a_{i+1} = b_i, i < 4$$

(9)

$$a_4 = b_4$$

(10)

Using the above equations, we can get the modified structure's feed-forward coefficients. It can also be applied to feed-back structures.

After solving the problem caused by introducing the extra delay, it begins to consider the signal and noise transfer function. As we all know, the unity-STF [9] sigma delta modulator which is the so-called cascade of integrators feed-forward form has the low distortion property. In wideband sigma delta applications, low distortion is selected to reduce the design requirements of op-amps and we get a wider frequency band above 1MHz.

If we design a low distortion sigma delta modulator, the modified structure changes the signal transfer function, which is not unity. In order to get a unity STF, we must add some

branch to compensate the modified coefficients. The follow is the new loop filter transfer function without the k_f branch in Figure 2, given by

$$H_1(z) = \sum_{i=1}^{4} b_i \left(\frac{z^{-1}}{1 - z^{-1}} \right)^i$$

(11)

Assume the extra loop delay in the feedback DAC path and the corresponding $STF(z)$ is

$$STF(z) = \frac{H_1(z)}{1 + k_f z^{-1} + z^{-1} H_1(z)}$$

(12)

To achieve the $STF(z) = 1$, a full-cycle delay block should be added at the modulator input to match the delay at the feedback DAC in addition to the direct feed-in branch at the adder. Another coupling branch which also has gain value of k_f is added to the adder before the quantizer to mach the feedback k_f branch [10]. The resulting $STF(z)$ is

$$STF(z) = \frac{1 + k_f z^{-1} + z^{-1} H_1(z)}{1 + k_f z^{-1} + z^{-1} H_1(z)} = 1$$

(13)

If the STF is unity, the DAC feedback path delay which is used to implement the DEM circuits could match the delay at the modulator input. If the DEM timing [11] is stringent, the mismatch can cause imperfect cancelling of signal component at the loop filter input and increase the linearity requirements of the modulator. Although the DEM timing and modulator input delay can be rightly controlled by clock signal in switched-capacitor $\triangle\Sigma$ ADCs, the insufficient speed of switched-capacitor can introduce gain error at the DAC feedback path and it should be avoided in actual realization.

It is known that the sampling frequency is usually limited by the available process, and the largest oversampling ratio of the $\triangle\Sigma$ ADC is low in wideband applications. The noise shaping can not fully depend on the improved oversampling ratio. Pole and zero optimization are usually used to enhance the noise shaping. Considering the pole and zero optimization and the extra loop delay within the loop, the same technique as was described earlier can be used to stabilize the loop. In this case, we consider one pair pole and zero optimization for 4th order sigma delta modulator. The corresponding loop filter transfer function is

$$H(z) = \sum_{i=1}^{2} a_i \left(\frac{z^{-1}}{1 - z^{-1}} \right)^i + \frac{1}{1 + gI^2(z)} \sum_{j=3}^{4} a_j \left(\frac{z^{-1}}{1 - z^{-1}} \right)^j$$

(14)

And the loop filter function with the extra delay is given as

$$H^{'}(z) = z^{-1} \times \left(k_f + \sum_{i=1}^{2} b_i \left(\frac{z^{-1}}{1-z^{-1}} \right)^i + \frac{1}{1+gI^2(z)} \sum_{j=3}^{4} b_j \left(\frac{z^{-1}}{1-z^{-1}} \right)^j \right)$$

(15)

The corresponding matrix notation about equation 14 and equation 15 is

$$\begin{bmatrix} a_1 \\ a_2 + a_1 \\ a_3 + a_2 + ga_1 \\ a_4 + a_3 + g(a_2 + a_1) \\ a_4 \end{bmatrix}^T \begin{bmatrix} I(z) \\ I^2(z) \\ I^3(z) \\ I^4(z) \\ I^5(z) \end{bmatrix} = \begin{bmatrix} k_f \\ b_1 \\ b_2 + gk_f \\ b_3 + gb_1 \\ b_4 \end{bmatrix}^T \begin{bmatrix} I(z) \\ I^2(z) \\ I^3(z) \\ I^4(z) \\ I^5(z) \end{bmatrix}$$

(16)

To match the H(z) and H'(z), we can get similar equations like equation (8) to (10). Considering the pole and zero optimization [12], we can also calculate the coefficients of the modified structure by making the variables in the matrix notation to be equal. The same conclusion can be easily extended to $\triangle\Sigma$ ADC using general multi pair pole and zero optimization.

3.2. Implementation of the Proposed Structure

To verify the proposed techniques, a 4th order wideband sigma delta modulator is proposed. Figure 1 shows a conventional cascade of integrators feed-forward structure. Since the DEM block can only be implemented with the non-overlapping interval between two clock phases, the oversampling ratio of the structure should not be larger in the high speed applications.

Figure 4 shows the modified block diagram of a low distortion sigma delta modulator. The first integrator of the loop filter becomes a delayed integrator because of added an extra one-cycle delay in the feedback path. The DEM timing is greatly relaxed and improves the linearity of the multi-bit feedback DAC. The more time is given to implementation of DEM algorithms such as data weight average (DWA) [13]. The corresponding coefficients can be obtained by the matrix notation (16), considering pole and zero optimization. So the modified structure's linearity is improved and the signal to noise ratio (SNR) is also larger than conventional structure because of the improved linearity of the feedback DAC.

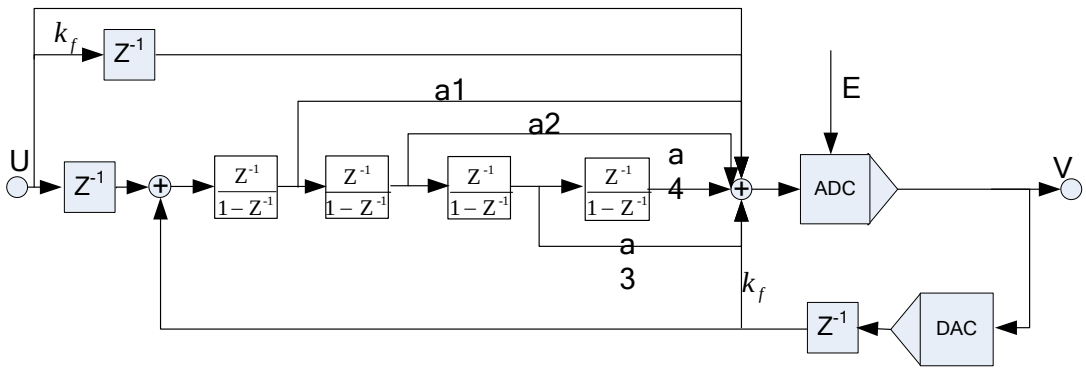


Figure 4. Block Diagram of a 4th-order Feed-Forward Sigma-Delta Modulator

In Figure 4, we can also consider low distortion. Because the appreciation of wideband sigma delta modulator, we must adjust the signal transfer function of the modified structure. Just as discussed before, we add one delay before the first integrator to cancel the feedback signal and add one delayed branch to match the feedback k_f branch. Finally, the STF of the modified structure is unity and the modulator behaves low distortion property.

4. The Simulation of the Proposed MATLAB Model

The proposed MATLAB model of the modified structure is shown in Figure 5.

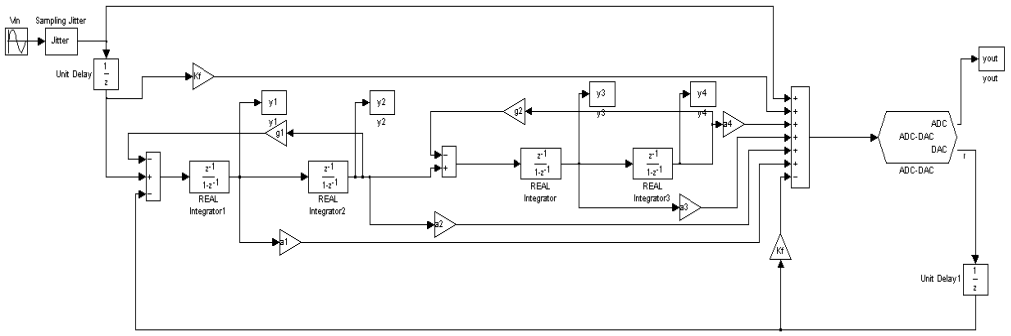
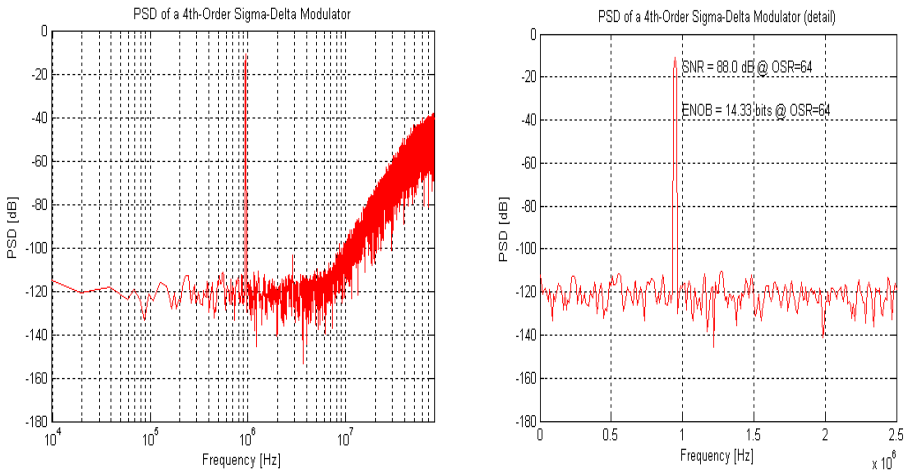


Figure 5.The MATLAB Model of the Proposed Structure

The coefficients of conventional structure can be initialized by the well-known 'delsig' toolbox with an NTF whose maximum out-of-band gain is 1.5 for stability [14]. Then equivalent transformations based on the proposed linear design technique and restore the STF to make it to be unity. Finally, the scaling of internal nodes' signal swings was performed and all coefficients were processed by rational approximations in order for switched capacitor circuit implementation except for the two too small ones g1 and g2.

The structure can be applied to multi-bit quantizer and the modified Lee's approximate criterion [14] could be used to estimate stability. One rule is to make the NTF not larger than 1.5. Figure 6 is the simulation results of the architecture. The input frequency bandwidth is 2.5MHz, and the sampling frequency is 160MHz under 32 oversampling ratio.



(a) (b)

Figure 6. The Simulation Results of the Proposed Structure

The test input frequency is given by the rule that the value of the sampling frequency to the test input frequency is equal to the value of points of the sampling to the numbers of the time period [15]. So the leakage of the signal is less. The input sine with 0.95MHz and the amplitude of -6dBFS is to verify the proposed MATLAB model and the FFT transform is applied to the output of the modulator. With the 16384 points, the SNR is 88dB and the ENOB is 14.33bits. The results shows that the modified structure using the proposed linear system theory technique can be applied to some communication applications, which require that the signal bandwidth is above 1MHz and the bits are greater than 14.

5. Conclusions

The linear system theory technique is used to compensate the insertion of the extra delay into to the loop of a sigma delta modulator. It makes the implementation of multi-bit feedback DAC easier than conventional structure. And in order to design a higher input bandwidth, low distortion techniques are also described that the STF must be unity to make the integrator only process the quantization noise. Finally, a 4th wideband sigma delta modulator is proposed to verify the method. From the MATLAB simulation results, the presented ideas can reduce the speed requirements and provide more flexibility in the design of sigma delta ADCs.

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References

[1] V. Singh, N. Krishnapura, S. Pavan, B. Vigraham, N. Nigania and D. Behera, "A 16MHz BW 75dB DR CT $\Delta\sum$ ADC Compensated for More Than One Cycles Excess Loop Delay", IEEE Custom Integrated Circuits Conference, **(2011)**.
[2] Y. Jun, Z. Zhaofeng, W. Jun, W. Chao, C. Zhenhai, Q. Wenrong and Yangtang, "Continuous time sigma delta ADC design and non-idealities analysis [J], Journal of Semiconductors, vol. 32, **(2011)**.
[3] S. C. lu, X .B. Song and J. Wang, Desing of high-precision data acquisition card based Lan [J], Joural of harbin university of science and technology, vol. 23, **(2012)**.
[4] P. Malla, H. Lakdawala, K. Kornegay and K. Soumyanath, A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT $\Delta\sum$ ADC for 802.11m/WiMAX Receivers, IEEE International Solid-State Circuits Conference, **(2008)**.
[5] J. Chae, S. Lee, M. Aniya, S. Takeuchi, K. Hamashita, P. K.Hanumolu and G. C. Tems, "A 63dB 16mW 20MHz BW Double-Sampled $\Delta\sum$ Analog-to-Digital Converter with an Embedded-Adder Quantizer", IEEE Custom Integrated Circuits Conf, **(2010)** September.
[6] J. Silva, U. Moon, J. Steensgarrd and G. C. Temes, "Wideband low-distortion Sigma Delta ADC topology [J]. Electron, Lett., vol. 12, no. 737, **(2001)**.
[7] R. N. Stenven, S. Richard and C. T. Gabor, "Delta sigma data converters", IEEE Press, New York, **(1996)**.
[8] C. T. Chen, Linear System Theory and Design, 3rd ed. Pxford, U.K.Oxford Univ. Press, **(1988)**.
[9] Second H. San, H. Konagaya, F. Xu, A. Motozawa, H. Kobayashi, K. Ando, H. Yoshida and C. Murayama, "Second-Order $\Delta\Sigma$ Modulator with Novel Feed-forward Architecture", 50th Midwest Symposium on Circuits and Systems, Montreal, Canada, **(2007)** August 5-8.
[10] K. Lee and G. C. Temes, Improved low-distortion $\Delta\Sigma$ ADC topology, IEEE International Symposium on Circuits and Systems, Taipei, Taiwan, **(2009)** May 24-27.
[11] A. Gharbiya and D. A. Johns, "On the implementation of input feed-forward delta-sigma modulators [J]", IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 6, no. 453, **(2006)**.
[12] J. Steensgaard, Nonlinearities in sc delta sigma ad converters, Proc IEEE ICECS, **(1988)**.
[13] R. T. Baird and T. S. Fiez, "Linearity Enhancement of Multi-bit $\Delta\sum$ AD and D/A Converters Using Data Weighted Averaging", IEEE Transactions on Circuits and Systems II, **(1995)**.
[14] S. Richard, C. T. Gabor, Understanding delta sigma delta converters, IEEE Press, New York, **(2005)**.
[15] L. Lu, S. Ying, H. Yan, L. Guo, L. Hao and L. XiaoPeng, "A 65-nm low-power high-linearity $\Delta\sum$ADC for audio applications[J]", Science Chia, vol. 4, **(2014)**.

