

## A 4th-Order Low-distortion Low-pass $\Sigma\Delta$ Modulator Using Timing-Sharing Technique

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### Abstract

A 4th-Order low-distortion low-pass  $\Sigma\Delta$  modulator structure is proposed in this paper, which uses the timing-sharing between the 3rd and 4th integrators during one clock phase. Compared with conventional cascade of integrators with distributed feed-forward (CIFF) sigma-delta modulator structure, the proposed structure not only solves the critical timing issue for the quantizer and feedback DAC path, but also eliminates an extra active adder to sum up the input feed-forward. By methods of delay redistribution structure, the time for quantization and feedback dynamic element match (DEM) operation can be extended from a non-overlapping interval for a conventional low-distortion structure to half of the sampling clock period. Capacitive input feed-forward (CIF) methodology eliminates the adder in front of the quantizer. Further, the op-amp of the last integrator is used as an active adder by op-amp sharing. Therefore, the power consumption can be reduced and the linearity of the feedback DAC is improved because of the increasing time which used for implementation of DEM algorithm. The proposed 4th-Order low-distortion low-pass  $\Sigma\Delta$  modulator with 4-bit quantizer is simulated in MATLAB. From the simulation results, the proposed structure can achieve a peak SNR (signal-to-noise ratio) of 87dB with 2.5MHz bandwidth under 32 oversampling ratio at 160MHz sampling frequency and the ENOB of 14.234bits in non-ideal condition.

**Keywords:** low-distortion, low-pass, time-sharing, sigma-delta, differential sampling, dynamic element match

### 1. Introduction

With the development of CMOS process with the increasing sampling rate, bandwidth of sigma-delta modulator is growing and has become one of the choices for wide-bandwidth high-resolution wired and wireless communications [1, 2]. To achieve high resolution and linearity, 1MHz bandwidth and 12bit resolution, it is a more challenging work. The main tendency in sigma-delta modulator is to achieve higher power efficiency and resolution that are conflict condition [3]. Until now, different modulator structures are designed to improve performance and every structure has advantages and shortcomings. There is not an optimal structure to achieve every specification and there are many challenges in design of low intrinsic gain of transistor and lower supply voltage in advance process. Therefore, improvement of sigma-delta modulator architecture is one of the most important topics in analog-to-digital filed [4].

Low-distortion sigma-delta modulator is one of a power efficient topology. It was invented to relax the specifications of the op-amp used in integrator, such as the output swing and the slew rate [5]. Only the quantization noise is processed in the loop filter, this allows lower output swing of integrators and reduce the slew rate requirement for op-amps. But there are some challenge in designing low-distortion, such as the timing

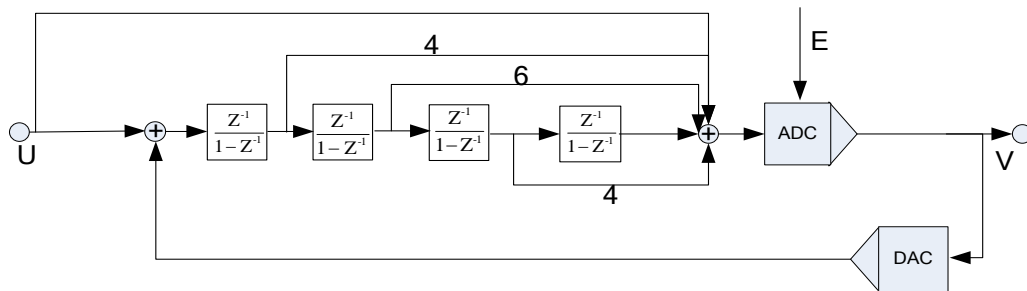
limitation on the feedback path and the additional power expense for the active. The proposed structure is to solve these issues in conventional low-distortion sigma-delta modulator.

This paper is organized as follows: The proposed 4th-order sigma-delta modulator topology is discussed and in section 2. The MATLAB model implementation is described in section 3. Section 4 shows the simulation results. Finally, conclusions are briefly given in section 5 and Section 6 gives the acknowledgements.

## 2. Proposed 4th-order Sigma-delta Modulator Topology

### 2.1. Modulator Architecture

The conventional 4th-order low-distortion sigma-delta modulator is shown in Figure 1. This structure is expanded from low order low-distortion sigma-delta modulators which were proposed [6]. From the Figure 1, we can see obviously that the adder in front of the quantizer must be constructed with a power op-amp because of many input feed-forward paths assembled at the quantizer input. To achieve the wider bandwidth and high resolution, we may increase the level of the quantizer because the system may be easy to unstable by increasing the modulator order purely.



**Figure 1. Conventional 4th-order Low-distortion Sigma-delta Modulator**

From the Figure 1, we get following equations:

$$Y(z) = X(z) + (1 - z^{-1})^4 E(z) \quad (1)$$

Here  $X(z)$  is input signal,  $Y(z)$  is output signal and  $E(z)$  is quantization noise of the modulator. Then the signal transfer function ( $STF$ ) and noise transfer function ( $NTF$ ) of the modulator are given by

$$STF(z) = 1 \quad (2)$$

$$NTF(z) = (1 - z^{-1})^4 \quad (3)$$

From the equation (2) and equation (3), the STF is unity and not delayed. The NTF provides a four-order noise-shaping function for the quantization noise of the modulator.

We can get a conclusion that the architecture showed as in Figure 1 is an effective architecture for design high-linearity and high resolution application. But it needs to deal with critical timing constraints for more level of quantizer and feedback DAC paths. Besides, the active adder for summing feed-forward inputs increases the power consumption. Hence, several methods are proposed to improve these issues.

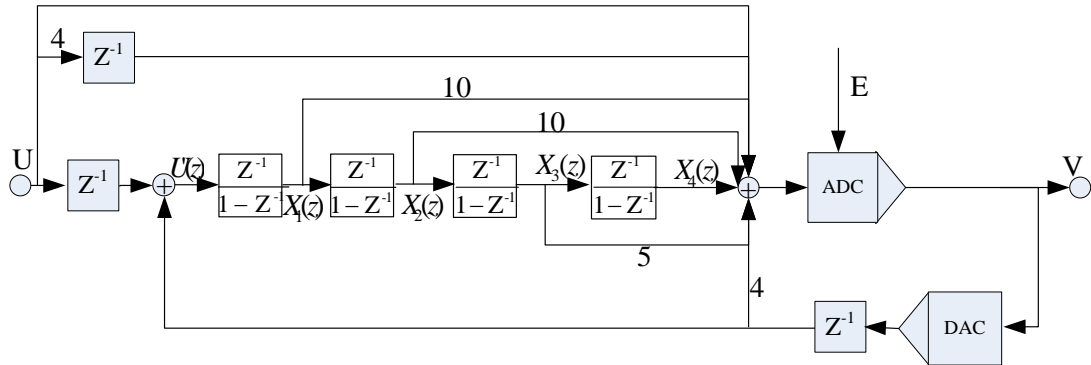
An improved architecture for low-distortion sigma-delta ADCs is presented in [7]. It relaxes the critical timing constraints of the SDM and also removes the active adder at the quantizer input. But integrators of the SDM need more strict specifications to process the feed-forward input signals that consume more power, such as double-sampling technology [8].

Another modulator topology also relaxes the critical timing constraints in the modulator feedback path in [9], the speed requirement of the quantizer and DEM logic can be greatly reduced. Besides, integrators can reduce power consumption because op-amps only need to process quantization noise. But this topology still need extra active adder to sum up signals in front of a quantizer. In turn, the total power consumption increases. Our work is to solve two issues: the critical timing constraints and removing the active adder.

Improved low-distortion modulator in [7] improves the above mentioned issues. It holds the unity signal transfer function (STF), greatly relax DEM issue and does not use an adder. It is learned that delay redistribution structure (DRD) and capacitive input feed-forward (CIF) are two essential methods to achieve this topology [10]. Delay redistribution structure (DRD) is used to relax DEM timing. The principal of this methodology is to create a delay in DEM path by this extra delay. Adding an extra delay in input, redistribution this delay contributes a delay in the feedback timing path. A whole delay time is increased to deal with DEM. Capacitive input feed-forward (CIF) methodology is to create only input feed-forward path to the input of last integrator of loop filter. Then move the input feed-forward path at the quantizer input to the input of the last integrator and multiplies the input feed-forward  $1 - z^{-1}$  times. So, there is no need a adder to sum the input feed-forward at the front of the quantizer.

There are two steps to build our novel architecture. First step is to modify third order sigma-delta modulator [11] with relaxed feedback timing into fourth order. Second step is to move the summing node at the input of the quantizer to the last integrator.

The proposed 4th-order low-distortion sigma-delta modulator is derived in Figure 2. This structure is based on third order modulator. To conduct this topology, coefficients and path match up to maintain the unity STF and the fourth order shaped NTF. These paths are added to create quantization noise in the modulator in equation. Following is the equation of this structure.



**Figure 2. The Proposed 4th-order Low-distortion Sigma-delta Modulator**

$$U + 4z^{-1}(U - V) + (U - V)z^{-1} \left[ \left( \frac{z^{-1}}{1 - z^{-1}} \right)^4 + 5 \left( \frac{z^{-1}}{1 - z^{-1}} \right)^3 + 10 \left( \frac{z^{-1}}{1 - z^{-1}} \right)^2 + 10 \left( \frac{z^{-1}}{1 - z^{-1}} \right) \right] + E = V \quad (4)$$

$$U \cdot \frac{1}{(1 - z^{-1})^4} + E = V \frac{1}{(1 - z^{-1})^4} \quad (5)$$

$$STF(z) = \frac{V}{U} = 1, NTF = \frac{V}{E} = (1 - z^{-1})^4 \quad (6)$$

In equation (6) shows unity STF and the fourth order shaped NTF. In coordination with paths and coefficients in equation (4) create the fourth order modulator in Figure 2. The improved structure relaxes the DEM timing issues. We can find that there is one clock delay in the feedback path. We can get the following equations.

$$U'(z) = -z^{-1}(1 - z^{-1})^4 E(z) \quad (7)$$

$$X_1(z) = -z^{-2}(1 - z^{-1})^3 E(z) \quad (8)$$

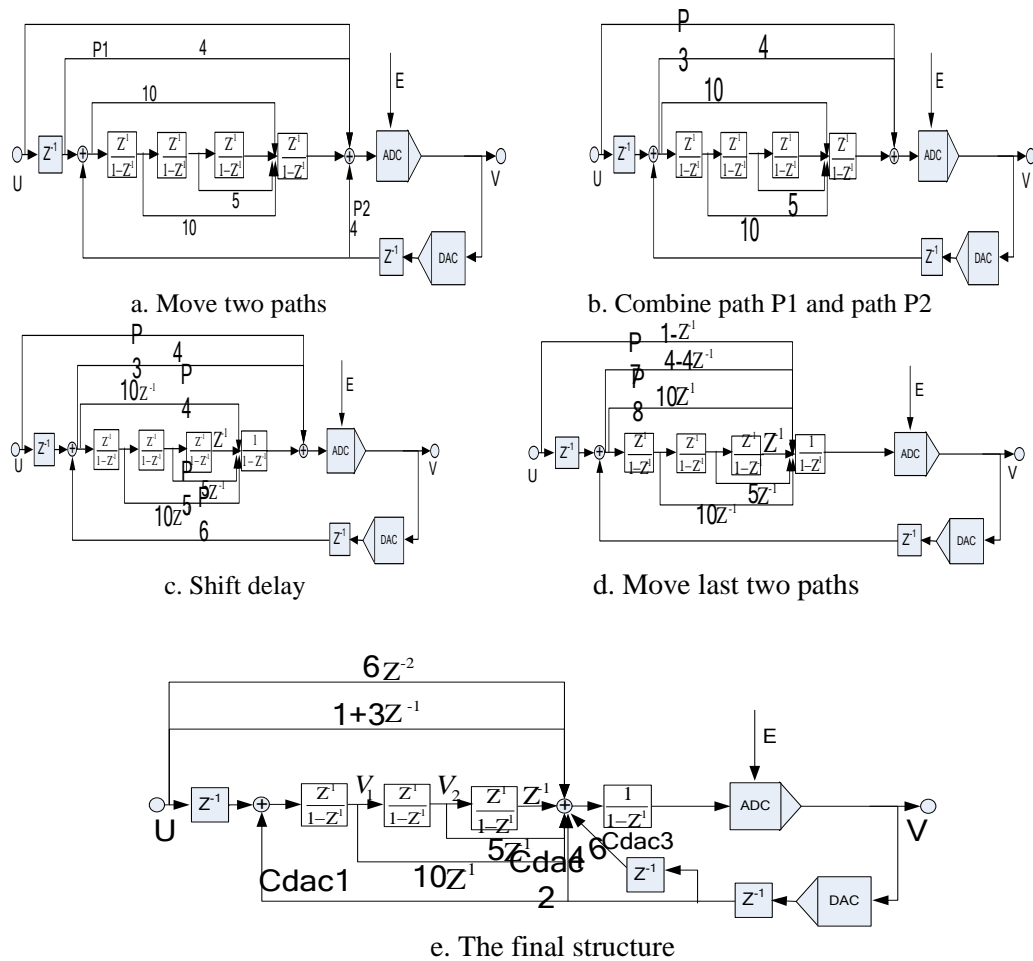
$$X_2(z) = -z^{-3}(1 - z^{-1})^2 E(z) \quad (9)$$

$$X_3(z) = -z^{-4}(1 - z^{-1})^1 E(z) \quad (10)$$

$$X_4(z) = -z^{-5} E(z) \quad (11)$$

In equation (8), we can see that the output signals of four integrators  $X_1$ ,  $X_2$ ,  $X_3$  and  $X_4$  are free of the input signal  $U$ , which means that the proposed 4th sigma-delta modulator keeps the quantization noise in loop filters only.

The next step is to move the summing node at the quantizer input to the front of last integrator, which means takes away an additional active adder. Because of many paths in front of the quantizer, it is necessary to remove these paths step by step.



**Figure 3. Step to Build the Proposed Low-distortion Sigma-delta Modulator**

Figure 3 (a) is the result of moving two paths in the Figure 2. The delay input feed-forward path P1 shares the input delay and the two paths are moved from the front of the quantizer to input of last integrator. Path P1 and Path P2 in Figure 3 (a) can be combined to path P3 in Figure 3 (b). Because both paths P1 and P2 are signals with a delay cycle and three times coefficients. The next step is to shift the delay in the last integrators to path P4, path P5 and path P6 in Figure 3 (c). Move the last two paths at the front of quantizer to the last integrator input. But these two paths need to multiply a factor  $1 - z^{-1}$ , showed in Figure 3 (d). The path P7 and path P8 in Figure 3 (d) can be combined into one path. But this path connects to the DAC path in first integrator, the DAC path minuses signal in

the same integrator hold phase. It can't realize this function because the capacitor can't save signal at the hold phase. So this path is shifted back to the input path and feedback path [6] for feasible implementation. Then, the final structure presents in Figure 3 (e).

Analysis on the proposed sigma-delta structure in Figure 3 (e) and we can get following equations.

$$V_1(z) = (U - V) \cdot z^{-1} \cdot \frac{z^{-1}}{1 - z^{-1}} \quad (12)$$

$$V_2(z) = (U - V) \cdot z^{-1} \cdot \left( \frac{z^{-1}}{1 - z^{-1}} \right)^2 \cdot z^{-1} \quad (13)$$

From equation (12) and equation (13),  $V_1$  is one-order shaped quantization noise and  $V_2$  is two-order shaped quantization noise. It is not hard to prove that the last two integrators can also only process quantization noise. And the proposed architecture sums up the signal by last integrator, a non-delay op-amp. Besides it also retains the advantage of low-distortion sigma-delta modulator [9].

## 2.2. Timing

The time in DAC feedback loop can be as long as a whole phase. And it is necessary to verify the proposed sigma-delta modulator structure offering sufficient processing time for the quantizer and the DEM logic. The timing diagram of the proposed 4th-order low-distortion sigma delta modulator is presented in Figure 4. The input signal delays one cycle and integrates in first integrator in the next phase two. After holding signal in second integrator and third integrator, a delay accompanies with it. As a result, in the fourth integrator, a non-delay integrator, signal samples and integrates simultaneously in the phase one. To send signal into the quantizer and the DEM logic, the circuits needs to accomplish until the end of the phase two. It is greatly longer than non-overlapping time interval in conventional low-distortion sigma-delta.

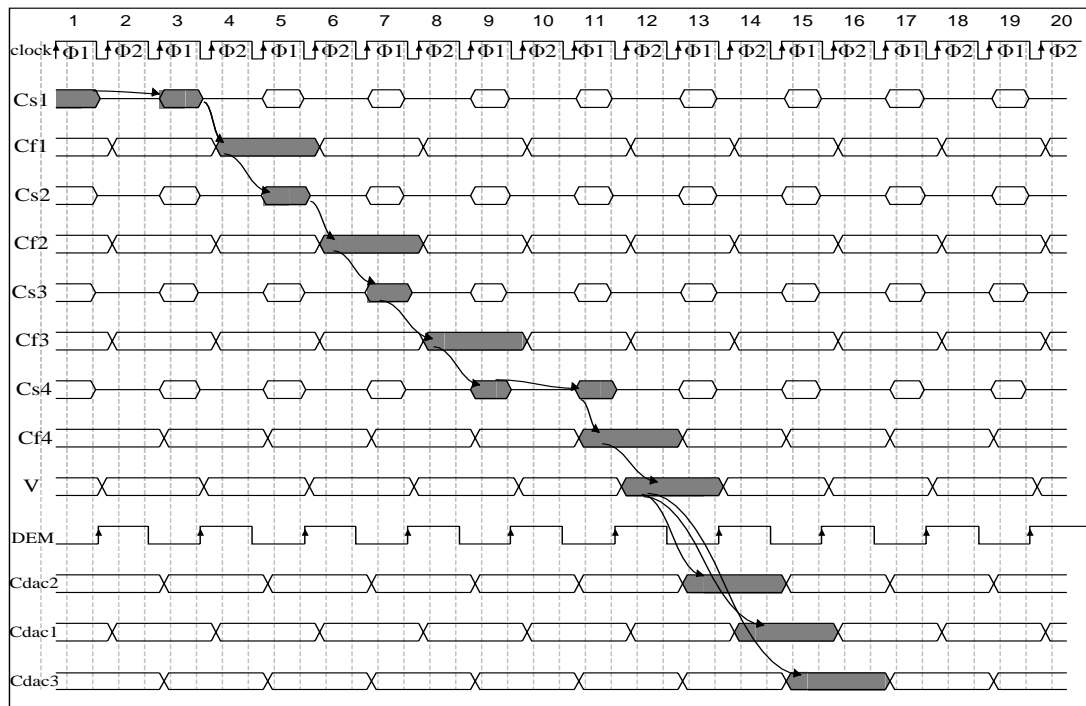


Figure 4. Timing Diagram of the Proposed 4th-order low-distortion SDM

Besides, the DAC paths sum up signal in different phases because the fourth integrator holds signals in the phase one and first integrator keeps signals in the phase two. CDAC2 signal minus the signal in the phase one. CDAC1 is in the phase two and CDAC3 is in the next phase one. It is evident that the proposed 4th-order low-distortion sigma-delta modulator provides enough time for quantization and feedback DAC circuits.

### 3. Implementation of the Proposed Architecture

#### 3.1. MATLAB Simulation

Because the proposed architecture has the advantages of low-distortion, which only process the quantization noise in loop filters. It reduces the requirements of the op-amp. We can build two MATLAB models that one's integrators are composed of ideal op-amp and the other's integrators are composed of non ideal op-amp, such as the sample jitter noise, KT/C noise and op-amp noise. We can compare the results of the two models to prove that the proposed architecture actually relaxes the specifications of the op-amp used in the integrator.

The ideal MATLAB model of the proposed architecture is presented in Figure 5. All integrators are ideal. The structure of the MATLAB model is same as that showed in Figure 3 (e). The coefficients of the input feed-forward path are also equal. An input sine wave signal with amplitude of -6dBFS and frequency of 0.947 MHz is used to verify this structure with 2.5MHz bandwidth under 32 oversampling ratio at 160MHz sampling frequency. FFT transform is applied to the output of the modulator. And 16384 points displays the SNR of 91.7dB and the ENOB of 14.94 bits. The results are shown in Figure 7 (a).

The non-ideal MATLAB model of the proposed architecture is presented in Figure 6. In this model, the op-amp is not ideal. KT/C noise and op-amp white noise are added to model. Under the same simulation condition with the ideal model, the results are shown in Figure 7 (b). The 16384 points displays the SNR of 87.4dB and the ENOB of 14.23bits.

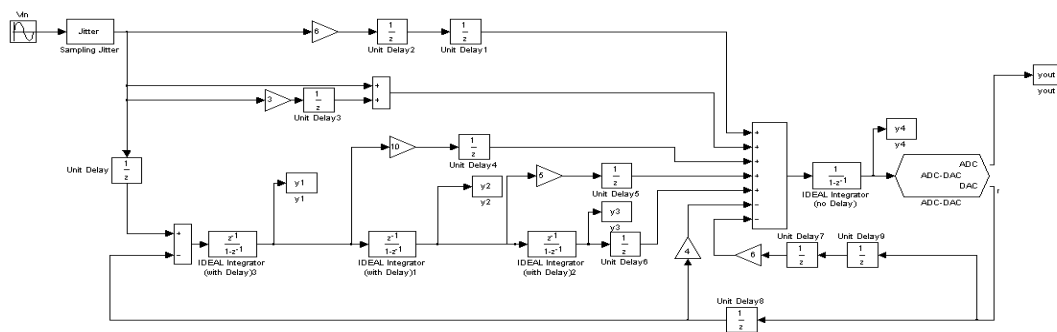
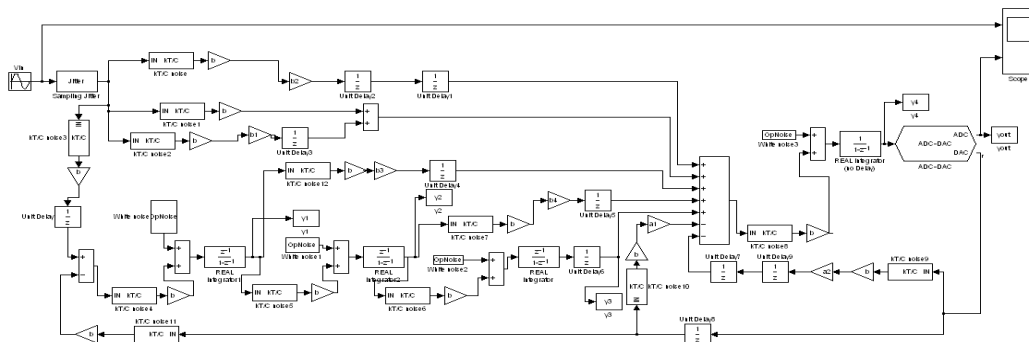
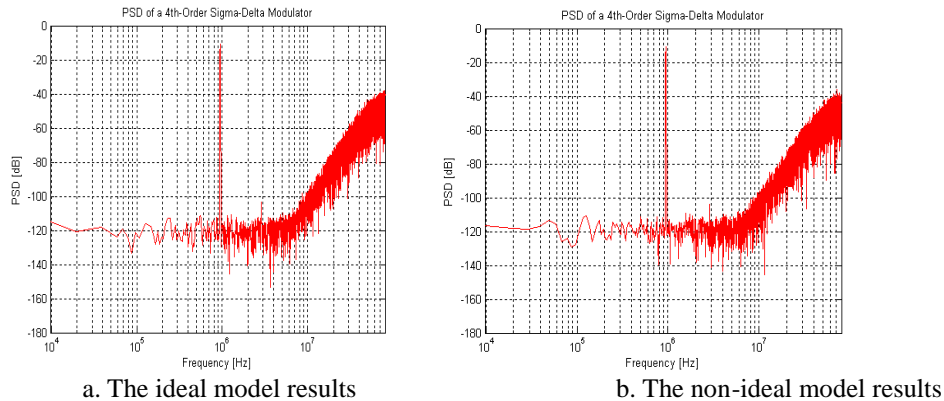


Figure 5. The Ideal MATLAB Model



**Figure 6. The Non-ideal MATLAB Model**



**Figure 7. The Results of the Ideal and Non-ideal MATLAB Model**

Comparing the results in Figure 6 and Figure 8, there are little difference in the ideal and the non-ideal of the proposed architecture. It is easy to verify that the proposed architecture reduces the requirements on loop filter.

### 3.2. Other Similar Structure Performance

A 4th-order 1bit sigma-delta modulator is presented in [12]. It uses signal flow graph to get the STF of the proposed modulator. The SNR of the structure in [12] is 92.8 with 100 KHz bandwidth at 128 oversampling rate under 25.6MHz sampling frequency. The bandwidth is little and the STF is not unity. Only the oversampling rate is large enough that its in-band STF is nearly flat, close to unity. Thus, low-distortion can be hold.

A sigma-delta modulator with shifted loop delays is provided in [13]. It implements the inherent quantization delay by shifting the delay from the last integrator to the quantizer, and it relaxes critical timing for DEM by shifting the delay from the first integrator to the feedback path. A 2nd-order double-sampled sigma-delta modulator is proposed to verify its topology. It was simulated in Cadence SPECTRE. For a double-sampled sigma-delta modulator, OSR=16, the simulated SQNR was 70.2dB. But the STF of the double-sampled SDM is also not unity. It's not sure that the method is good for high order SDM structure.

A 3rd-order 4-bits cyclic-type quantizer is proposed in [14]. All the integrators in this structure share an op-amp. It was simulated with the oversampling ratio of 16 and a sampling range of 80MHz. Simulation results show that the SNR is 81.97dB.

Compared to above three type sigma-delta modulator, the architecture proposed in this paper has some advantages over them. Simulation results showed that the proposed architecture has a wide bandwidth and a high SNR and ENOB.

## 4. Conclusions

In this paper, a 4th-order low-distortion low-pass sigma-delta modulator using time sharing technology is presented. This structure can be used in any bit quantizer modulator. By timing sharing, the critical timing issue of quantization and feedback DAC is solved. As the linearity of feedback DAC is improved, it is a possible that the implementation of high order multi-bit quantizer sigma-delta modulator. By use of the op-amp of the last integrator as active adder, power consumption reduces. Besides, the MATLAB simulation verifies that the proposed DSM topology do achieve high performance.

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