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Design and Implementation of Phase Locked Loop for Break-lock in Monopulse Receivers using Linear Frequency Modulation Interference Signal

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Abstract

In this paper, the break-lock phenomenon of phase locked loop (PLL) in monopulse radar receiver for missile seeking applications is presented. The continuous wave radar echo and linear frequency modulated (LFM) interference signals are injected into the PLL simultaneously with an assumption that initially, the PLL locks on to the echo signal frequency. The PLL is assumed to be operating at an intermediate frequency (IF) of 50 MHz with a typical bandwidth of 200 kHz. The frequency deviation required to break-lock as a function of interference signal power and modulation rate is analyzed. The simulation results show that break-lock is achieved at a frequency deviation of 0.36 MHz for a typical LFM signal power of -14 dBm and 200 kHz modulation rate. The break-lock in the PLL is also estimated for selected values of LFM signal power and modulation rates, such as 300, 400 kHz, when the echo signal power at the PLL input is -10 and -14 dBm. The PLL with third order passive loop filter is modeled and designed using exact method. The computer simulation is carried out using visual system simulator (VSS) AWR software and potential conclusions are demonstrated.

Keywords: *jamming, monopulse, phase lock loop, radar receiver, tracking radar*

1. Introduction

The monopulse is a radar technique used to find the direction of the target by receiving the echo signal with two or more antennas. This technique has become the most successful tracking schemes in missile seeker applications [1]. Jamming of such radar receiver can be achieved either by introducing imperfections in the monopulse design or by using multiple source techniques in order to distort the angle of arrival of the echo signal at the monopulse antenna such that the monopulse tracker is caused to move away from the target that results in break-lock in the missile seeker [2]. Most of the modern missile seekers invariably employ phase locked loop (PLL) as a frequency tracking subsystem in the monopulse radar receivers [3]. The PLL mainly includes a phase detector, loop filter and a voltage controlled oscillator (VCO). When two different signals such as reference input and interference signal are simultaneously applied at the input of the PLL, the loop locks onto the reference input signal so long as the VCO output frequency is exactly equal to the division ratio (N) times the reference input signal frequency. The break-lock is said to occur when the VCO output frequency deviates from reference signal frequency and locked onto interference signal frequency [4]. The effects of interference signal on break-lock in the PLL have been presented in several studies [5-9]. A multiple input multiple output (MIMO) radar system that employs monopulse

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processing at each of the receivers for tracking a moving target have been analyzed in [5]. The statistical parameters of the monopulse receiver and the effects of LFM waveform on tracking accuracy are illustrated in [6]. The maximum likelihood angle estimation technique is analyzed [7-8] for the detection of two closely unresolved targets in the sea clutter environment by implementing modified generalized likelihood ratio. The time-frequency characteristic of non-stationary linear frequency modulated signal [9] is estimated using Wigner Ville Transform to detect the presence of the wrong frequency component.

In this paper, the break-lock phenomenon of the PLL in the presence of continuous wave (CW) linear frequency modulation (LFM) interference signal is illustrated. The objective of the paper to estimate the frequency deviation as a function of interference signal power and modulation rate at break-lock in the PLL. The PLL is designed with a typical bandwidth of 200 kHz and is implemented using visual system simulator (VSS) AWR software. The computer simulation is carried out for selected interference signal power from -14 to -2 dBm with the radar echo signal power at the PLL input are -10 and -14 dBm.

2. System Overview and Modeling

A. Linear FM Generator

The LFM signal is generated by frequency modulating the sinusoidal carrier signal centered at an intermediate frequency (IF) of 50 MHz by a sawtooth waveform of 2 V (peak) using an FM modulator. The block diagram of LFM generator implemented using VSS AWR software is shown in Figure 1.

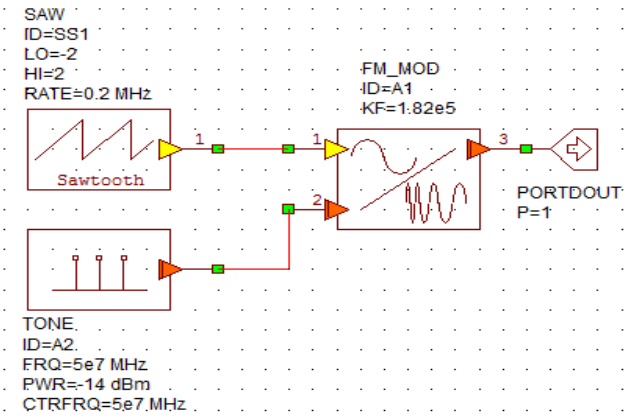

Figure 1. LFM Signal Generation

As shown in Figure 1, the FM modulator block (FM_MOD) frequency modulates the sinusoidal carrier signal (TONE) by the modulating input signal (SAW) and produces baseband LFM signals. The instantaneous frequency of the carrier signal is shifted by an amount equal to the modulating signal times the frequency sensitivity (MHz/volt) of the FM modulator. Specifically, if the modulating input signal is v (t), and carrier has an amplitude (A) with center frequency (f_c), then the output signal, y (t) is given by:

$$y(t) = A \exp[j \bullet (2\pi f_{off} t + 2\pi k_f \int_0^t v(\tau) d\tau)] \quad (1)$$

where, f_{off} is offset frequency from the carrier and k_f is the frequency sensitivity. The LFM signal is generated with following key parameters: modulating voltage (v_m) = 2 V,

modulating frequency (f_m) = 200 kHz, carrier center frequency = 50 MHz, carrier power = -14 dBm. The modulating signal and LFM spectrum are shown in Figure 2. (a) and (b).

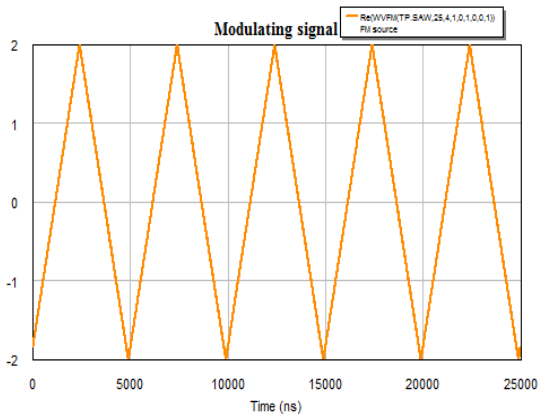

Figure 2. (a). Modulating Signal

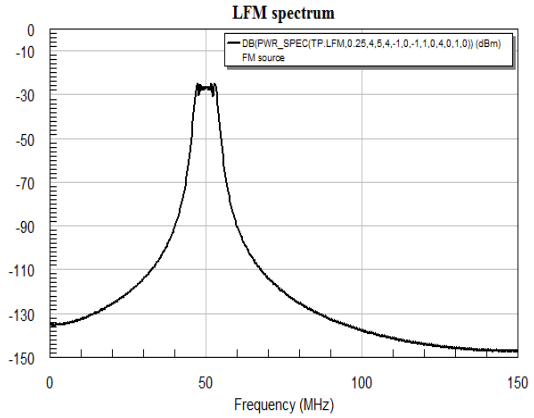

Figure 2. (b). LFM Spectrum

It is seen from Figure 2(a) that the sawtooth signal has an amplitude of 2 volt peak and time period of 5000 nsec with 50% duty cycle. It is depicted from Figure 2(b) that the bandwidth of the LFM signal is approximately 5 MHz centered at 50 MHz.

B. Phase Locked Loop

The monopulse radar receiver invariably employs phase locked loop (PLL) which includes a phase detector (PD), loop filter and voltage controlled oscillator (VCO). Mainly, the PLL includes a charge pump PD as compared to classical voltage phase detector due to the fact that the charge pump provides infinite pull-in range and zero steady state error [10]. The charge pump produces a current by comparing the reference input and the VCO output phase. The PD output current is proportional to the difference in the phase between these two signals. The loop filter impedance when multiplied with this current, the control voltage at the VCO input is obtained. The VCO control voltage controls the output signal phase such that when the phase of these two signals at the phase detector input becomes equal, the PLL locks on to the input reference frequency. When the phase difference at the phase detector input becomes too large, a large error is developed at the phase detector output. Thus, the PLL loses the frequency lock form the initially locked signal. The frequency locking and unlocking of the PLL is characterized by the loop filter.

The loop filter is a crucial element which determines the bandwidth and tracking performance of the receiver loop. For our simulation, a third order passive loop filter is considered due to fact that a third order filer is generally recommended for most of RF applications and it is rare that a PLL is constructed with a filter higher than third order. In addition, the passive loop filter has the advantage over active filter that there is no active device to add noise into the PLL. The loop filter considered is designed using exact method. The exact method of filter design involves with solving the time constants and then determining the loop filter components from these time constants [11]. The different key parameters considered in the design of the loop filter are phase margin (ϕ), loop bandwidth (f_c), phase detector gain (K_Φ in mA), VCO gain (K_{vco} in MHz/volt) and pole ratio (T_{31}). The pole ratio is the ratio of the third order pole and the reference pole of the loop filter. The phase margin determines the loop stability, which is typically chosen between 48 to 55 degrees. The loop bandwidth is the crucial parameter in filter design which determines the spur rejection and lock time of the loop. The selection of pole ratio has an impact on reference spur in the loop. The time constants of filter are determined from phase margin (ϕ) of the loop forward gain [G(s)] given by

$$\phi = \pi + \tan^{-1}(\omega T2) - \tan^{-1}(\omega T1) - \tan^{-1}(\omega T1T31) \quad (2)$$

where, T_1,T_2 and T_3 are the filter time constants. The loop forward gain G(s) is given by:

$$G(s) = \frac{k_\phi \bullet k_{vco}}{S} \bullet Z(s) \quad (3)$$

where, Z(s) is loop impedance, K_Φ is phase detector gain, K_{vco} is gain of VCO. In equation (2), the value of phase margin (ϕ) and the pole ratio (T_{31}) are known, so an equation containing T_1 and T_2 can be obtained. Another equation of T_1 and T_2 can be obtained by finding the maximum value of phase margin at a frequency equal to the loop bandwidth. It is seen that the loop maximizes the phase margin at a frequency equal to loop bandwidth [12]. So, we can write

$$\left.\frac{d\phi}{d\omega}\right|_{\omega=\omega C} = 0 \quad (4)$$

Solving the above equation, we can express

$$\frac{\omega_C T2}{1+(\omega_C T2)^2} = \frac{\omega_C T1}{1+(\omega_C T1)^2} + \frac{\omega_C T3}{1+(\omega_C T3)^2} \quad (5)$$

Now, solving equation (2) and (5) for two unknowns, the time constants T_1 and T_2 can be determined. The time constant T_3 can be obtained by using the relation

$$T3 = T1T31 \quad (6)$$

Once the time constants are determined, the loop filter components are obtained by defining the constants k_1, k_2, k_3 and k_4 given as:

$$k_1 = C_{tot} \quad (7)$$

$$k_2 = (T_1 + T_3) \bullet k_1 \quad (8)$$

$$k_3 = \frac{T_1 T_3 k_1}{T_2} \quad (9)$$

$$k_4 = \frac{C_3}{C_1} \quad (10)$$

By solving the above four equations, the filter components R_1, R_2, C_1, C_2 and C_3 are determined. The typical parameters chosen for the design of the loop filter are: phase margin (ϕ) = 55 deg., input frequency (f_{comp}) = 50MHz, loop bandwidth (f_c) = 200 kHz, VCO output frequency (f_{out}) = 4 GHz, phase detector gain (K_Φ) = 2.5 mA and VCO gain (K_{vco}) = 40 MHz/volt. The filter components are found to be R_2= 1kΩ, R_3= 7.5kΩ, C_1= 100 pf, C_2=2.2 pf and C_3= 15 pf. The loop filter designed by the above method is

introduced into the PLL and the simulation is carried out. The third order PLL implemented using VSS software is shown in Figure 3.

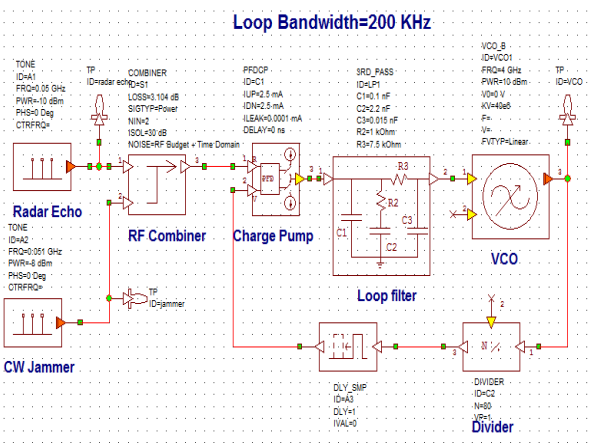

Figure 3. Third order PLL

C. Monopulse Radar Receuver

The monopulse radar receiver implemented using VSS software is shown in Figure 4.

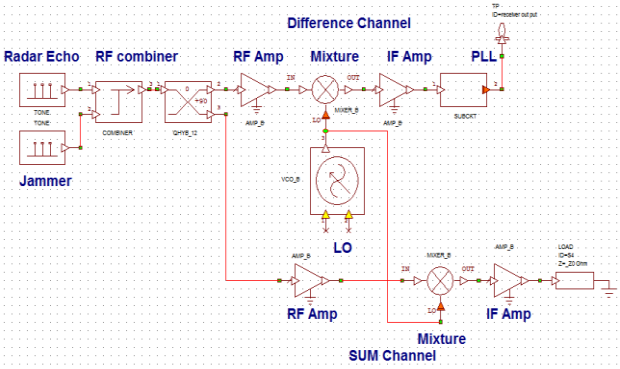

Figure 4. Monopulse Radar Receiver

As shown in the Figure 4, the sinusoidal CW radar echo signal and LFM interference signal are applied at the receiver input simultaneously. The quadrature hybrid coupler at the receiver front end divides the input signal power into sum and difference channel signals, which are 90^0 out of phase to each other. The signals in each channel are then amplified by an RF amplifier and heterodyned to an intermediate frequency centered at 50 MHz. The difference channel signal is applied to the PLL and break-lock in the PLL is studied.

3. Computer Simulation

The computer simulation is performed at IF stage of the receiver with the difference signal at the PLL input. The radar echo signal is assumed to be operating at an IF frequency of 50 MHz with -14 dBm power. The LFM interference signal is centered at an IF frequency of 50 MHz with power of -14 dBm is applied at the PLL input. The VCO output frequency is chosen to be 4 GHz (designed value) with 10 dBm power. Initially, it is assumed that the PLL is locked onto the radar echo signal frequency such that the PLL output frequency is equal to the VCO output frequency (typically 4 GHz). Then the frequency deviation of LFM signal is increased starting with a small deviation. It is observed that when the frequency deviation gets wider than the loop bandwidth (typically 200 kHz), the PLL becomes unstable and loses the frequency lock from the echo signal frequency. The break-lock is observed through the frequency spectrum of the PLL and the

deviation required to break-lock in the PLL is measured as a function of interference signal power. The simulation is also carried out for selected interference signal power from -14 to -2 dBm and different modulation values of rate such as 300 kHz, 400 kHz. The above aspects simulated with the echo signal powers of -14 and -10 dBm.

4. Results and Discussion

The simulation results of break-lock measured through the frequency spectrum of the PLL are shown in Figure 5(a), 5(b) and Figure 6(a), 6(b). The results are presented for a typical LFM signal power of -14 dBm and modulation rate of 200 kHz, when the echo power at the PLL input is -14 and -10 dBm.

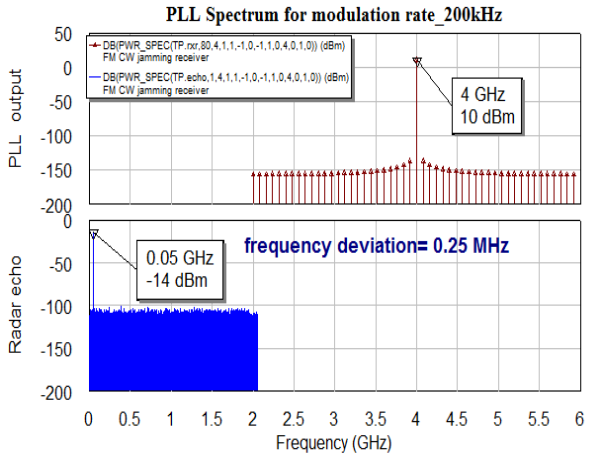

Figure 5. (a) PLL Spectrum at Frequency Deviation of 0.25 MHz and Echo Power of -14 dBm

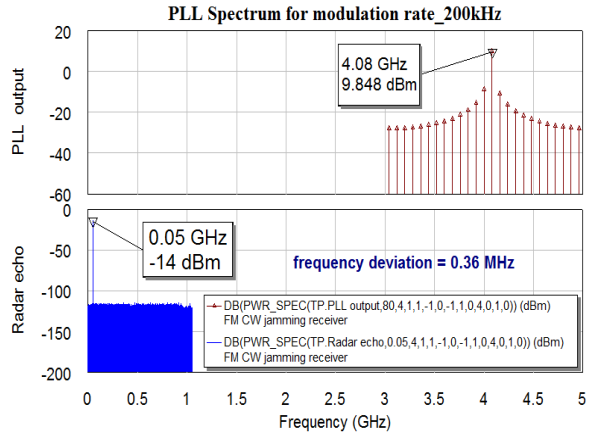

Figure 5. (b) PLL Spectrum at Frequency Deviation of 0.36 MHz and Echo Power of -14 dBm

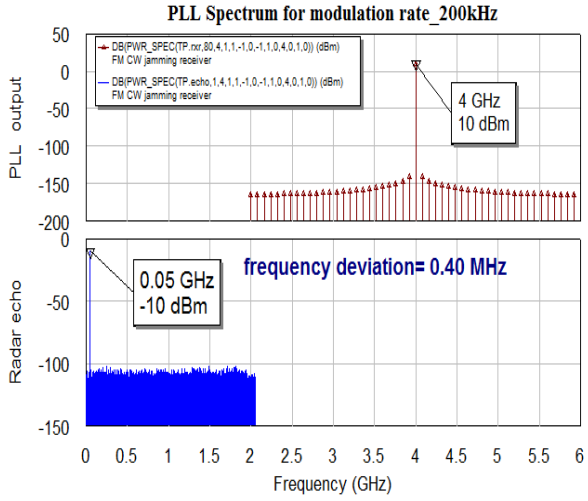

Figure 6. (a) PLL Spectrum at Frequency Deviation of 0.40 MHz and Echo Power of -10 dBm

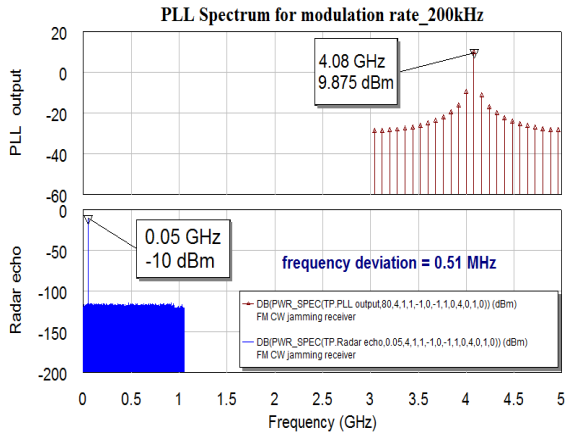

Figure 6. (b) PLL Spectrum at Frequency Deviation of 0.51 MHz and Echo Power of -10 dBm

It is seen from Figure 5(a) that the radar echo power is -14 dBm at 0.05 GHz MHz and the PLL output power is 10 dBm at 4 GHz for a frequency deviation of 0.25 MHz, which demonstrates that the PLL is locked on to the echo signal frequency as the PLL output frequency is equal to the VCO output frequency. From the Figure 5(b), it is seen that the PLL output power is 9.85 dBm at 4.08 GHz for the value of frequency deviation of 0.36 MHz, which reveals that the frequency deviation required to break-lock is 0.36 MHz for the radar echo power of -14 dBm.

Similar simulation results are depicted in Figure 6(a) and (b) for the radar echo power of -10 dBm. It is clear from Figure 6(a) that the PLL output power is 10 dBm at 4 GHz, for a frequency deviation of 0.40 MHz, demonstrating that the PLL is locked on to the radar echo signal frequency. It is clear from Figure 6(b) that he frequency deviation required to break-lock is 0.51 MHz for the radar echo power of -10 dBm.

The simulation results of frequency deviation as a function of LFM signal power and modulation rates at break-lock are shown in Figure 7(a) and 7(b).

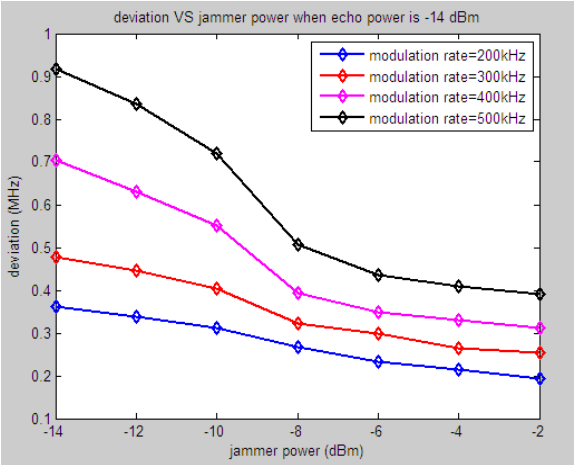

Figure 7 (a). Frequency Deviation Vs LFM Signal Power at Break-lock with Echo Power of -14 dBm

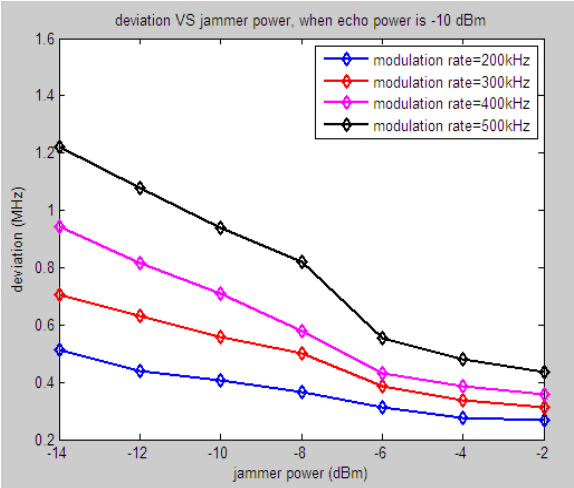

Figure 7(b). Frequency Deviation Eviation Vs LFM Signal at Break-lock with Echo Power of -10 dBm

From the Figure 7(a), it is clear that for a typical modulation rate of 200 kHz, the frequency deviation required to break-lock is 0.36 MHz for a jammer power of -14 dBm and it is 0.19 MHz for a jammer power of -2 dBm. This result demonstrates that the break-lock is achieved at higher values of frequency deviation, when the jammer power is less.

From Figure 7(a), it is seen that the frequency deviations at break-lock are 0.36 and 0.91 MHz for the modulation rates of 200 and 500 kHz, respectively. From this result, it can be demonstrated that the lower is the modulation rate, lesser is the frequency deviation required to break-lock. From the above results, it can be demonstrated that the LFM signal power and frequency deviation are the key parameters to break-lock in the PLL. So, for effective jamming of the PLL in the monopulse receiver, the LFM jamming signal with suitable power and frequency deviation is to be injected into the receiver along with the radar echo signal.

5. Conclusion

The simulation results of break-lock of the PLL in monopulse receiver in the presence of LFM interference signal have been presented. The break-lock is measured through the

frequency spectrum of the PLL. It is demonstrated that the frequency deviation required to break-lock is 0.36 MHz for a typical modulation rate of 200 kHz and LFM, and radar echo signal powers of -14 dBm each. Furthermore, it is estimated that the frequency deviation required to break-lock is 0.36 and 0.91 MHz for the modulation rates of 200 and 500 kHz respectively, for a typical LFM signal power of -14 dBm. It is also verified that break-lock is achieved at lower values of frequency deviation when the modulation rate is less. So, the developed PLL model and the simulation results will provide greater flexibility in designing the monopulse radar receiver and effective jamming of missile seekers.

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