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A Novel Research of ZVZCS Synchronous Rectification Converter Based on Phase-shifted Full-bridge Control

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Abstract

Due to synchronous rectification based on Phase-shift full bridge converter is difficult to work in a state of soft switch, to solve this problem, this paper sets out an control approach of synchronous rectification based on the ZVZCS phase-shifted full-bridge, and the drive signal of synchronous rectification side uses leading-leg drive waveform after a certain time delay and applies the resonant principle in the switching process, not only keeping full bridge ZVZCS soft switching but also realizing MOSFET of the synchronous rectification ZVS. The simulation of saber and experimental research show that the converter has a good performance.

Keywords: *ZVZCS converter, synchronous rectification, the simulation of saber*

1. Introduction

With the rapid development of the contemporary technology, phase-shift full-bridge converter was highly concerned by people due to advantages like simple circuit structure, high power density power supplies and high efficiency and easy to realize soft-switching for switching devices. In low voltage and high current output situation, phase-shifted full-converter will cause a great power loss and decrease the overall efficiency if the power supply to the voltage drop on the secondary rectifier diode. The synchronous rectification technology was introduced, using the power MOSFET with very low on-state resistance to replace the diode rectifier [1-2], in order to improve the overall efficiency of power supply under the circumstance of low voltage and high current.

ZVS was achieved in paper [3], but the synchronous rectifier was working at hard switch state. All switches ZVS was realized in synchronous rectifier converter in paper [4], but the lagging leg switches was hard to realize soft-switching when at light load situation due to the use of conventional phase-shifted full-bridge converter. In paper [5], a phase-shift full bridge ZVZCS was proposed which the leading leg switches and lagging leg switches can realize soft switch under wide scope situation, and the circuit structure is not only simple, but also low dissipation loop. Based on this, asynchronous rectifier converter control method based on phase-shift full bridge ZVZCS was proposed in this paper, it got the opposite wave of the drive wave for the leading leg switches, coupled with appropriate delay, it not only can realize ZVZCS for full bridge side of converter, but also can realize ZVS for secondary synchronous rectifier. The proposed control method add the simple circuit in traditional synchronous rectifier topology, namely realize wide range of soft switch enabled for all switches, it can further reduce the overall loss, increase the efficiency of power supply. To verify the effectiveness of the proposed converter, theoretical analysis and experimental results will be presented with 4.8kW on-board charger specification.

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2. Operation Principle for Converter

Schematic diagram of the proposed converter is shown in figure 1. Q_1-Q_4 are ZVZCS switches for phase-shift full bridge, C_1 and C_3 are parallel capacitance for Q_1 and Q_3, C_1=C_3=C_r, D_1 and D_3 are anti-parallel diode for Q_1 and Q_3, D_2 and D_4 are serious diodes for lagging arm Q_2 and Q_4, C_b is blocking capacitor, L_{lk} is leak inductance of the transformer, Q_5 and Q_6 are synchronous rectifier switches. L_5 and L_6 are multiple frequency inductances, R is load, C is load capacitor, K is turns ratio for transformer, the control sequence diagram of converter is shown in Figure 2.

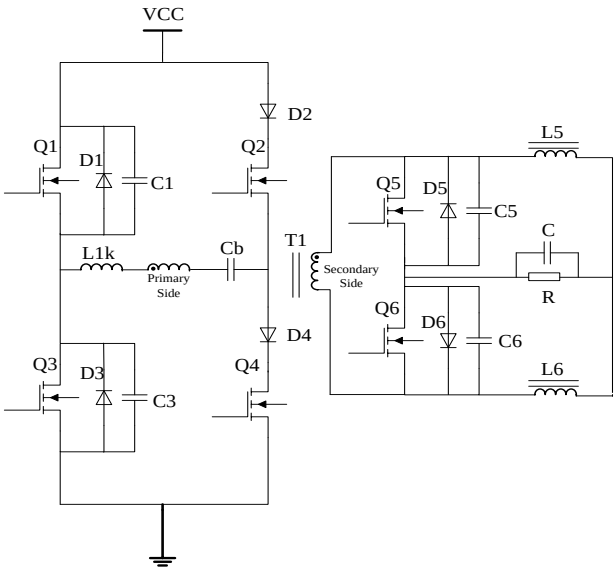


Figure 1. Schematic Diagram of the Proposed Converter

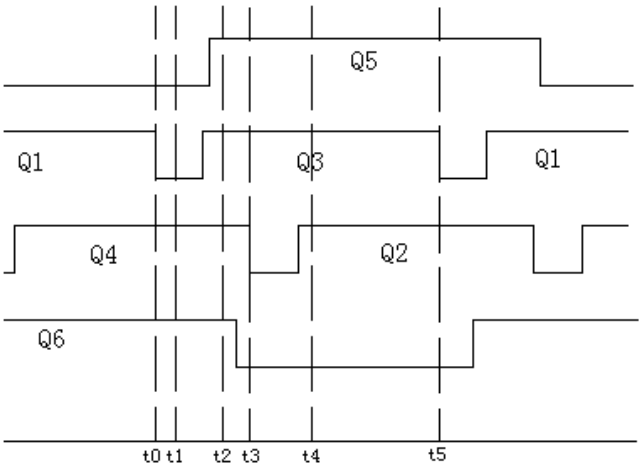


Figure 2. Key Waveforms of the Proposed Converter

(1)Mode 1(t_0)

At t_0, Q_1 and Q_4 are on, the current from original side flow from Q_1, blocking capacitor C_b,the transformer primary side, leakage inductance L_{lk} and Q_4 towards the vice side to pass the power and charge to block C_b and the parasitic capacitance of C_3 in the leading

leg switches. the vice side current flow from L_5, load R and Q_6 back to the secondary side of the transformer , and to C_5 charge . Another current loop L_6, R, Q_6. $U_{AB}=U_{in}$, $U_A=U_{in}$, $U_B=0$, the voltage value of the blocking capacitor C_b $U_{Cb}(t_0)$.

(2) Mode 2 [t_0, t_1]

At t_0, turn off Q_1, capacitor C_1 begins to charge from 0 to a voltage , a voltage from the capacitor C_3 starts discharging U_{in} , Q_1 is the zero voltage turn-off. Secondary inductance reflected to the primary series with the leakage inductance , the inductance is very great at this time , the primary current i_p can be approximated seen as unchanged, $I_{p0} = I_0/K$,as a constant current source, and continue to charge the blocking capacitor C_b . At time t_1 , the capacitor C_3 is completely discharged and has been reduced to 0 ,the diode D_3 will naturally be connected.

$$u_{Cb}(t) = U_{Cb}(t_0) + \frac{I_{P0}}{C_b}(t - t_0)$$

$$u_{C1}(t) = \frac{I_{P0}}{2C_r}(t - t_0)$$

$$u_{C3}(t) = U_{in} - \frac{I_{P0}}{2C_r}(t - t_0)$$

(3) Mode 3 [t_1, t_2]

At t_2, D_3 opened, at the same time, open Q_3, and Q_3 is zero voltage turning. The primary side circuit of D_3, C_b, transformers, Q_4. At the same time there are two secondary current loop , one current loop L_6, R, Q_6, current freewheel ,another current loop for the C_5, L_5, R, so this loop until the diode D_5 ,C_5 discharge guide . At this point turn on Q_5, the Q_5 is zero voltage turning on. At this point Q_5, Q_6 are turned on simultaneously, the transformer secondary is shorted, so blocking capacitor C_b voltage is applied to the leakage inductance of all, the primary current starts to decrease linearly. At t_2, primary current drop to zero. $U_{AB} = 0$, $U_A = 0$, $U_B = 0$.

The primary current drops to zero at t_2. The continuing period is:

$$t_{12} = \frac{L_{lk} I_{P0}}{U_{Cb}}$$

(4) Mode 4 [t_2, t_3]

In this mode, the primary current $i_p = 0$, there are two sides of the transformer freewheeling circuits, one for the L_5, Q_5, R, another one for the L_6, C_6, R -wheeling until D_6 turns on, off Q_6, Q_6 zero voltage is turned off . $U_{AB}=U_{Cb}$, $U_A=0$, $U_B=-U_{cb}$.

(5) Mode 5 [t_3, t_4]

At t_3, due to the primary current is zero , so the Q_4 is off, the Q_4 is with zero current shutdown mode, after small period of delay, opening Q_2, due to the presence of leakage current cannot be mutated , so Q_2 is zero current turn . $U_{AB}=-U_{in}$, $U_A=0$, $U_B=U_{in}$.

(6) Mode 6 [t_4, t_5]

At t_4, the primary energy began to secondary output while blocking capacitor C_b to reverse charge. At t_5 off Q_3, from the beginning of the next half cycle [t_5, t_{10}], equivalent to the above-mentioned period [t_0, t_5]. Blocking capacitor voltage reaches its maximum at the time t_6, therefore:

$$U_{Cb}(t_6) = U_{Cb}(t_5) - 2\frac{C_r U_{in}}{C_B} = U_{Cb} - \frac{I_{P0}}{C_b} t_{45} - 2\frac{C_r U_{in}}{C_b} = -U_{Cb}$$

Due to C_r and C_b, so

$$U_{Cb} = \frac{I_{P0}}{2C_b} t_{45}$$

3. Conditions of Achieving Soft Switching and Synchronous Rectifier Drive Design

(1) Achieving ZVS conditions for the leading leg switches

To ZVS conditions for the leading leg switches, the transformer leakage inductance and the capacitor resonance process must have sufficient energy to charge the capacitor in all consumed (including the transformer primary winding parasitic CTR), thus it must meet the following formula:

$$E > \frac{1}{2} C_r U_{in}^2 + \frac{1}{2} C_b U_{in}^2 + \frac{1}{2} C_{TR} U_{in}^2$$

During the period of achieving ZVS, as the current of primary side of the transmer remains the same and approximately equal to a current source. Therefore, the ZVS can be realized as long as the dead time satisfy the following formula.

$$T_d > \frac{2C_r U_{in}}{I_1}$$

(2) Conditions for the lagging leg switches to realize ZCS

From the analysis of principles for converter, the conditions for the lagging leg switches to realize ZCS is the primary current should be reduced to 0 before the lagging leg switches is on, so t_{12} is:

$$t_{12} = \frac{2L_{lk} C_b}{t_{45}} = \frac{4L_{lk} C_B}{DT}$$

D is the duty factor and T is the period in the above formula

(3) conditions for synchronous rectification to achieve soft switching and driving

In the case of synchronous rectifier with heavy loads, if the conventional hard-switch, then the switch loss will be great which will cause a great heat on switch tube, it will cause not only secondary rectification efficiency is low , but also make the life of the switch reduced. So the best solution is to make the synchronous rectifier switch work in conditions of the soft-switching state, it will not only reduce the loss, but also to increase the service life of the switch.

In this paper, the parallel resonant secondary inductance and capacitance of the switch, the shunt capacitance voltage release to zero, so that the natural anti-parallel diode conduction, to achieve synchronous rectifier switch tube ZVS. In an example Q_5, Q_5 is driven by the drive waveform to Q_1 reverse delay, delay time of the dead time plus ultra forearm LC resonant time. Therefore, the delay time T_5 is:

$$T_5 = T_{D12} + \frac{\pi}{2} \cdot \frac{1}{\sqrt{\frac{1}{L_5 C_5} - \frac{R^2}{4L_5^2}}} \geq \frac{2C_1 U_{in}}{I_P} + \frac{\pi}{2} \cdot \frac{1}{\sqrt{\frac{1}{L_5 C_5} - \frac{R^2}{4L_5^2}}}$$

Synchronous rectification side MOSFET driving waveform is ultra forearm drive waveform to be inverted and delayed, super signal after opto isolated forearm after a RC delay circuit, the delay time parameters are:

$$\tau = -\mathrm{R} \cdot \mathrm{C} \cdot \ln\left(\frac{E - V}{E}\right)$$

After comparison with standard 5V voltage comparator output goes back into after the synchronous rectifier MOSFET driver chips. As shown in Figure 3.

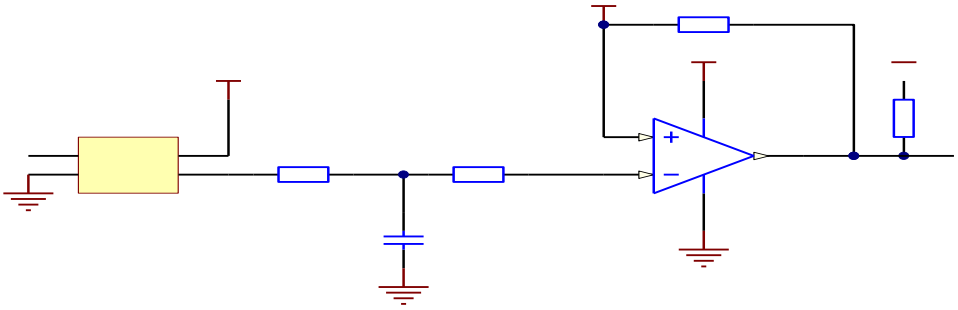


Figure 3. Synchronous Rectifer Circuit

4. Simulation and Analysis

In order to verify the correctness and feasibility of the control method, simulation analysis was carried out saber the simulation model is shows in Figure 4. Input voltage is 530V, output power is 4.8KW (48V/100A).

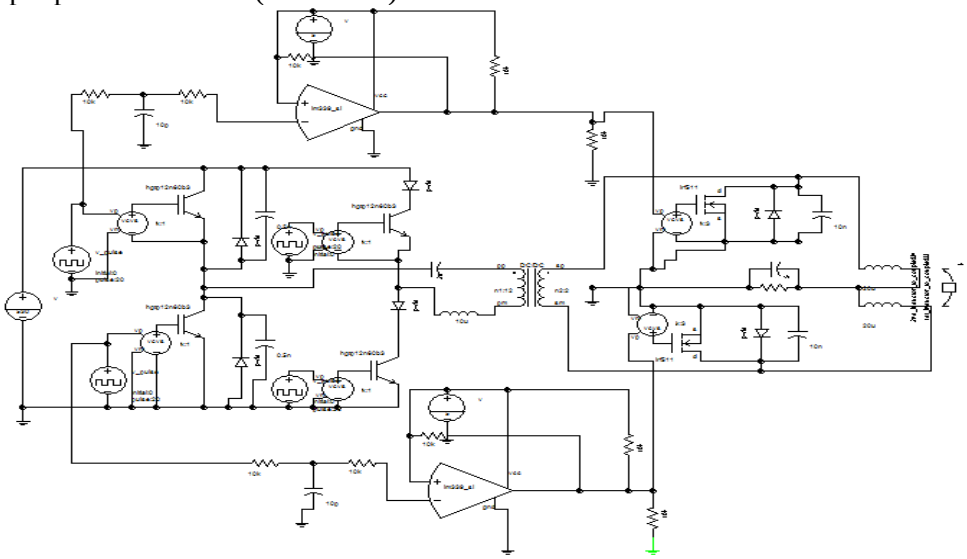
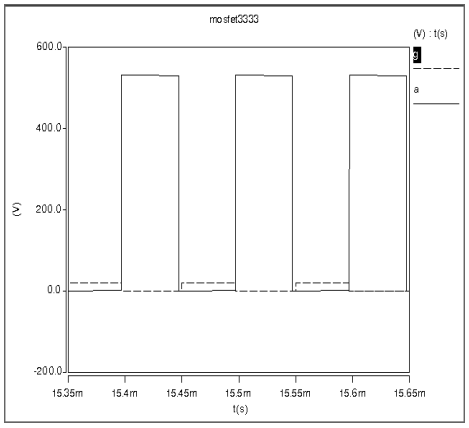
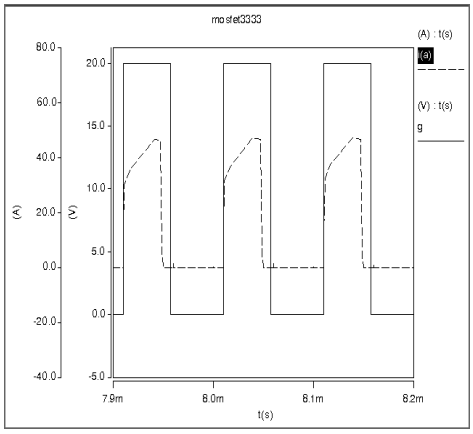


Figure 4. Saber Simulation Circuit

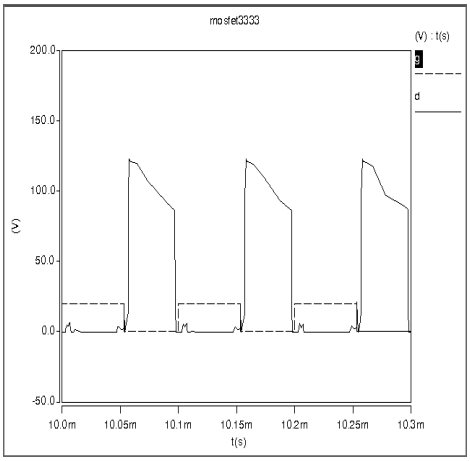
From Figure 5, by means of the solid line that is Vce of Q_5 waveform and dashed that is Vge of Q_5 waveform, ZVS condition for leading leg switches is shown in Figure (a). ZCS condition for lagging leg switches is shown in Figure (b), drive waveform of Q_4 is the solid line, LC by Q_4 of current waveform is the dashed line. In addition, ZVS condition for synchronous rectifier is shown in Figure (c), and the solid line is Vds of Q_5, dashed line is Vgs of Q_5 . Load output is shown in Figure (d).



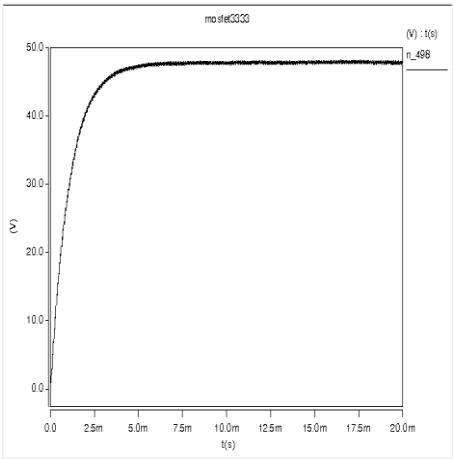
(a) ZVS Condition for Lagging Leg Switches



(b) ZCS Condition for Lagging Leg Switches



(c) ZVS Condition for Synchronous Rectifier



(d) Load Output Voltage

Figure 5. Experiment Simulation Waveforms

5. Experiment Result

To verify the effectiveness of the proposed converter, prototype of the proposed converter is designed with following specifications. Input voltage is 380V and output voltage is 48V.Output power: 4.8KW(48V/100A). Switches are FGA25N120. The ratio of transformer n = 5.5, $L_5 = L_6 =$ 20uH, blocking capacitor C_b = 2uF. As shown in Figure 6, experimental waveforms of the proposed converter, ZVS condition for leading leg switches are achieves, including the waveform 1 for Vce and the waveform 2 for Vge , the same as (a) corresponding to simulation and experimental results seen in Figure 5. ZCS condition for lagging leg switches is shown in Figure 7, in where the waveform 1 is Ic and the waveform 2 is Vge, Corresponding to Figure 5 (b) simulation and experimental results can be seen. ZVS condition for synchronous rectifier is shown in Figure 8, in where the waveform 1 is Vge, the waveform 3 is Vce, the same as (c) corresponding to simulation and experimental results seen in Figure 5.

At the same time to test the whole efficiency of the proposed converter in this paper, with traditional PSFB converter through the contrast analysis of figure 9 is given the same input and output parameters of both the overall efficiency contrast curve. Can be seen from the figure 9, the overall efficiency of the proposed converter than traditional PSFB converter have certain to improve under different load in this paper.

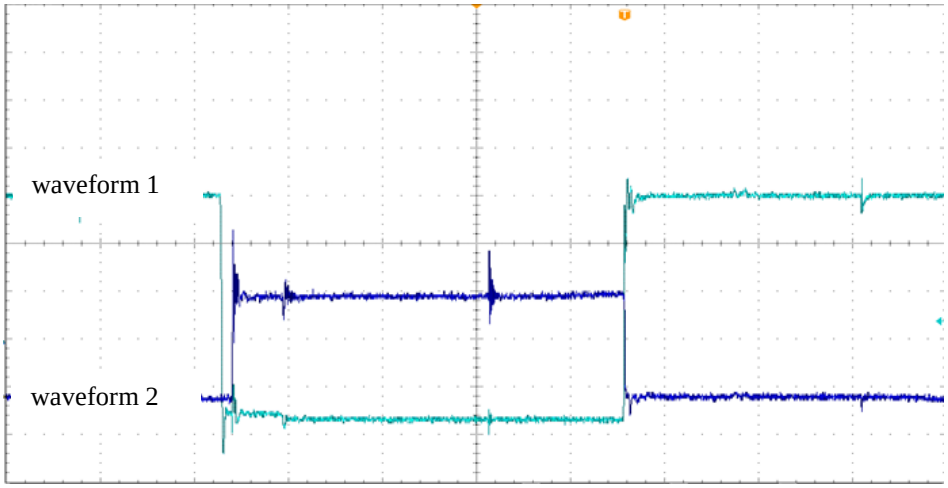


Figure 6. ZVS of Leading Leg Switches

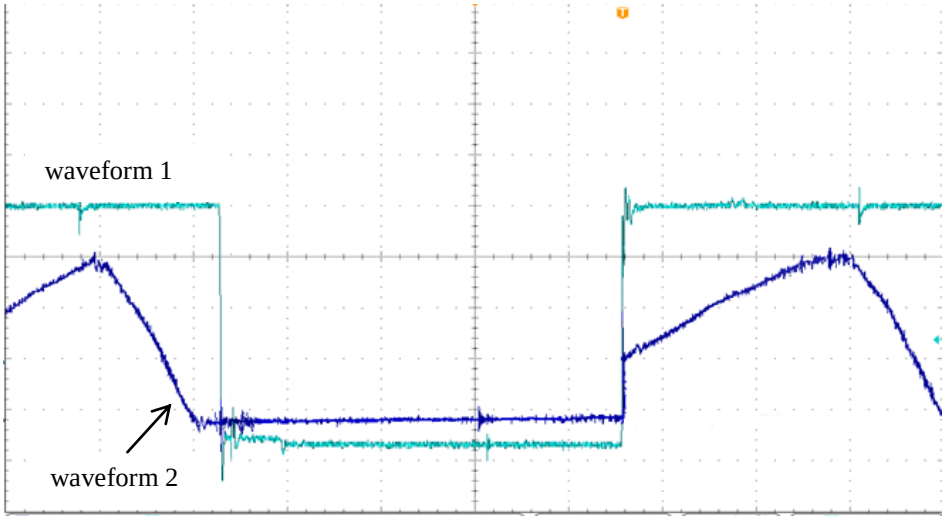


Figure 7. ZCS of Lagging Leg Switches

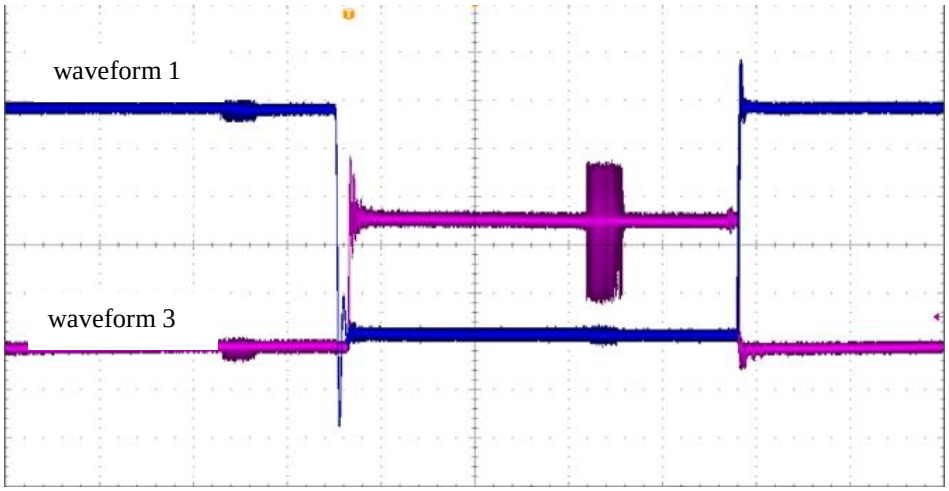


Figure 8. ZVS Condition for Synchronous Rectifier

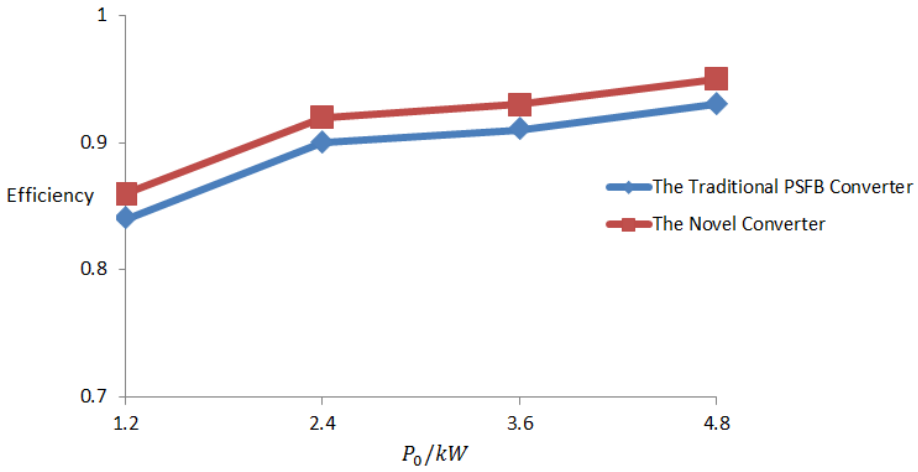


Figure 9. Curves of Efficiency

5. Conclusion

In this paper, a novel control method based on ZVZCS converter synchronous rectifier is presented, using the topology of the lag bridge arm concatenated diode: The seconary side rectifier drive signal get the opposite of the two PWM waveform from advanced arms and add proper delay, not only achieve the full bridge ZVZCS, but also carry out the sychronous rectifer ZVS. Simulation and experimental results show that this control method can enable all switches of the converter to work within large scope of soft switch which will improve the efficiency of the converter.

Acknowledgements

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