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Analysis and design of Phase Frequency Detector using Current Mode Logic

Anu Tonk[1] and Bal Krishan[2]

Department of Electronics Engineering, YMCA UST, Faridabad, Haryana
[1]tonkanu.saroha@gmail.com
[2]kadiyan26@yahoo.com

Abstract

The design of phase frequency detector (PFD) using CMOS current mode logic (CML_PFD) is presented in this paper. Further its performance has been compared with a proposed PFD, denoted here as M_CML_PFD. The simulation results are focused on accounting the power dissipation, delay and output noise. Both the PFDs are designed to be dead zone free and using 0.35μm CMOS technology on SPICE simulator. The output noise experienced is reduced by 6.5% in M_CML_PFD. The power dissipation of the proposed M_CML_PFD is 15.72% lesser and delay is 2.37 times less than the CML_PFD when operating at 100 MHz input frequency with 3.3V voltage supply.

Keywords: *Phase Locked Loop, High Speed Integrated Circuits, Phase frequency detector, Current Mode Logic, D flip flop*

1. Introduction

Phase locked loops (PLL) are widely used for clock phase synchronization, frequency synthesis, wireless systems, digital circuits, high performance microprocessor systems and disk driven electronics [1]. There is an increasing demand for a high frequency operation and low jitter PLL. A common architecture for clock generation uses a phase frequency detector (PFD) for simultaneous phase and frequency acquisition. Traditional phase frequency detector finds out the difference in phase and frequency between two inputs [3]. These frequency inputs are reference frequency and the output of voltage controlled oscillator [2]. A difference in phase results in a pulse generated at either the UP or DOWN output of the PFD. Ideally, the pulse width is linearly proportional to the phase difference. Current-mode-logic circuits play an important role in the design of CMOS frequency synthesizers for modern wireless digital communication systems [6]. Current mode logic (CML) is a popular logic style for high speed circuits. This type of logic was first implemented using bipolar transistors [4] and extended for applications with MOS transistors. Conventional CMOS, however, has almost negligible static power dissipation but still the dynamic power dissipation during transition from one logic level to another has led to the development of a logic that reduced the dynamic power dissipation. Thus the Current Mode Logic (CML) was introduced as it requires a smaller dynamic power than that of the conventional logic because of smaller output swings [5].

2. Circuit Architecture

2.1 CML_PFD

The CML_PFD in Figure1 has been designed using two D flip flops. Further the D flip flop involves use of two D latches in master slave configuration as shown in Figure 2.The main block of CML_PFD is nothing else but a "D latch", shown in Figure 3, on which the working of CML_PFD mainly depends.

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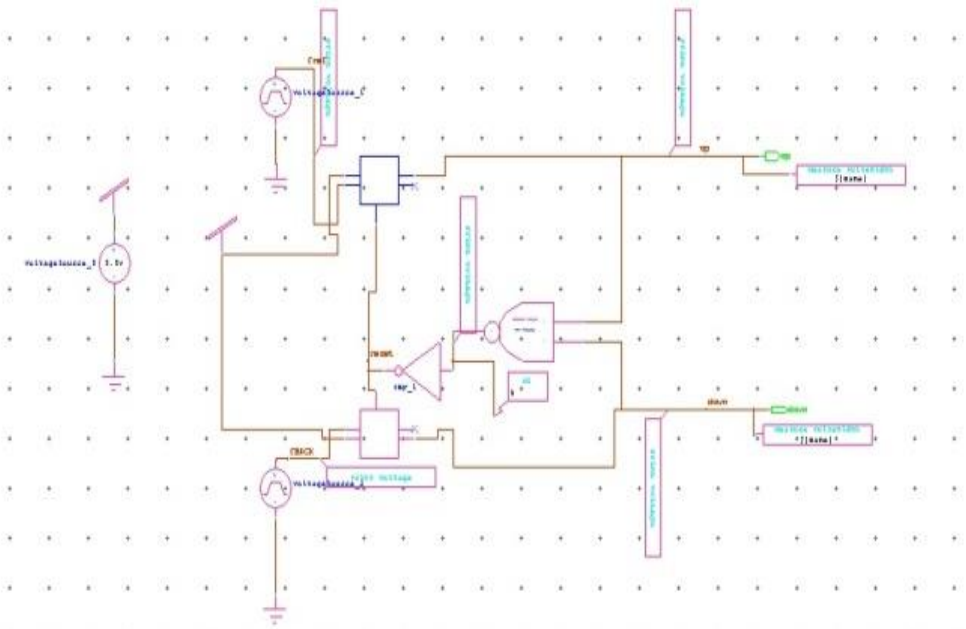

Figure 1. CML Design using Two D Flip Flops

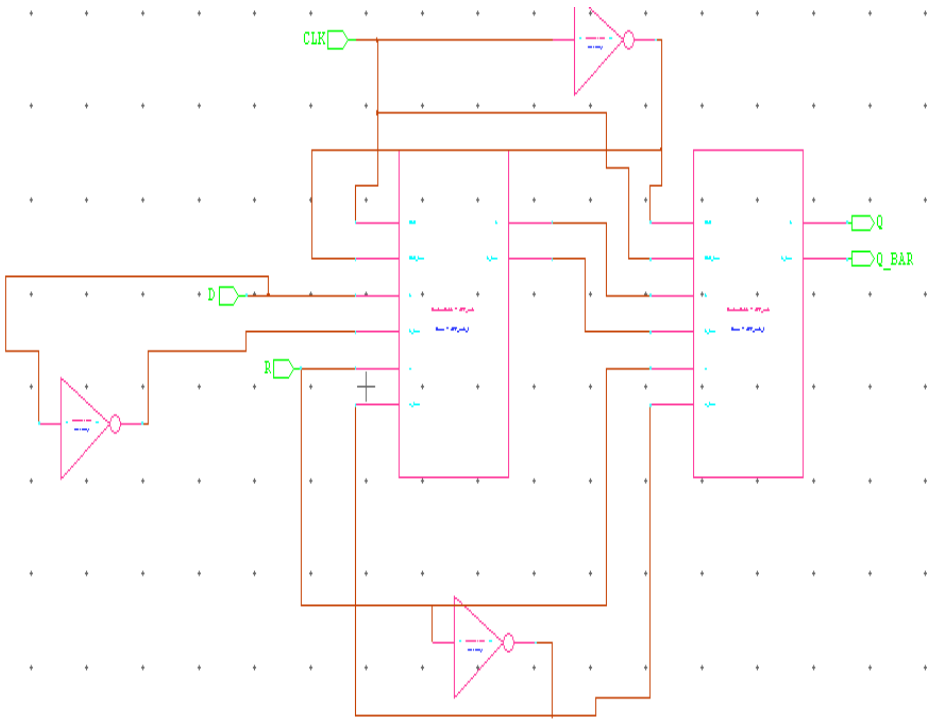

Figure 2. Two D Latches in Master Slave Configuration to form D Flip Flop

In CML_PFD the D-latch has been designed using Current Mode logic. The D latch here is negative edge triggered. PMOS_1 and PMOS_2, PMOS_1 and PMOS_3, NMOS_6 and NMOS_3 working as current mirror source. PMOS_4 and PMOS_6 is diode connected load which remain in saturation region. D and D_BAR are given at NMOS_2 and NMOS_5 respectively while CLK and CLK_BAR at NMOS_1 and NMOS_7. NMOS_6 and NMOS_9 are used to provide ground path to outputs when CLK_BAR signal is high. This force the circuit to be in reset state. The working of D

latch depends on the clock condition which has been explained as follows with the two possible conditions:

Case 1: When Clk=1 and ClkX=0

a) *When D=1 and DX=0 then* PMOS_3 is ON and thus Q=1

b) *When D=0 and DX=1 then* PMOS_3 is ON and a path is provided to ground through NMOS_5 and NMOS_1 and thus Q=0

Case 2: When Clk=0 and ClkX=1

Then Q will remain in same state as previous because NMOS_8 and NMOS_9 are acting as hold circuit.

Thus the D latch in CML_PFD is the main building block and responsible for overall characteristics of CML_PFD.

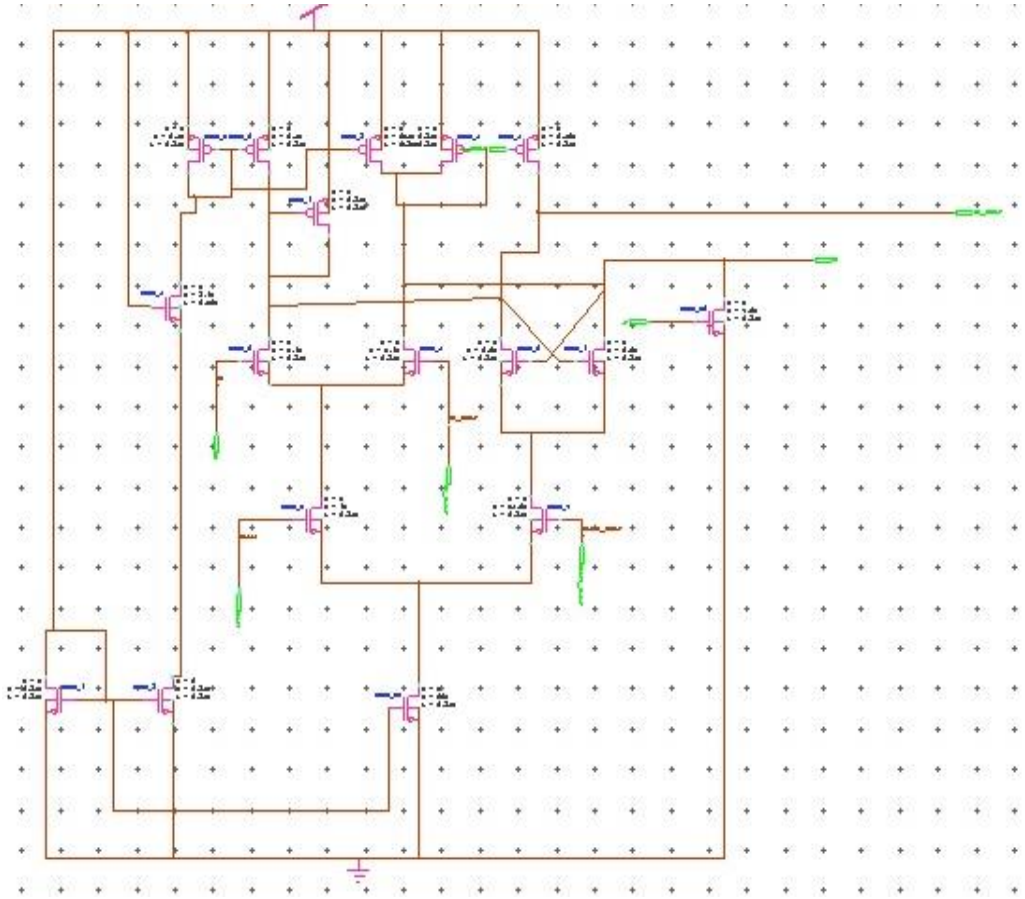

Figure 3. Schematic of D Latch used in CML_PFD

2.2 M_CML_PFD

For the standard CML_PFD and proposed M_CML_PFD the difference lies in the design of D latch as shown in Figure 4.

On Comparing Figure 3 and Figure 4 we notice that PMOS_2 and PMOS_3 are removed which results in the reduction of the number of current mirrors, hence the dependence on the current reduces considerably. With this the glitches in the output are reduced and the same can be observed from the graphs of CML_PFD and M_CML_PFD in locked state. Here PMOS_6 acts as load and is in saturation always. Also the transistor count in M_CML_PFD is reduced further decreasing the power dissipation. A reduction in delay and faster response is observed too in the proposed circuit.

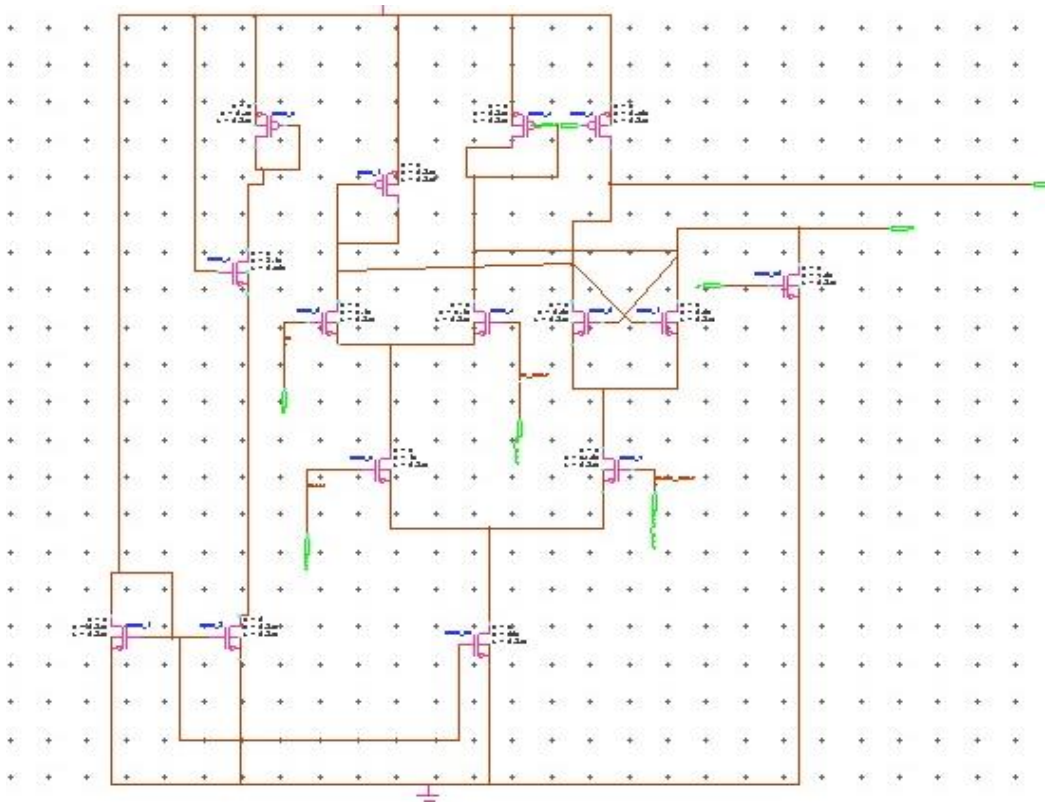

Figure 4. Schematic of Proposed D Latch in M_CML_PFD

3. Simulation Results

The simulations mentioned above were done using Tanner tools 14 version. With the help of S-EDIT, W-EDIT, L-EDIT net list was generated and SPICE commands were used to obtain various parameters mentioned in the Table 1.

3.1 Output Waveforms

Table 1. Setup Parameters

Rise time/RT	0.01 ns
Fall time/FT	0.01ns
High Time/HT	5ns
Low time/LT	5ns
Pulse Width/PW	5ns
Bit pattern	1010011
AC analysis(Frequency Sweep Type)	dec
Start frequency ; Stop frequency	10 meg; 100 meg
Number of frequencies	10

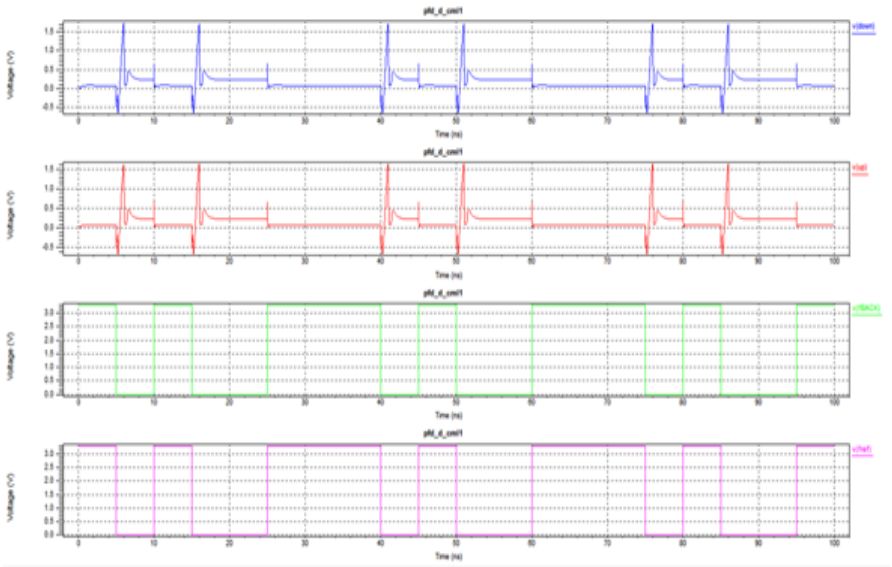

Figure 5(a). Locked State of CML_PFD with Same Reference and Feedback Frequencies [v (Down), v (Up), v (Back) and v (Ref) from Top to Down]

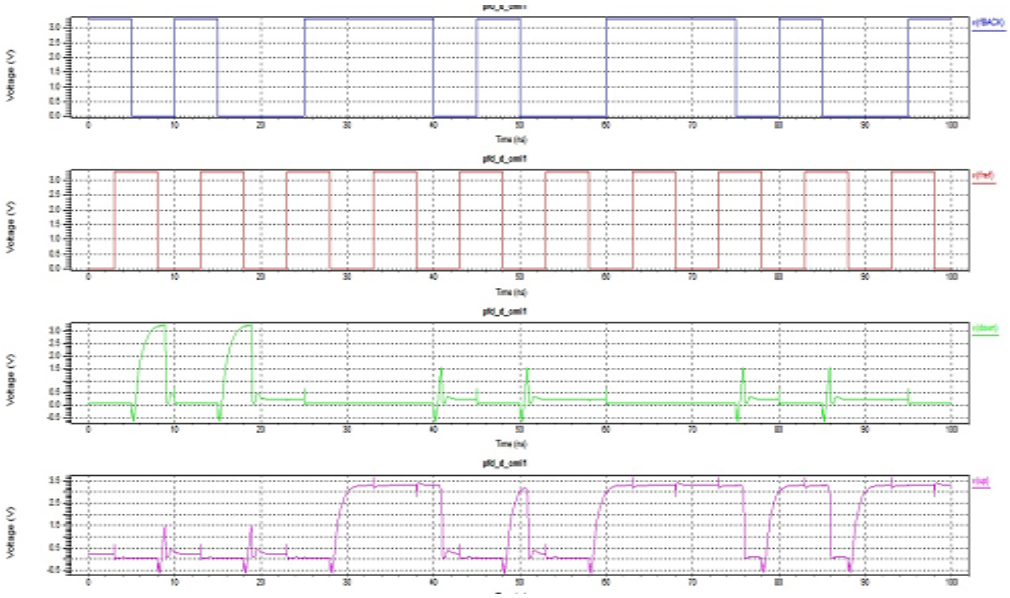

Figure 5(b). Output of CML_PFD when Both Feedback and Reference Frequencies are Different (Lead/Lag at Different Instants) [v (Back), v (Ref), v (Down) and v (Up) from Top to Down]

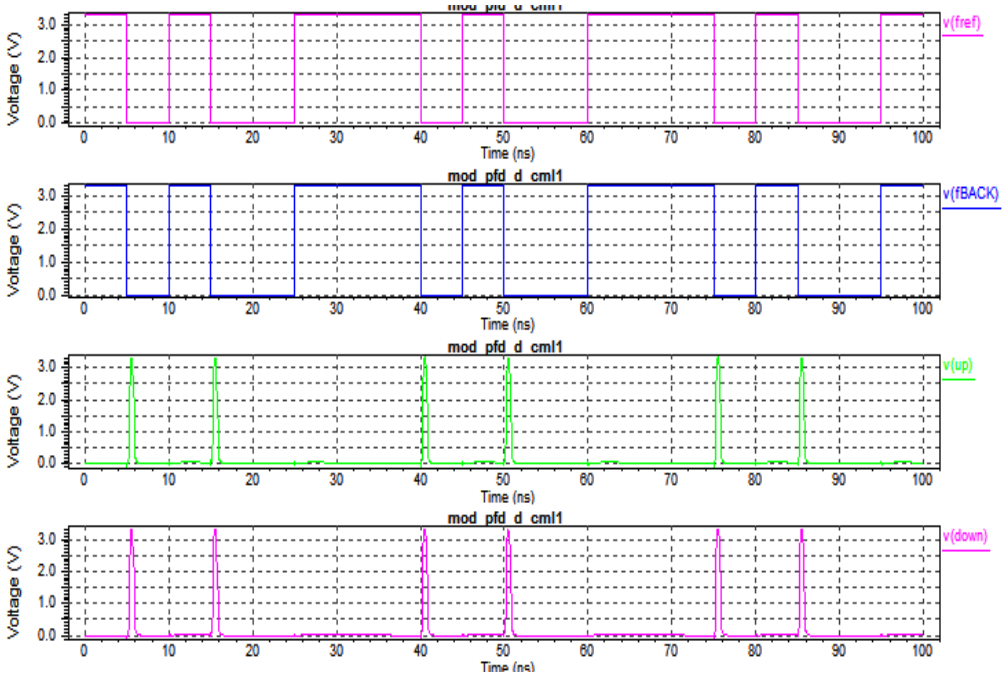

Figure 6(a). Locked State of M_CML_PFD with Same Reference and Feedback Frequencies [v (Down), v (Up), v (BACK) and v (Ref) from Down to Top]

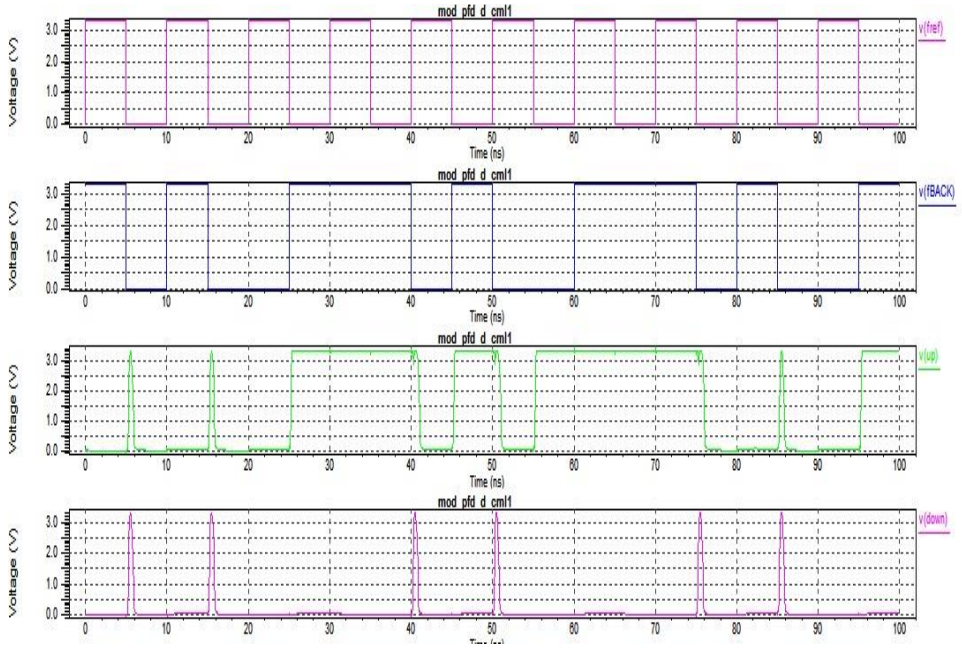

Figure 6(b). Output of M_CML_PFD when Both Feedback and Reference Frequencies are Different (Lead/Lag at Different Instants) [v (Down), v (Up), v (BACK) and v (Ref) from Down to Top]

Figure 5(a) displays the pfd characteristics of CML_PFD when output of VCO (fback) and reference frequency (fref) are of same frequencies. In it we can observe that whenever both the falling edges of fback and fref occur simultaneously, there will be a glitch on up and down signal displaying that the two frequencies are locked in phase as well as frequency Next, if fback is leading fref then the up signal goes high and remains in the

high state till the next falling edge appears but if fref is leading fref then the down signal will become high as observed in figure 5(b). Same is true for M_CML_PFD.

3.2 Transfer Curves

Table 2. Setup Parameters

Parameter1(for sweep)	K
Start value	0ns
Stop value	10ns
Sweep type	Linear
Step	0.5
Voltagesource_2 master interface	Pulse
Delay (Voltagesource_2)	K
Rise Time, Fall Time	0.01ns
VHigh	3.3V
VLow	0V

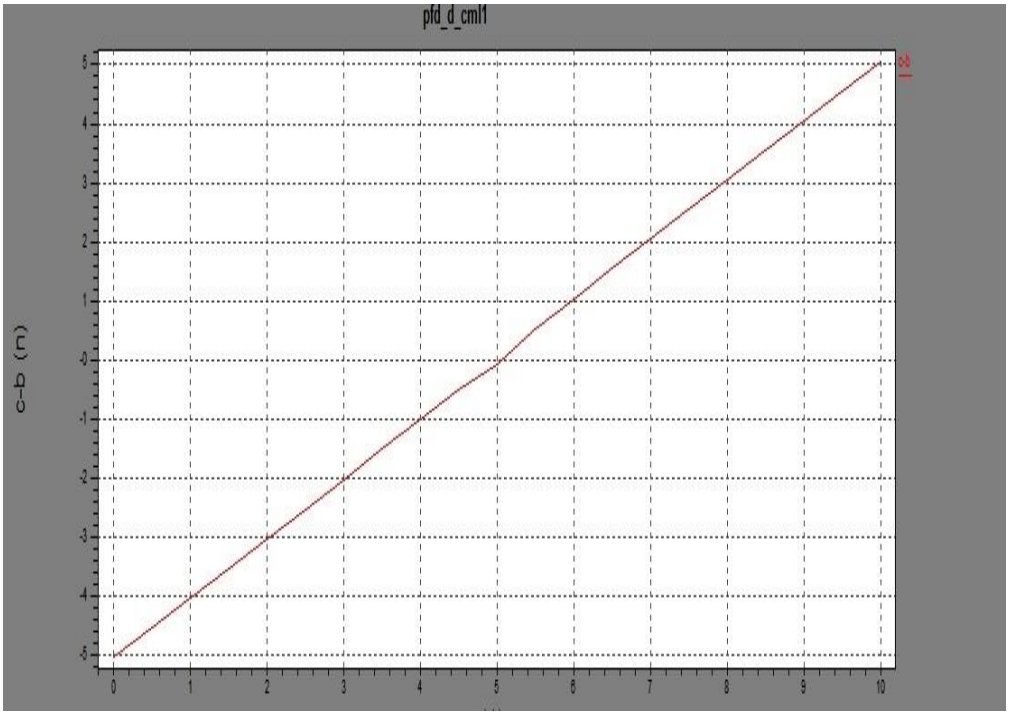

Figure 7. Transfer Curve for CML_PFD

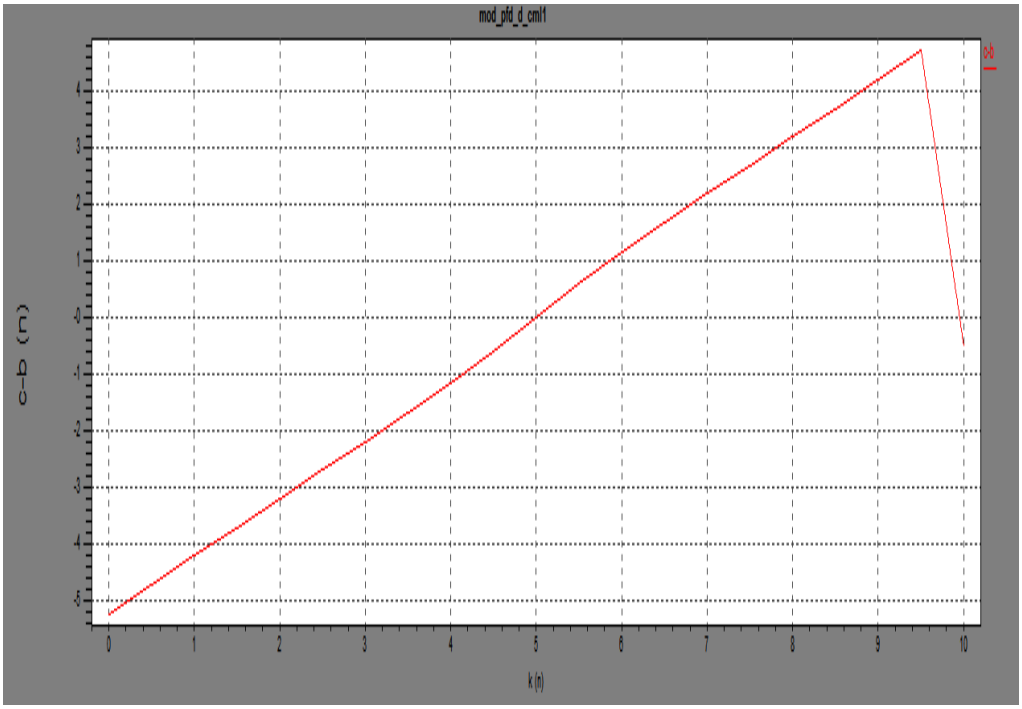

Figure 8. Transfer Curve of Proposed M_CML_PFD Circuit

For Plotting the transfer curves use the option of Arithmetic traces in W-Edit. The transfer curve has c-b(ns) value on Y axis and k(ns)value on X-axis. This shows the variation of difference of V(up) and V(down) with respect to the delay (k) sweep set for the Voltagesource_2. This in turn is represents no dead zone if the graph obtained is linear "Dead zone" is a problem that occurs in non-ideal PFD's generally resulting in the flatness of the phase response graph near the origin thus contributing to the occurrence of phase noise and jitter. The PFD doesn't detect the phase error when it is within the dead zone region, then PLL locks to a wrong phase which is highly undesirable and the probability of obtaining inaccurate results increases substantially. But the improvised design presented in this paper leads to a dead zone free PFD as depicted by the transfer curve shown in Figure 7 and Figure 8.

3.3 Delay

The benefit of a faster logic propagation delays in speed critical paths of mixed signal applications such as the phase detector of a high-speed PLL is invaluable [5].

The propagation delay or in a mixed signal circuit can lead to errors and noise. Thus for the reduction in noise it is very important to obtain a high speed circuit or indirectly reduce the total circuit delay.

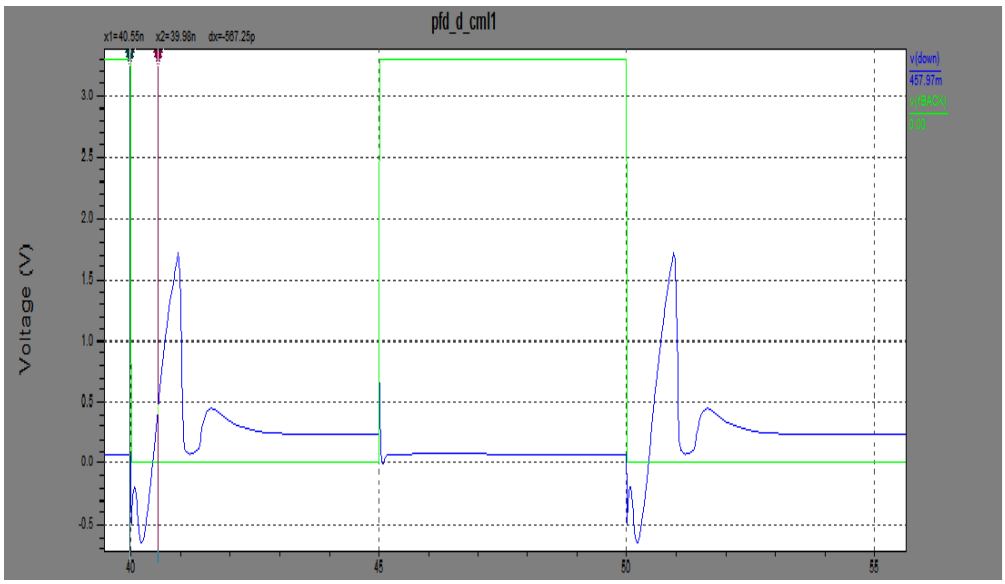

Figure 9. Graph for Delay Calculations of CML_PFD

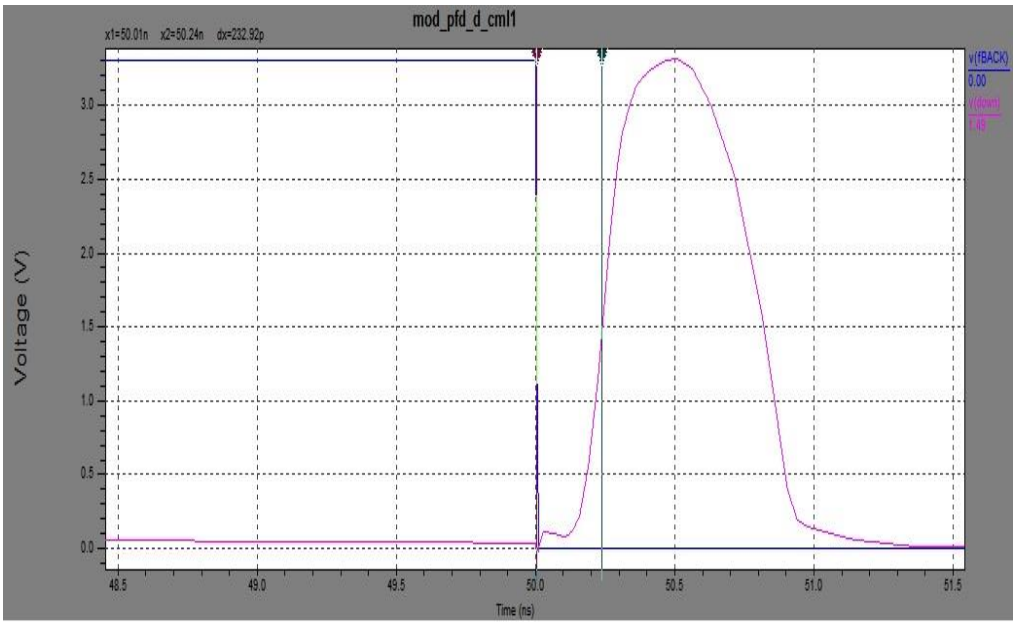

Figure 10. Graph for Delay Calculations of M_CML_PFD

As can be observed here by comparing Figure 9 and Figure 10, we see that the total delay for the proposed model M_CML_PFD is approximately 0.24 ns. The total delay of the CML_PFD is 0.5ns. Thus the overall speed of M_CML_PFD considerably improves in comparison to CML_PFD. This results in an added advantage especially in case of phase frequency detector as it is used for mixed signal applications where a slight difference in speed can totally change the output. This may even result in jitter which is not appreciated.

3.4 Noise Spectral Density vs. Frequency

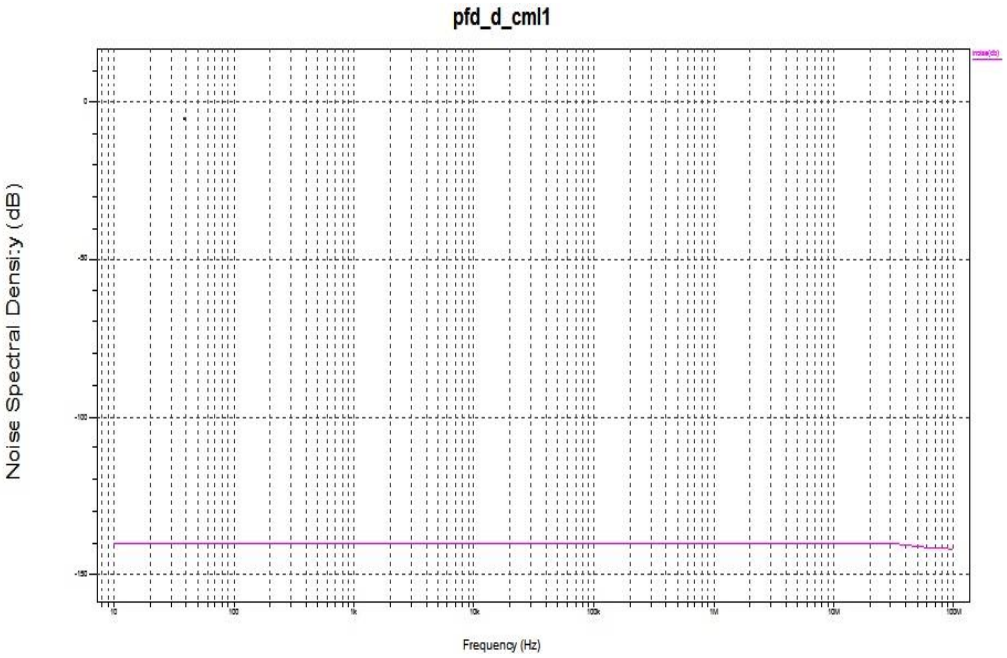

Figure 11. Noise Spectral Density Graph for CML_PFD (x Axis Represents a Frequency Range from 10 to 100 MHz and y Axis Represents Noise in db)

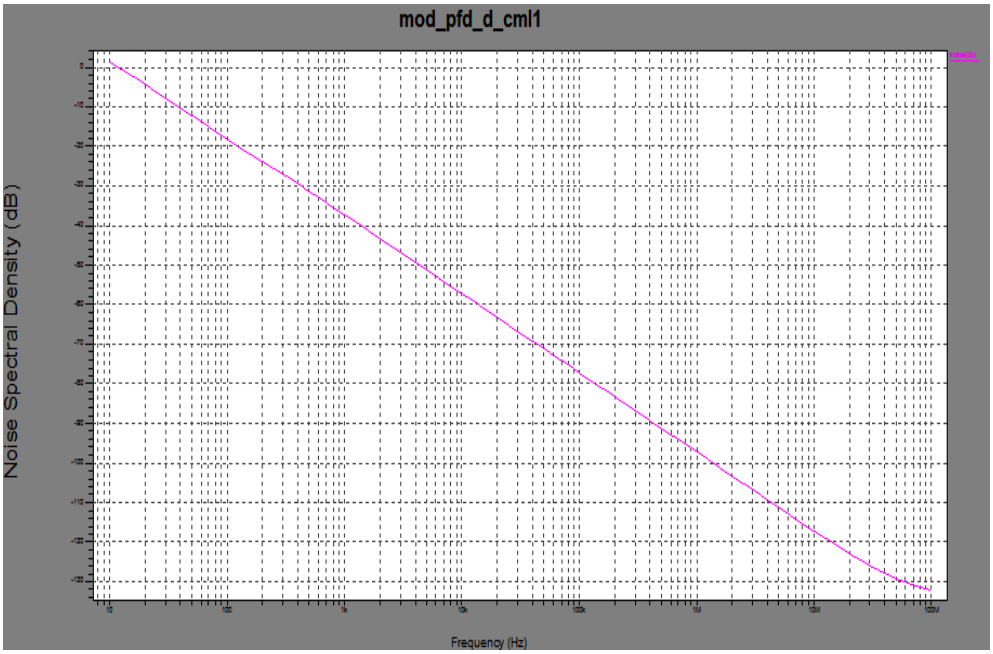

Figure 12. Noise Spectral Density Graph for M_CML_PFD (x Axis Represents a Frequency Range from 10 to 100 MHz and y Axis Represents Noise in db)

4. Conclusions

This paper presents PFD architecture using current mode logic technology which is a novel one. While on one hand it is dead zone free on the other it consumes low power and operates at a better speed. Zero dead-zone implies that the PFD can detect any amount of phase error thus probability of occurrence of an error has been considerably reduced.

- The M_ CML_PFD which is proposed here is found to be better in performance than the CML_PFD, as the transistor count is reduced.
- As it can be inferred from the Table 3, the power dissipation of the proposed CML_PFD is 15.72% less than the previous CML_PFD.
- Similarly delay is is reduced by 2.37 times as compared to the previous CML_PFD.
- Also noise experienced is reduced by 6.5% which is a noticeable Figure as noise is a very important parameter.

Table 3. Comparison Table based on Various Parameters between Previous and Proposed CML_PFD

	CML_PFD	M_CML_PFD
Power	7.25mw	6.11 mW
Glitch Time	0.08ns	0.56 ns
Glitch Period	10ns	10 ns
Delay	0.57ns	0.24 ns
Output Noise	-142.16db	-132.88 dB

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Authors

Anu Tonk, holds a B. Tech in Electronics & Communication Engineering from ASET, Amity University, Noida in 2012 and is currently persuing M. Tech in VLSI Design from YMCA University of Sciences and Technology, Faridabad.

Areas of Research interests: VLSI Design, Nanoelectronics & Devices, Communication Engineering

Bal Krishan, received a B.E. degree in Electronics & Communication Engineering from CRCE (Now DCRUST University), Murthal, Sonepat, Haryana in 1997 and M.Tech in Nanotechnology from Jamia Millia University, Delhi in 2009. He has presented a number of research papers in various National & International conferences and has to his credit published papers in research Journals. He is pursuing PhD in the field of Nanoelectronics from YMCA University of Sciences and Technology, Faridabad (Haryana). Presently he is working as Assistant Professor, Electronics Engineering Department, YMCA UST, Faridabad, Haryana.

