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Design of a ROM-Less Direct Digital Frequency Synthesizer on FPGA

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Abstract

DDFS (Direct Digital Frequency Synthesizer) is a new technique of frequency synthesizes which introduces the advanced digital processing theory into frequency synthesis. A direct digital frequency synthesizer is composed of a phase accumulator, an adder, an ROM for wave pattern saving, a D/A converter and a LPF (low pass filter). With the rapid development of VLSI, the speed of algorithm is required increasingly higher. This paper proposes a new frequency synthesizer by improving the structure of data storage which ensures the accuracy and speed. Rotation method was used to resolve the expected angle into many small rotation angles and sting wave symmetry principle was used to resolve the string wave. From point to area, the values in one quadrant were calculated and sampled and then the data was saved in ROM. Under the control of frequency, the data in ROM was read and then transferred to the D/A converter chip and the following low pass filter to achieve frequency synthesize. This algorithm could reduce the usage of ROM to increase the calculation efficiency.

Keywords: *string wave, digital frequency synthesizes, usage efficiency, Verilog, FPGA*

1. Introduction

Frequency synthesizer is the device that utilizes one or more standard signals to produce discrete frequency signals with algorithms. DDS technique is the third-generation frequency-synthesis technique after digital integrated circuit and microelectronic technology and it's developing rapidly. It's based on digital signal processing to synthesize frequency from the phase-frequency characteristic of signals. It has high frequency resolution ratio, short frequency conversion time, wide relative bandwidth, continuous phase signal. The output capacity of arbitrary waveform and digital modulation and is widely used in instruments, remote communication, radar, electronic countermeasure, navigation, radio and television. Especially in short wave frequency hopping communication, the signal is changing within wide frequency bandwidth and is required to quickly switch frequency and phase position in small frequency interval. So the intrinsic signal source utilizing DDS technique is an ideal choice [1].

DDS has an advantage in producing common signals with fewer devices and can be used in various system modules. But traditional DDS has low efficiency and accuracy. The design and realization of an improved harmonic signal generator is reported here. It focuses on the improvement of frequency accuracy and compression of memory capacity. It's proved that with the improvement of structure and the introduction of new algorithms, the compression of memory capacity is achieved without damaging the system speed and stability [2, 3].

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2. Frequency Synthesizer

In the early stage high-frequency acceptor, only expensive quartz oscillator can be used to produce resonant circuit and now can be replaced by frequency synthesizer. Initial frequency synthesis is proposed by H. J. Finder from Institute of Electrical and Electronics Engineers. To output one or more expected frequency, one or more frequency references are required. With its low cost and increasing efficiency, frequency synthesizer is widely used in communication devices. Frequency synthesizer is classified into three categories, DAS (Direct Analog Synthesis), DDFS and Indirect Frequency Synthesis.

2.1. Direct Analog Synthesis

Direct Analog Frequency Synthesis is the earliest frequency synthesis technique and composed of harmonic generation circuit, band pass filter circuit, mixer circuit, doubling circuit and produces the expected frequency from one or more reference frequency signals. From the point of phase position, it can be classed as coherent and incoherent. The difference is that only one reference frequency source is required to acquire plural output frequency for the former one, while more are needed for the latter one [1].

Asynchronous frequency synthesizer needs many reference frequencies and is composed of switch, oscillator, mixer, band pass filter. And the accuracy and stability is determined by quartz [2]. More vibration-mixing circuits can be used to get a wider frequency range as shown in Figure 1.

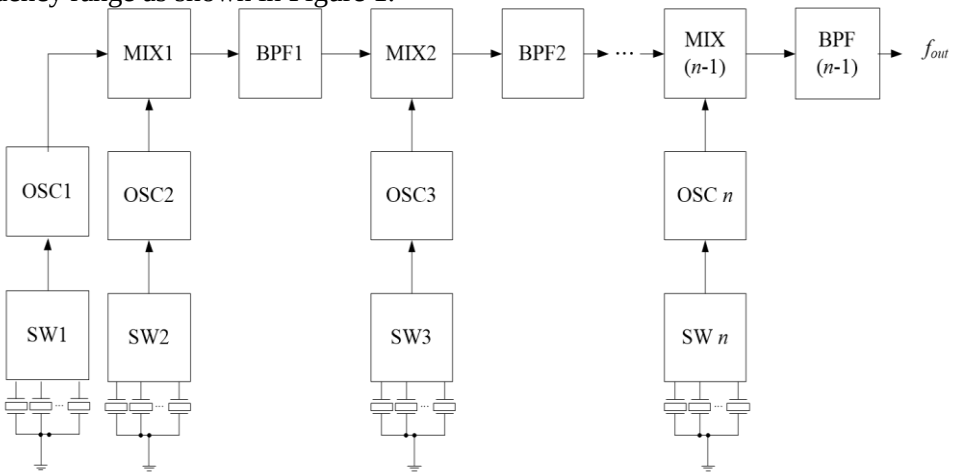

Figure 1. The Diagram of Asynchronous Frequency Synthesizer

Synchronous frequency synthesizer only needs one frequency reference source and is composed of mixer, band pass filter and divider. The structure of a synchronous frequency synthesizer is shown in Figure 2.

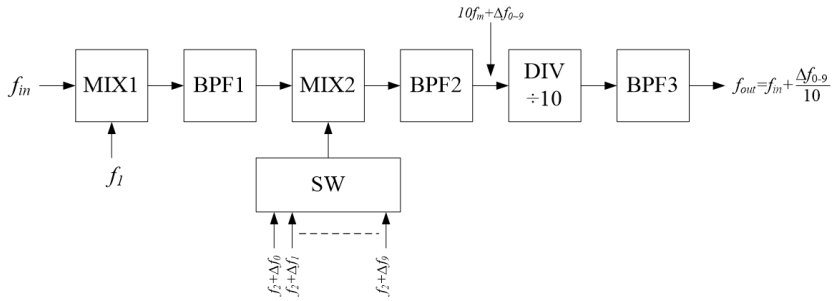

Figure 2. The Diagram of Synchronous Frequency Synthesizer

2.2Indirect Frequency Synthesis

Indirect Frequency Synthesis uses the Phase Locked Loop principle to achieve frequency synthesize, as shown in Figure 3. It' s feedback control system [1].

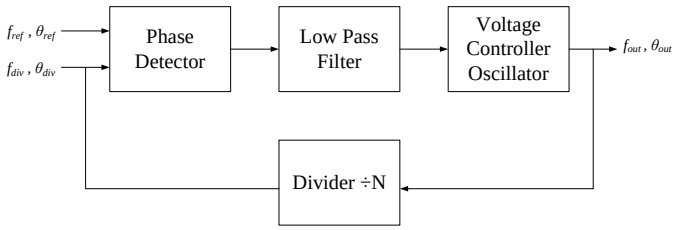

Figure 3. The Structure of the Phase Locked Loop

2.3Direct Digital Frequency Synthesis

Direct digital frequency synthesis firstly stores the function value of one cycle into string wave generator, and then the phases are accumulated by the phase accumulator. The corresponding address signal is output according to the final phase position. The string wave generator outputs the function amplitude stored in ROM using the address with look-up Table method. The wave is got via the digital analog converter. Finally, the expected frequency is got via the low pass filter. The basic structure is shown in Figure 4. Phase accumulator and string wave generator are the most important modules in the structure of direct digital frequency synthesis.

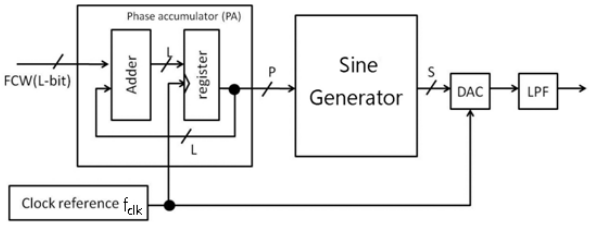

Figure 4. The Basic Structure of Direct Digital Frequency Synthesis

The phase accumulator is a controller with a slope of the curve. The output is a curve with P digits. And the slope is controlled by the Frequency Control Word with L digits [3]. The output diagram is shown in Figure 5.

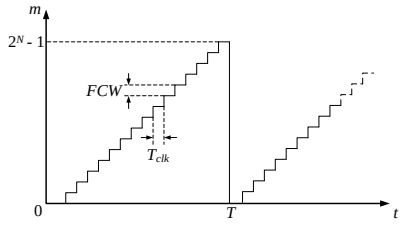

Figure 5. The Output Diagram of a Phase Accumulator

As the working frequency of the phase accumulator is fclk, after one cycle, the Frequency Control Word is added by one. The output efficiency of direct digital frequency synthesis is show in (1).

$$f_{out} = f_{clk} \times FCW / 2^l \qquad (1)$$

So the output efficiency is proportional to the Frequency Control Word. During the frequency synthesis process, the sample frequency is fixed, so it's the Output frequency resolution that determines the change of Frequency Control Word. As shown in Figure 6.

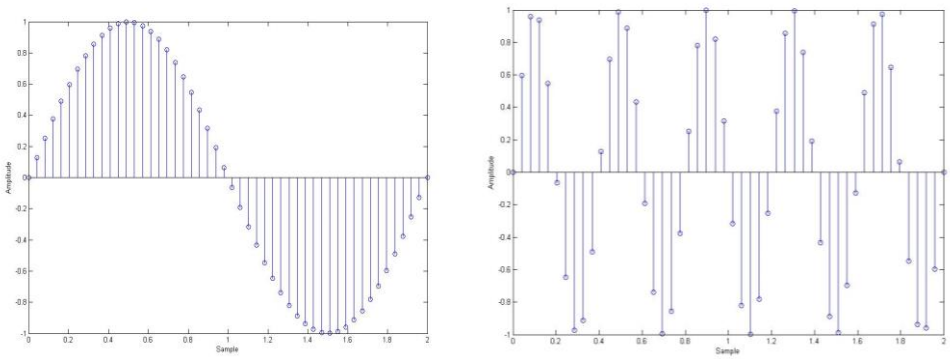

Figure 6. The Influence of Frequency Control Word on Output Frequency Resolution

String wave generator is also called PSAC (Phase-to-sinusoid Amplitude Convertor). We can regard the phase accumulator as a ROM. Digital sinusoidal waveform with S digits is stored in the phase accumulator and it's S×2L digits for the ROM. The ROM size is reduced without decreasing the resolution and the output of phase accumulator is reduced to P digits. The outcome of phase truncation is that the size of ROM is reduced to S×2L digits. In the direct digital frequency synthesis, the waveform generator is the chief module to limit the working frequency and efficiency loss.

2.4 The Design of String Wave Generator

The string wave generator is used to produce the electrical signal with particular parameters for the circuits. It can be divided into sine wave signal generator, rectangle pulse signal generator, function signal generator and random signal generator according to the wave form. The initial direct digital frequency synthesizer uses read only memory look-up Table method to produce string wave signal. Although phase reduction and string wave symmetry characteristics are used to save the read only memory, it still costs much storage space. And too large-size read only memory may cause the slow operating speed and high energy loss of direct digital frequency synthesizer. So the ways to reduce the size of memorizer are proposed included angular decomposition, angular rotation, multipartite Table method, and polynomial approximations [4]. This paper is based on angular rotation to design and realize the string wave generator.

Angular rotation method uses the algorithm named as CORDIC (Coordinate Rotation Digital Computer). CORDIC decompose the expected angle into some preliminary basic rotation angles. And the rotation motion can be achieved by simple shift and add/subtract operation. Angular rotation algorithm carries out continuous angular rotation until the angle of rotation equals to the input angle. The output is the sine and cosine value of the input angle [5, 6].

The process to calculate the sine and cosine value is equal to calculate the point ($X\theta$,$Y\theta$) in the unit circle in Figure 7. We started from point (X0,Y0)=(1,0).

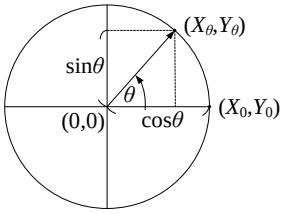

Figure 7. The Schematic Diagram of Angle θ

As shown in Figure 7:

$$\begin{bmatrix} X_\theta \\ Y_\theta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} = \cos \begin{bmatrix} 1 & -\tan\theta \\ \tan\theta & 1 \end{bmatrix} \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} \tag{2}$$

It's shown in Figure 8 that the angle of rotation θ into N digressive small rotation angles θn

$$\theta = \sum_{k=0}^{N-1} \delta_i \theta_i \ , \quad \theta_i \geq 0 \tag{3}$$

δi is -1 when θi rotations clockwise and 1 when Θ i rotations anticlockwise.

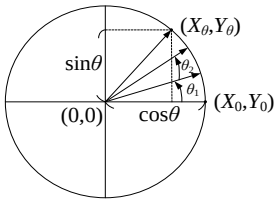

Fig 8.he Disintegration of the Rotation Angle For the small rotation

$$\begin{bmatrix} X_{i+1} \\ Y_{i+1} \end{bmatrix} = \cos\theta_i \begin{bmatrix} 1 & -\delta_i \tan\theta_i \\ \delta_i \tan\theta_i & 1 \end{bmatrix} \begin{bmatrix} X_i \\ Y_i \end{bmatrix}, \ i = 0,1,2,\cdots N-1, \tag{4}$$

$$\theta_i = \arctan\left(2^{-i}\right), \quad i = 0,1,2,\cdots,N-1 \tag{5}$$

That is $\tan\theta_i = 2^{-i}$, then

$$\cos\theta_i = \frac{1}{\sqrt{1+\tan^2\theta_i}} = \frac{1}{\sqrt{1+2^{-2i}}}, \quad i = 0,1,2,\cdots N-1 \tag{6}$$

(4) can be written as

$$\begin{bmatrix} X_{i+1} \\ Y_{i+1} \end{bmatrix} = \cos\theta_i \begin{bmatrix} 1 & -\delta_i 2^{-i} \\ \delta_i 2^{-i} & 1 \end{bmatrix} \begin{bmatrix} X_i \\ Y_i \end{bmatrix}, \ i = 0,1,2,\cdots N-1, \tag{7}$$

So vector （X0,Y0） arrives at vector （Xθ,Yθ） after N-time rotation.

$$z_{i+1} = z_i - \delta_i \arctan(2^{-i}), \quad i = 0,1,2,\cdots N-1$$

$$\begin{aligned} \begin{bmatrix} X_\theta \\ Y_\theta \end{bmatrix} &= \left(\prod_{i=0}^{N-1} \cos\theta_i \begin{bmatrix} 1 & -\delta_i 2^{-i} \\ \delta_i 2^{-i} & 1 \end{bmatrix} \right) \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} \\ &= K \left(\prod_{i=0}^{N-1} \begin{bmatrix} 1 & -\delta_i 2^{-i} \\ \delta_i 2^{-i} & 1 \end{bmatrix} \right) \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix} \end{aligned} \tag{8}$$

K is the modulus correction factor, and

$$K = \frac{1}{P} \prod_{i=0}^{N-1} \cos\theta_i = \prod_{i=0}^{N-1} \frac{1}{\sqrt{1+2^{-2i}}} \tag{9}$$

When N→∞, K→0.607253, so it can be regarded as a constant.

So, the calculation of vector rotation (2) can be transformed to the calculation of (9) and the following iteration calculation.

$$\begin{aligned} x_{i+1} &= x_i - \delta_i y_i \cdot 2^{-i} \\ y_{i+1} &= y_i - \delta_i x_i \cdot 2^{-i}, \quad i = 0,1,2,\cdots,N-1 \end{aligned} \tag{10}$$

As (7) is a constant and can be predetermined, so only the calculation (10) is needed. In the iteration calculation, to follow the rotated angle, a new variable is introduced and defined as

$$z_{i+1} = z_i - \delta_i \arctan\left(2^{-i}\right), \quad i = 0,1,2,\cdots,N-1 \tag{11}$$

It represents the left angle to be rotated after i-time rotation. Arctan(2-i) can be predetermined and stored in the register. (10) and (11) constitute the basic iteration relation of CORDIC algorithm [7].

Equation (10) only contains shift, addition and subtraction operation and is suitable to be realized in hardware. This is the original intention of CORDIC algorithm. Figure 9 is the hardware construction of this algorithm. It' s realized by shifter and adder. As the hardware construction of multiplication is too complex and the operation speed is slow, so the multiplication is replaced by shifter to simplify Rotation Angle algorithm. This method can greatly simplify the complexity of operation structure and increase the operation speed.

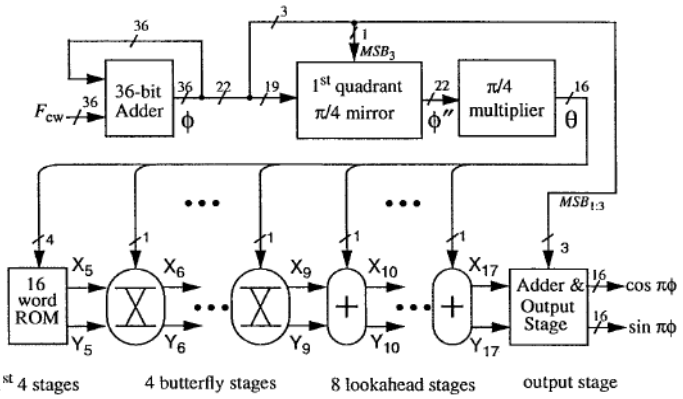

Figure 9. The Hardware Construction of Angular Rotation Method

2.5 Error Analysis

Although DDFS has high operation speed and simple structure, its Spectrum Purity is not good. And quantization error is the main factor that can influence the Spectrum Purity. Quantization error mainly occurs at the output point of phase position and amplitude of the phase accumulator, as shown in Figure 10.

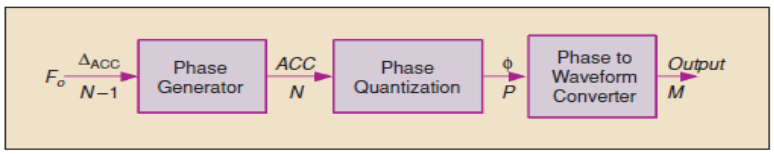

Figure 10. The Main Error Source of Direct Digital Frequency

The phase position input of direct digital frequency synthesizer is usually 16 digits or 32 digits. To reduce the size of ROM in the system structure, the digits are usually reduced, which causes the sampled phase position error [8].

The cause of the amplitude quantization error is that the data in digital system is expressed in limited digits, which results in error with the actual simulated data. Amplitude quantization error is caused by the limited digits to store the wave amplitude in the table system.

3.The Design and Realization of the Frequency Synthesizer

3.1The Application of String Wave Symmetry

The LUT (Look-Up Table) used in this article is to store a complete sine wave in ROM and 1/4 cycle is used to construct the whole wave according to the symmetry and repeatability of the wave to reduce the size of the memory. Figure 11 is the structure of the direct digital frequency synthesizer based on this idea [11], MSB1 and MSB2 are the highest point and the second highest point of phase accumulator, respectively and they are corresponding to the quadrant of the angle.

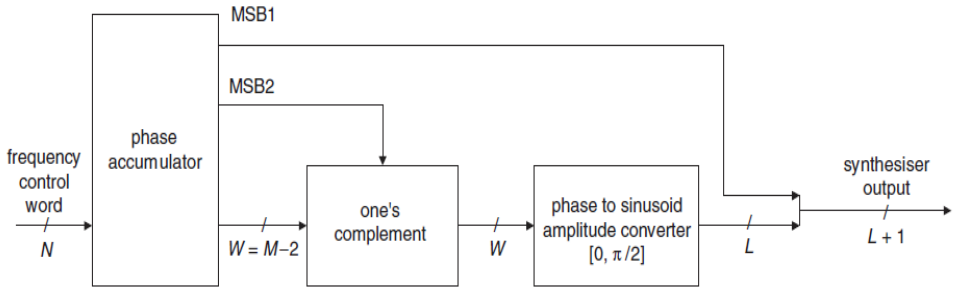

Figure 11. The Structure of the Direct Digital Frequency Synthesizer

The transformation of waveform is shown in Figure 12. First, a rectangle wave is produced through the phase. Then, through a phase position symmetry operation, a triangle wave is got. After the triangle wave is shaped by the converter, half-cycle sine wave can be got. Finally, through a negative transformation of the amplitude every other cycle, the sine wave can be got which is double of the triangle wave [9, 10].

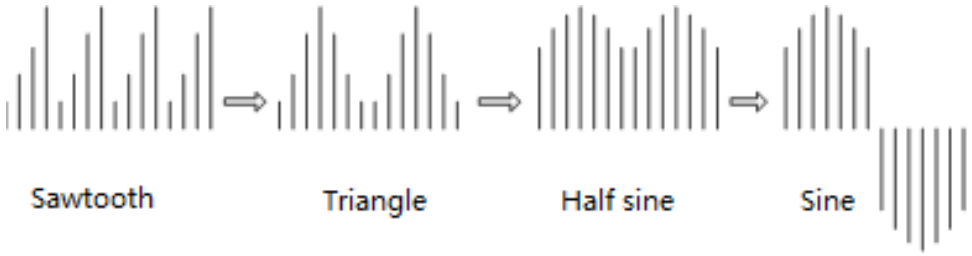

Figure 12. The Waveform Transformation Process of the Sine

3.2 The Improvement of Register

In this paper, the error compensation is stored in ROM and the simplify method is called bit reduction. The data will be stored in ROM except the first digit. The first digit is directly assigned by external circuit and combined with the data in ROM. This is used to judge the quadrant when the ROM is invoked. Take an ROM with 24×8 digits for an example, when the first n digits are all 0 or 1, then the n digits can be omitted. Then 2n×8 digits can be saved in ROM. This reduced ROM can be restored with shift register. So much ROM room can be saved with this method.

ROM is composed of column decoder, row decoder, core array, word-line buffer and clock buffer. Figure 13 is the basic structure of ROM. Its capacity is 2m × n digits. M is the number of address lines including row address and column address. N is the digits of output data. Phase position is used as address to read the table. Higher and higher required resolution, bigger and bigger the content of the table. It's exponential to the digits.

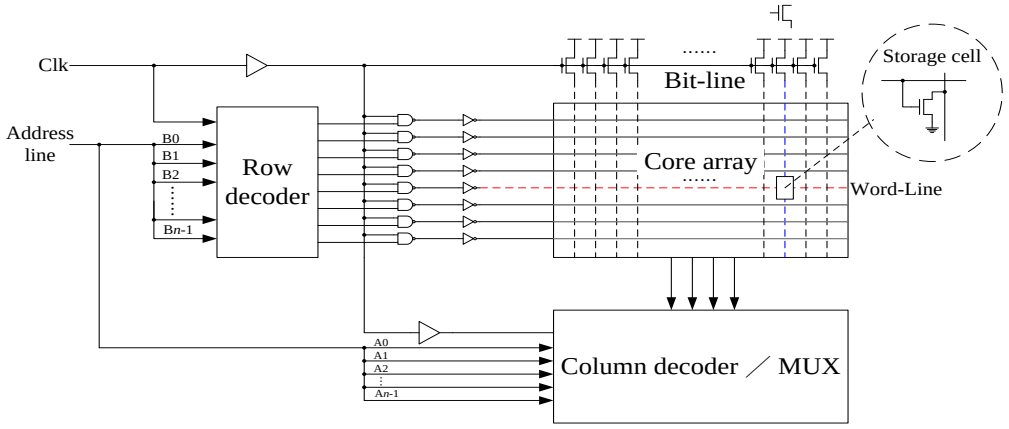

Figure 13. Basic Structure of ROM

The output is got by using the input angle to get the sin/cos value with Look-Up Table. Sin/cos is realized in ROM. The value of sin/cos in the first quadrant can reduce the size of ROM. When ROM works, the reading of data is done by selecting a word-line according to the column address. Then the row decoder selects n-digit data line according to row address to output. Usually the row address is high address and column address is low address. The cross of word-line and digit line is called core array, this is also where data is stored. The cells in the core array represent a digit data. The required data can be read by selecting the word-line and digit line. So through the planning of ROM, half-size ROM is needed [12].

3.3 The Realization of Frequency Synthesizer

Figure 14 is the complete structure of the circuit which can distinguish quadrant, invoke ROM, and combine ROM and output with two ROMs as the center.

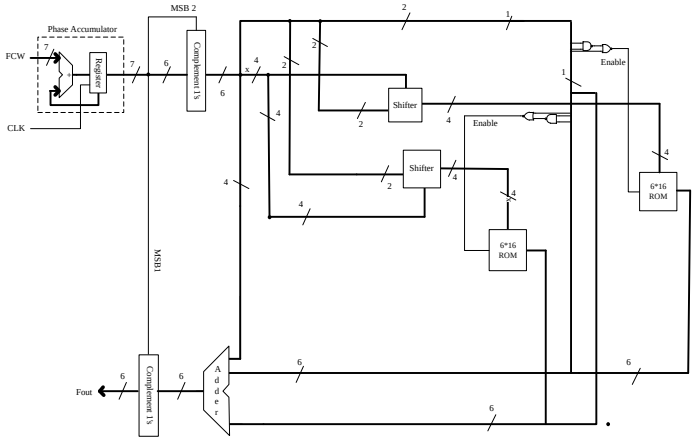

Figure 14. The Structure of the Frequency Generator

The circuit diagram is composed of three parts. The first part is input analysis including recognizing the quadrant and analyzing the input order. The second part is to invoke ROM to read data by analyzing the order. The third part is to calculate the final coordinate to add and input the value from ROM, as shown in Figure 15.

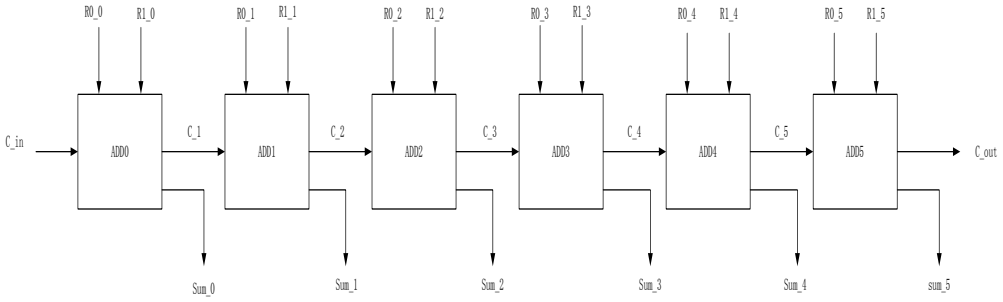

Figure 15. The Adder Module

From the three parts of the system, after the input is shifted in the shifter, the results are combined in the first and second parts or the first and third parts. This principle is shown in Figure 16. Two groups of addresses are got after shifting and then they're stored in ROM and added, and then output after being checked [13].

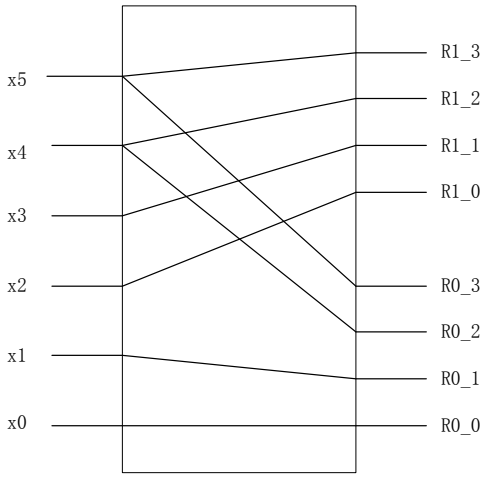

Figure 16. The Principle Diagram of the Shifter

4. The Simulation and Assessment of the Frequency Synthesizer

Verilog HDL is a hardware describing language developed from C language program and its grammar is free. It describes the structure and behavior of digital system hardware with text form. It can be used to show logic circuit diagram, logic equation, and the logic function fulfilled by digital logical system. Verilog HDL is used in this design.

ISE (Integrated Software Environment) is the hardware design tool developed by Xilinx and has the best reputed PLD design environment. ISE was used in this article to assess the design. The assessment includes comprehensive simulation and functional simulation. Functional simulation means to simulate the logical function of the designed circuit to test if it can meet the design requirement. Usually the waveform can directly show the relation between the input and the output signal [14].

To achieve the function with the simplest programming, verilog is used to construct the top module of the direct frequency synthesizer. Two ROMs are invoked in the top module. Then test bench is constructed. Input the address into test bench and get the output. Then the simulation is done in ISE.

4.1 Design of the Frequency Generator

The main module is shown in Figure 17 and it's the structure of direct digital frequency synthesizer in this paper. This module also includes the clock, which is used for assessing the test bench and the trigger of the driving module in the main module.

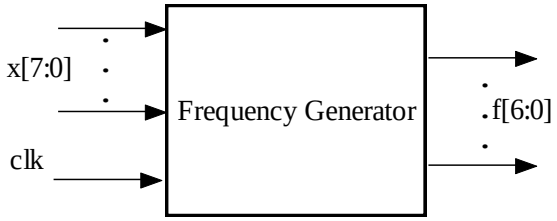

Figure 17. The Ports of the Frequency Generator

Figure 18 shows the submodule created in the test. The submodule deals with 6 signals, so it's invoked 6 times. The output corresponding to different input is the data we need [15].

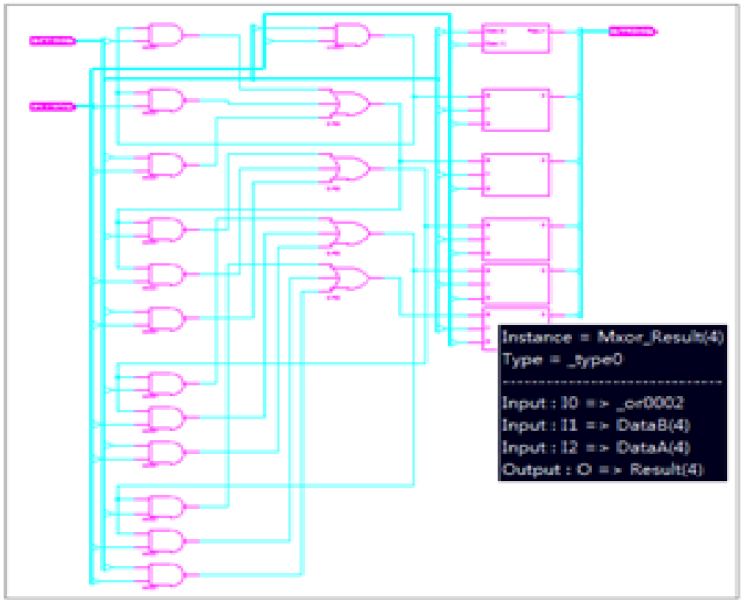

Figure 18. The Logic Structure of the Submodule

4.2 The FPGA Realization of the Frequency Synthesizer

FPGA (Field Programmable Gate Array) is one of the semi-custom made circuits in ASIC (Application Specific Integrated Circuit). It resolves the short point of custom made circuits and the limited gate circuits in programmable devices. FPGA has all the function of digital devices from high-performance CPU to simple 74 series circuits. With FPGA to develop digital circuits, we can save the designing time, reduce the area of PCB, increase the stability of the system. System designers can link the logic blocks in the FPGA with programmable connection, as a circuit breadboard is put into a chip. The logic blocks and link can be changed at the designer's will, so FPGA can fulfill the logic function required [16].

The circuit design based on Verilog can be quickly programmed into FPGA to test with simple planning and is the popular technique in modern IC design. These programmable devices can be used to realize some basic logic gate circuits, like AND, OR, XOR, NOT, or more complex combination function such as decoder or mathematical equations. In

most of the FPGA, these programmable devices also include memory elements such as Flip-flop or other complete memory blocks.

In the hardware realization of FPGA, the selection of proper chip is also a very important part of the work and is the basis of the design. The major process is choosing proper FPGA chip manufacture, FPGA chip series, and FPGA chip model. Considering the size of the system and the production upgrade, the EPlC4F400C6 chip in Cyclone series is chosen.

4.3 The Result and Analysis of Simulation

This is the functional test of the structure of the frequency synthesizer of the devices with ISE. The wave form is shown in Figure 19.

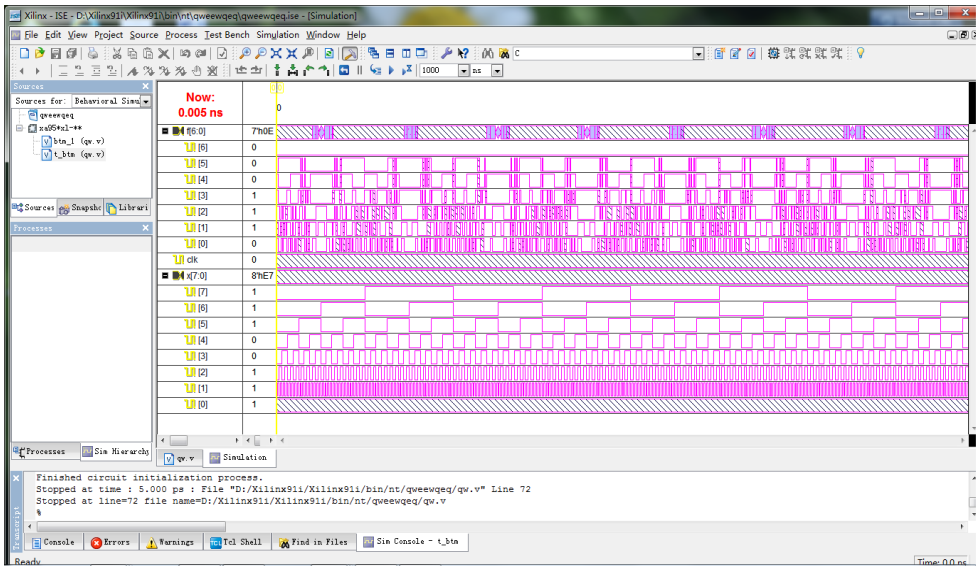

Figure 19. The Waveform of the Digital Simulation

By changing the frequency word, we verified the function of DDS with different frequency, the simulation results of 1200KHz and 10KHz sine wave was shown in Figures 20 and 21.

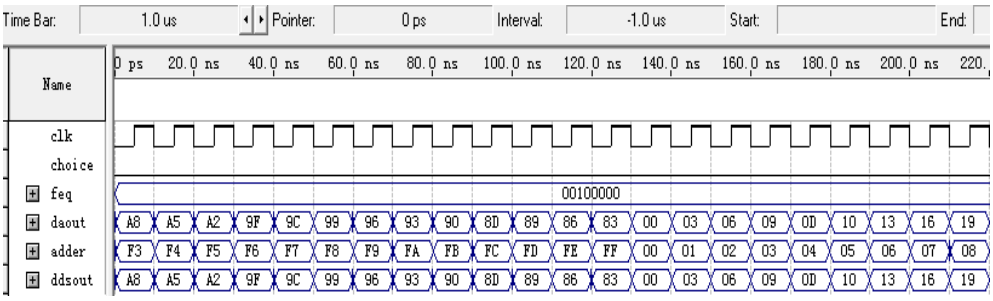

Figure 20. Result of 1200KHZ Sine Wave

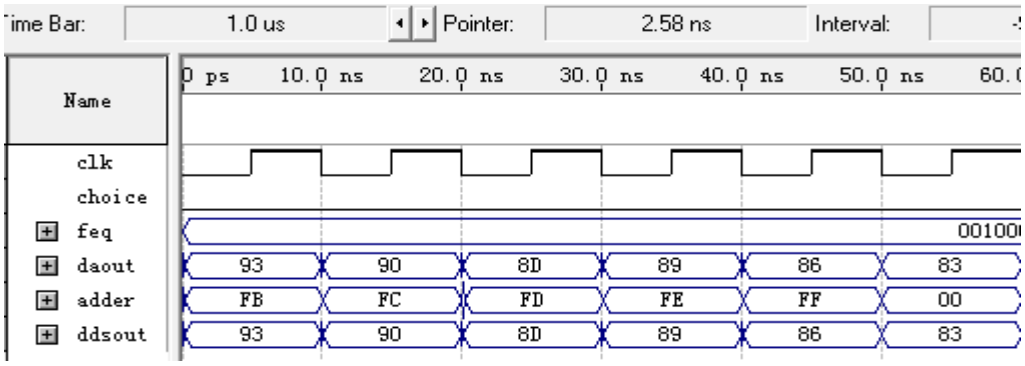

Figure 21. Result of 10kHZ Sine Wave

As shown in the above two figures, the output frequency is as same as the one provide by frequency control word, and the result is right. The amplitude corresponds to the number stored in the ROM. The DDS also got high frequency accuracy and met the requirements basically.

5. Conclusions

In recent years, with the development of ultra-high-speed digital circuits and in-depth study of the DDS, the speed of DDS is more and more crucial. The study found that, in the process of compositing waveform by looking up table, the speed of DDS is restricted to the speed of accessing ROM. In this paper, we improved the ROM frame of traditional DDS based on the work mode of phase accumulator pipeline. The proposal of combination the ROM data and external data assignment, which reduced the times of ROM accessing, enhanced the speed of DDS. The theoretical analysis and design of a new direct digital frequency synthesizer is completed. The simulation of hardware and software is also done. The results show that the size of ROM is reduced without reducing the working frequency of DDS and damaging the accuracy. As while as, the operating speed of the system is improved, and the power consumption is reduced. It's provides a new insight to embed DDS into computer system.

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