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Assessment of Single Phase Cascaded Multilevel Inverter using Equal and Unequal Amplitude Carriers

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Abstract

This work presents the comparison of various multicarrier based Pulse Width Modulation (PWM) techniques for the chosen single phase CMLI (Cascaded Multi Level Inverter). In this paper, a single phase symmetrical cascaded multilevel inverter is controlled with sinusoidal, THI (Third Harmonic Injection), Trapezoidal, TAR (Trapezoidal Amalgamated Reference) and Stepped Wave reference with Equal Amplitude Carriers (EAC) and UEAC (Un Equal Amplitude Carriers). The proposed EAC and UEAC are applied for various PWM strategies. The PWM methods used for the analysis are PD (Phase Disposition) PWM, POD (Phase Opposition and Disposition) PWM, APOD (Alternative Phase Opposition and Disposition) PWM, CO (Carrier Overlapping) PWM, PS (Phase Shift) PWM and VF (Variable Frequency) PWM with EAC and UEAC. For all the PWM methods and references the UEAC produces less THD and higher fundamental RMS (Root Mean Square) values except for m_a =1. For m_a =1 the EAC provides less THD (Total Harmonic Distortion) and higher fundamental RMS (Root Mean Square) values for all the PWM methods and references. To validate the developed technique, simulations are carried out through MATLAB/SIMULINK.

Keywords: *Equal Amplitude, Unequal, Variable Frequency, THD, CMLI*

1. Introduction

MLIs (Multi Level Inverter) have been extensively used in high power applications because they can realize high voltage and high power output through the use of semiconductor switches without use of transformer and without dynamic voltage balance circuits. Single phase five level inverter topology are discussed in this paper. Various bipolar multi-carrier modulation strategies with sine, trapezoidal, TAR, THI and stepped wave reference have been developed using MATLAB-SIMULINK /R2012a/March 2012. and tested for different modulation indices with equal and unequal amplitude carriers.

Nabae, *et al.*, [1] suggested a new neutral-point-clamped Pulse Width Modulation (PWM) inverter composed of main switching devices which operate as switches for PWM and auxiliary switching devices to clamp the output terminal potential to the neutral point potential has been developed. This inverter output contains less harmonic content as compared with that of a conventional type. Two inverters are compared analytically and experimentally. In addition, a new PWM technique suitable for an ac drive system is applied to this inverter. The neutral-point-clamped PWM inverter adopting the new PWM technique shows excellent drive system efficiency, including motor efficiency, and is appropriate for a wide-range variable-speed drive system. Takahashi and Mochikawa [2] introduced a simplified method to calculate harmonic currents of an induction motor and optimum PWM switching patterns to minimize the harmonic loss are presented. Neglecting the harmonic iron loss, the harmonic loss of the motor is proportional to the

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square of the rms current. The waveform of the harmonic current is approximately equal to that of the leakage reactance applied to the same PWM voltage. Its approximation error is very small under normal operating condition. The main results obtained using these approximation are as follows: 1) the optimum PWM patterns of the pulse number from seven to 41; 2) how to choose the optimum pattern and calculate it by using a computer; 3) the effect of a resistance of the windings and skin effect of the secondary conductor; and 4) microcomputer PWM optimum voltage control schemes. Comparison with other controls is shown by using experimental and calculating results and confirms the effectiveness of this control scheme. Carrara, *et al.,* [3] gave idea about generalization of the pulsewidth modulation (PWM) sub harmonic method to control single-phase or three-phase multilevel Voltage Source Inverters (VSI) is considered. An analytical expression of the spectral components of the output waveforms covering all the operating conditions is derived. The analysis is based on an extension of Bennet's method. The improvements in harmonic spectrum are pointed out, and several examples are presented, which prove the validity of the multilevel modulation. Peng and Lai [4] discussed multilevel voltage source converters which emerging as a new breed of power converter options for high-power applications. The multilevel voltage source converters typically synthesize the staircase voltage wave from several levels of DC capacitor voltages. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The techniques to balance the voltage between different levels normally involve voltage clamping or capacitor charge control. There are several ways of implementing voltage balance in multilevel converters. Without considering the traditional magnetic coupled converters, this paper presents three recently developed multilevel voltage source converters: (1) diode-clamp, (2) flying-capacitors, and (3) cascaded-inverters with separate DC sources. The operating principle, features, constraints, and potential applications of these converters are discussed. Kang and Hyun [5] proposed a simplified method to calculate the relation between the reference phase voltage and the output phase voltage to the load neutral point. Boora, *et al.,* [6] proposes a new single inductor multi output DC/DC converter that can control the dc link voltages of single-phase diode-clamped inverter asymmetrically to achieve voltage quality enhancements. Namei, *et al.,* [7] developed a hybrid cascaded converter topology with series connected symmetrical and asymmetrical diode clamped H-bridge cells. Pereda and Dixon [8] suggested a solution for using only one dc source in asymmetric cascaded multilevel inverter. Najafi and Yatim [9] developed a new multilevel inverter which is used to reduce complexity and gate circuit. Kangarlu, *et al.,* [10] proposes a new topology with reduced number of switches which is used to operate in high power, high voltage, improved output waveform quality and flexibility. Judi and Nowicki [11] propose bypass technique for multi level inverter to ensure even power distribution in all voltages sources. Kangarlu and Babaei [12] developed an optimal structure in different criteria such as number of switches; standing voltage on the switches, number of dc voltage sources, *etc.* Babaei, *et al.,* [13] proposed anew algorithm to determine magnitude of dc voltage source. Palanivel and Dash [14] developed using carrier pulse width modulation technique which is used for lower magnetic interference and high output voltages. Babaei, *et al.,* [15] introduced a new single-phase cascaded multilevel inverter is proposed. This inverter is comprised of a series connection of the proposed basic unit and is able to only generate positive levels at the output. Therefore, an H-bridge is added to the proposed inverter. This inverter is called the developed cascaded multilevel inverter. In order to generate all voltage levels (even and odd) at the output, four different algorithms are proposed to determine the magnitude of dc voltage sources. Reduction in the number of power switches, driver circuits, and dc voltage sources is the advantage of the developed single-phase cascaded multilevel inverter. As a result, the installation space and cost of the inverter are reduced. These features are obtained by the comparison of the conventional cascaded multilevel inverters with the proposed cascaded topology. The ability of the proposed inverter to

generate all voltage levels (even and odd) is reconfirmed by using the experimental results of a 15-level inverter. Selvamuthukumaran, *et al.*, [16] proposes a hybrid multicarrier pulse width modulation (H-MCPWM) technique to reduce leakage current in a transformer less cascaded multilevel inverter for photovoltaic (PV) systems. The transformer less PV inverter topology has the advantages of simple structure, low weight and provides higher efficiency. However, the topology makes a path for leakage current to flow through parasitic capacitance formed between the PV module and the ground. A modulation technique has significant impact to reduce the leakage current without adding any extra component. The proposed H-MCPWM technique ensures low leakage current in the transformer less PV inverter system with simplicity in implementation of the modulation technique using lesser number of carriers. Experimental prototype developed in the laboratory demonstrates the performance of the proposed modulation technique in reducing the leakage current.

2. Proposed Topology

The main feature of a MLI is its ability to reduce the voltage stress on each power device due to the utilization of multiple DC sources. Though there are several types of MLI, the configuration of Modular Structured Multilevel Inverter (MSMI) also called cascaded type is unique when compared to other types of multilevel inverter in the sense that it consists of several modules that require SDCS. The function of this MLI is to synthesize a desired voltage from SDCS which may be batteries, fuel cells or solar cells. The number of modules (M) which is equal to the number of DC sources required depends on the number of levels (m) in the output of the MSMI. M and m are related by m=2M+1. For output voltage consisting of five levels, which are $+2V_{dc}$, $+V_{dc}$, 0,$-V_{dc}$ and $-2V_{dc}$, the number of modules required in the MSMI is two. Compared to other types of MLI, the MSMI requires less number of components with no extra clamping diodes or voltage balancing capacitors that only further complicate the overall inverter operation. Each module of MSMI has the same structure whereby it is represented by a single phase full bridge inverter. This simple modular structure not only allows practically unlimited number of levels for the MSMI by stacking up the modules but also facilitates its packaging.

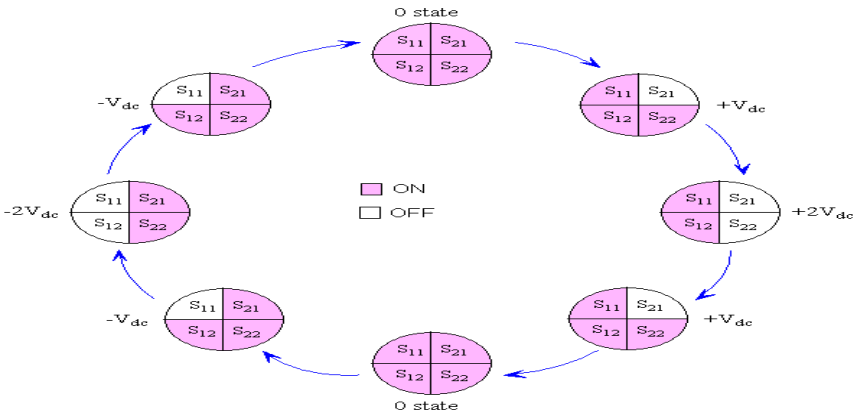

Figure 1. Cyclic Switching Sequence of Chosen MSMI

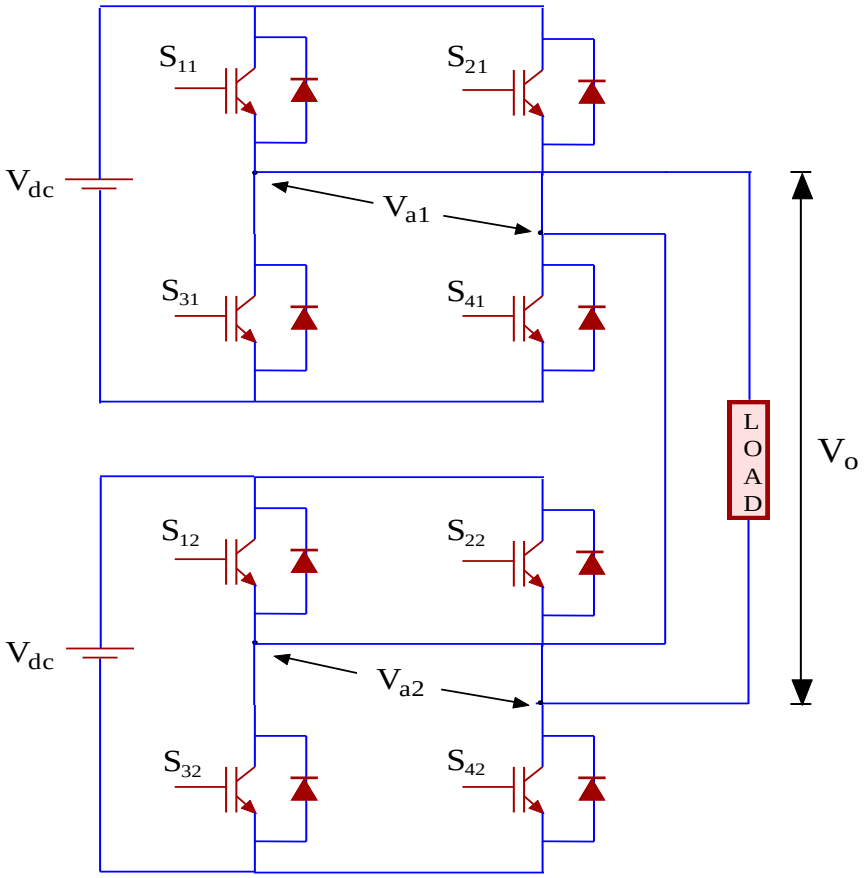

Figure 2. Five Level Cascaded Inverter

Figure 1 shows the possible switching states for the single phase five level inverter. The cascaded MLI can be used as compensator in power systems because it does not present unbalance problem in DC source. The structure of separate DC sources is well suited for various renewable energy sources such as fuel cell, photo voltaic cell and biomass cell. Figure 2 display the power circuit for single phase five level cascaded inverter.

3. Modulation Strategy

In these proposed topology they are two methods are used
1. Equal Amplitude Carriers
2. Un Equal Amplitude Carriers (or) Variable Amplitude Carriers (VAC)

3.1. Equal Amplitude Carriers (EAC)

In this method, all the triangular carriers used will have the same amplitude. The proposed PWM methods are PDPWM, PODPWM, APODPWM, COPWM, PSPWM and VFPWM with sine, THI, trapezoidal, TAR and stepped wave references. Figure 3 to 5 shows the sample carrier arrangement, output voltage and FFT plot for PDPWM strategy with sine reference (m_a = 0.8 and m_f=20). Where m_a and m_f are the amplitude and frequency modulation index.

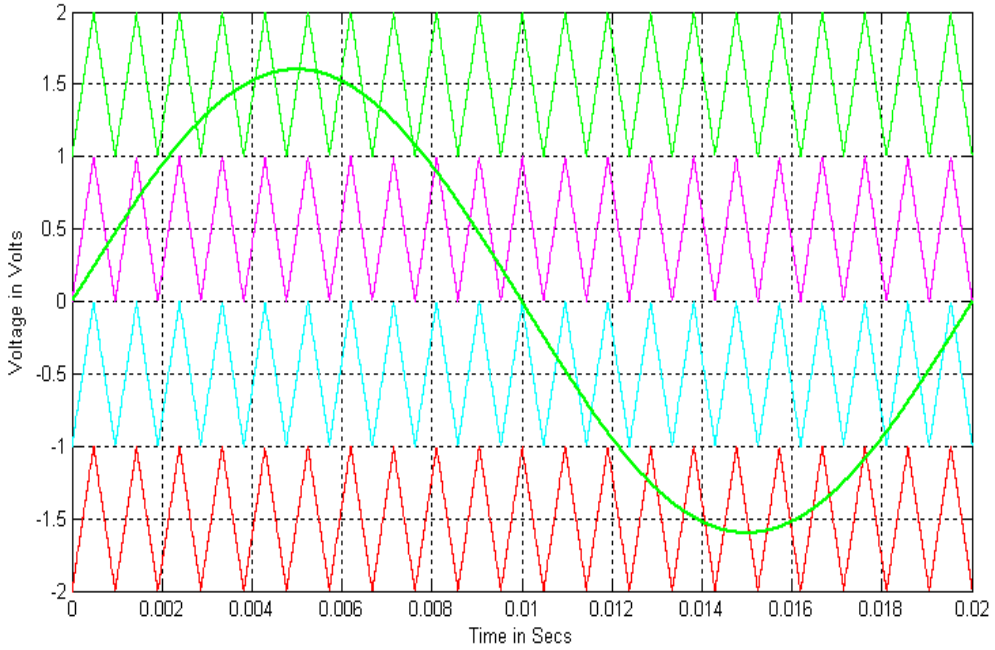

Figure 3. Sample Carrier Arrangement for Equal Amplitude Carriers with PDPWM Strategy (Sine Reference for m_a = 0.8 and m_f =20)

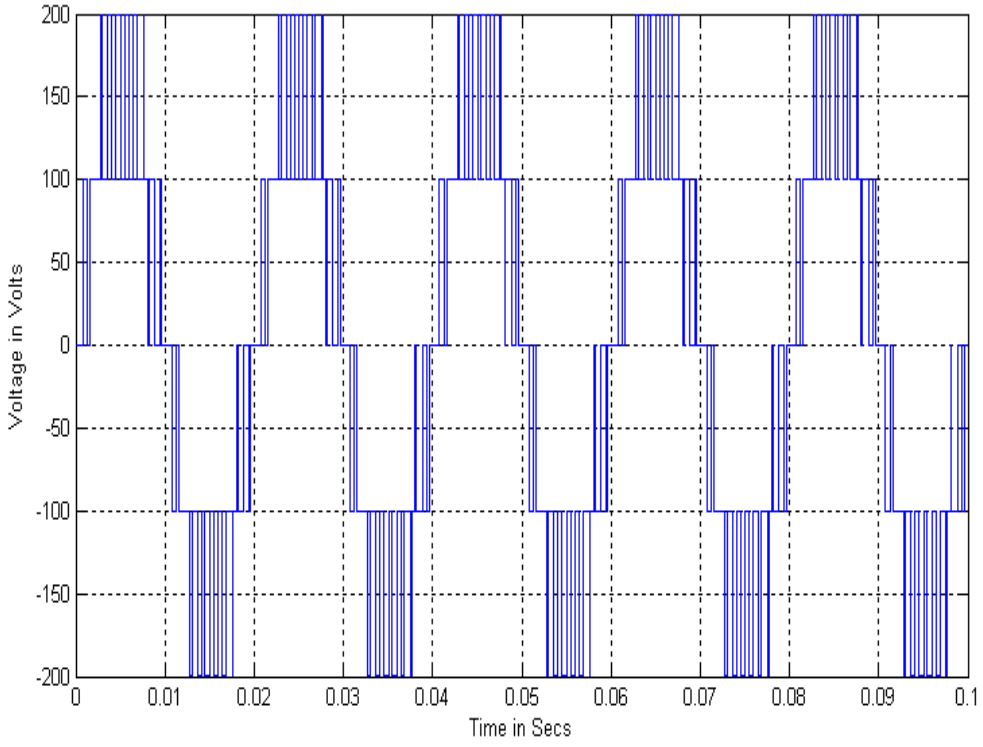

Figure 4. Output Voltage of Five Level Inverter based on Equal Amplitude Carriers with PDPWM Strategy (Sine Reference for m_a = 0.8 and m_f =20)

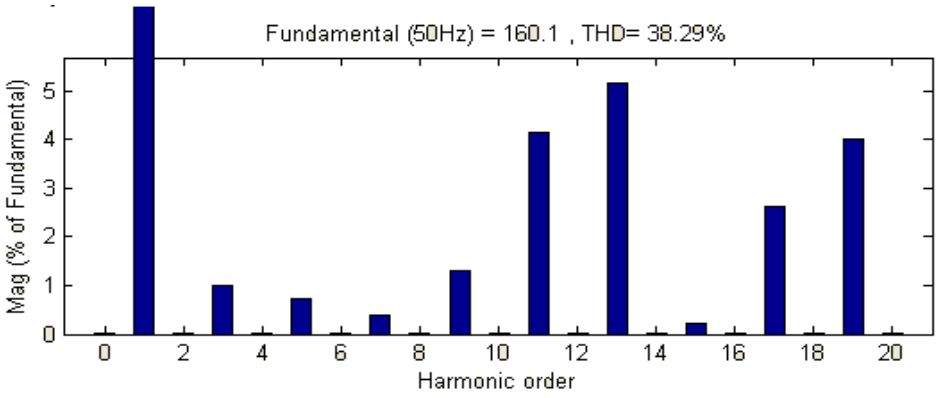

Figure 5. THD Plot for Five Level Output Voltage based on Equal Amplitude Carriers with PDPWM Strategy (Sine Reference for m_a = 0.8 and m_f=20)

3.2. Un Equal Amplitude Carriers (UEAC) (or) Variable Amplitude Carriers (VAC)

In this method, all the triangular carriers used will not have the same amplitude. The PWM methods used are UEAPD (Un Equal Amplitude Phase Disposition) PWM, UEAPODPWM, UEAAPODPWM, UEACOPWM, UEAPSPWM and UEAVFPWM with sine, THI, trapezoidal, TAR and stepped wave references. Figure 6 to 8 shows the sample carrier arrangement, output voltage and FFT plot for PDPWM strategy with sine reference (m_a = 0.8 and m_f=20). Figures 9 to 12 show the sample reference waveforms. The following parameters are used for the simulation V_{dc1} = V_{dc2} = 100V, R (Resistance) = 100 ohms, A_c (Amplitude of the carrier signal) = 0.5, 1 and 1.5, A_m (Amplitude of the modulating signal = 2, f_c (frequency of the carrier signal) = 1000 Hz and 2000Hz and f_m (frequency of the modulating signal) = 50 Hz. m_a is varied from 1 to 0.6 for equal amplitude carrier methods. In EAC method if m_a is varied from 1 to 0.51 then the inverter will work as a five level inverter and if the m_a is varied from 0.5 to zero then the inverter will work as a three level inverter. But in case of UEAC method if m_a is varied from 1 to 0.26 then the inverter will work as a five level inverter and if the m_a is varied from 0.25 to zero then the inverter will work as a three level inverter. This paper focuses on bipolar carrier with sinusoidal, third harmonic injection, trapezoidal, TAR and stepped wave reference function. Four carriers are not equal in amplitude. Intermediate carriers below and above zero level have half the amplitude of the outermost two carriers. Simulations are performed with different values of m_a ranging from 0.25 to 1. In paper m_f is chosen as 20 as a trade off in view of the following reasons: (i) to reduce switching losses (which may be high at large m_f) (ii) to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies (iii) to effectively utilize the available FPGA/dSPACE system for hardware implementation. The simulated output voltages are shown for only one sample value of m_a=0.8. For the single phase system the carrier frequency is limited up to 1000Hz. For the three phase system the carrier frequency range may be from 2 KHz to 10 KHz. In this paper we have chosen carrier frequency as 1 KHz. So the frequency modulation index is 20.

Where

$$m_a = \frac{A_m}{A_c} \quad - \quad (1)$$

$$m_f = \frac{f_c}{f_m} \quad - \quad (2)$$

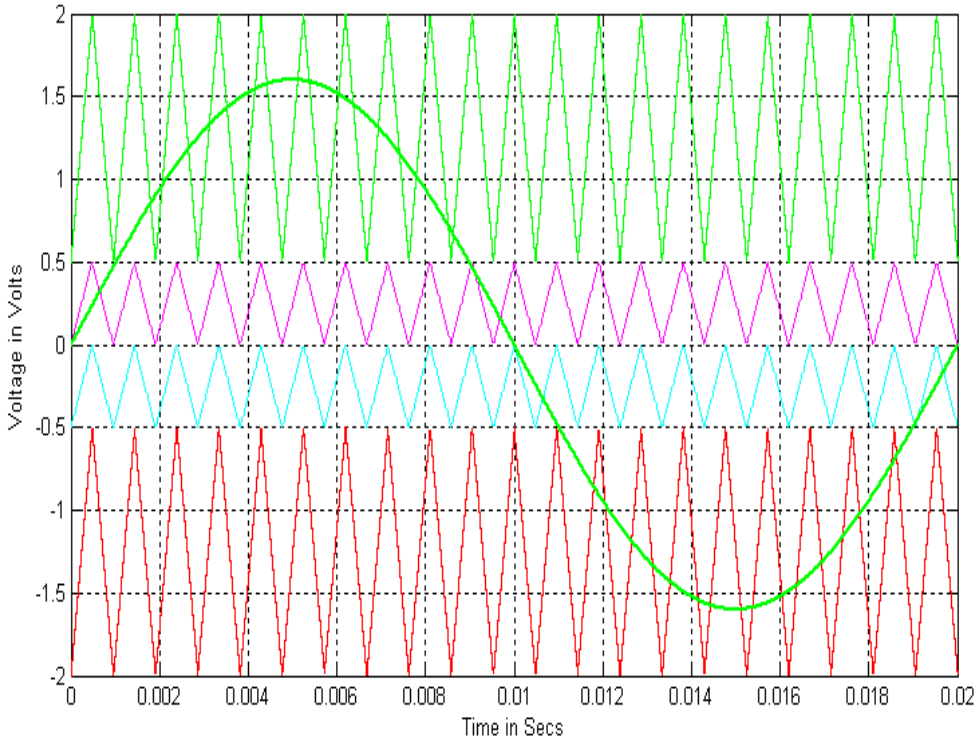

Figure 6. Sample Carrier Arrangement for Unequal Amplitude Carriers with PDPWM Strategy (Sine Reference for m_a = 0.8 and m_f =20)

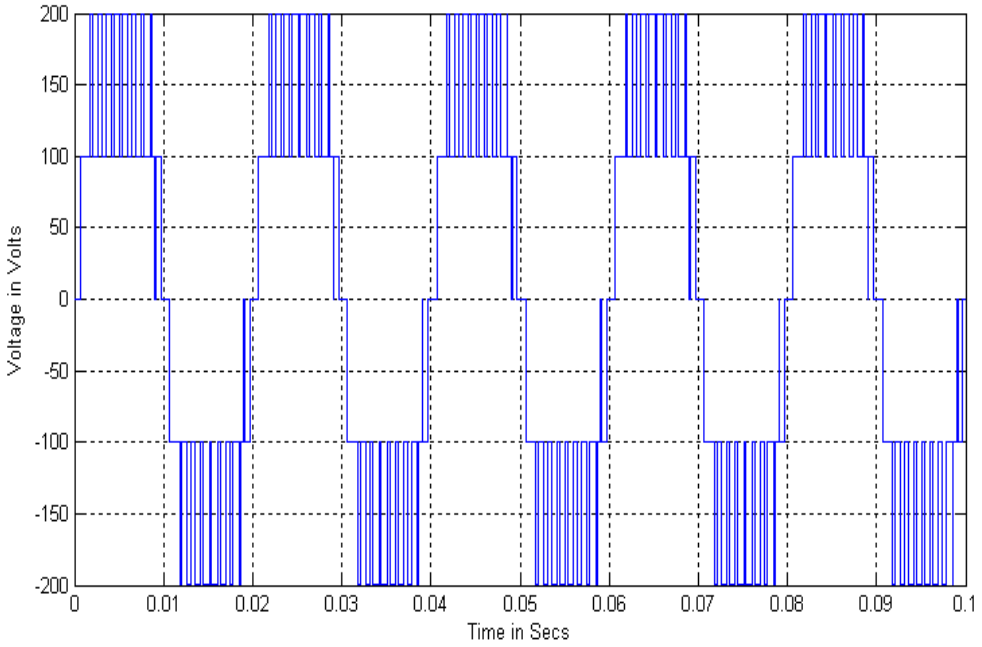

Figure 7. Output Voltage of Five Level Inverter based on Unequal Amplitude Carriers with PDPWM Strategy (Sine Reference for m_a = 0.8 and m_f =20)

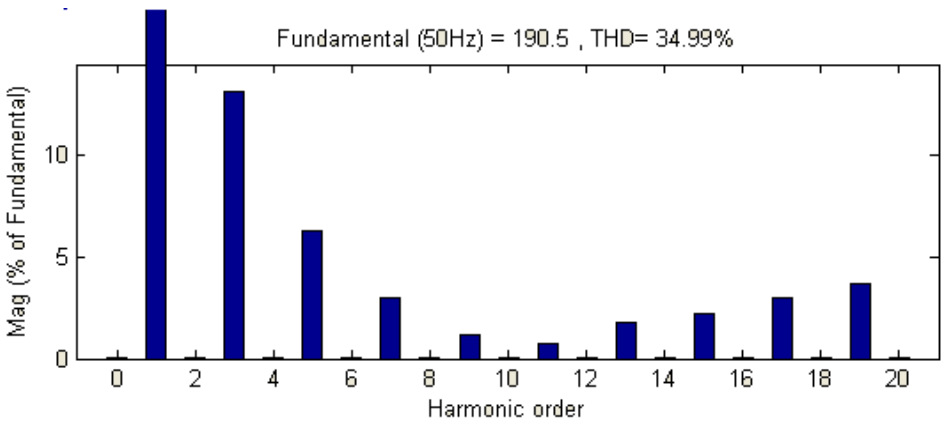

Figure 8. THD Plot for Five Level Output Voltage based on Unequal Amplitude Carriers with PDPWM Strategy (Sine Reference for m_a = 0.8 and m_f =20)

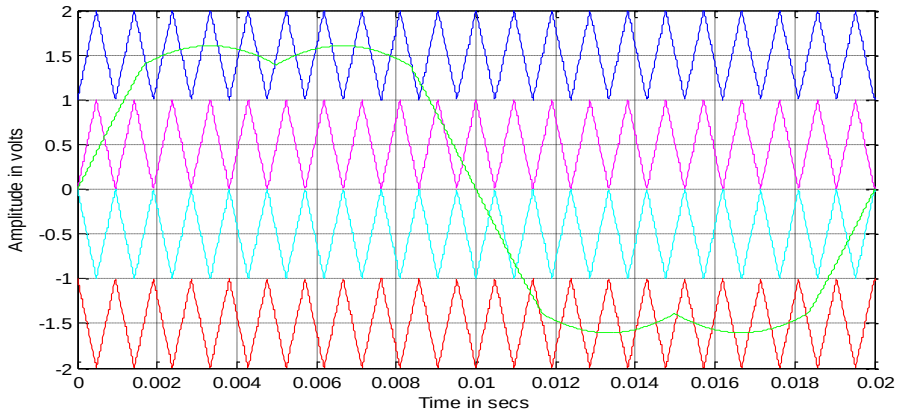

Figure 9. Sample Carrier Arrangement for Equal Amplitude Carriers with PDPWM Strategy (THI Reference for m_a = 0.8 and m_f =20)

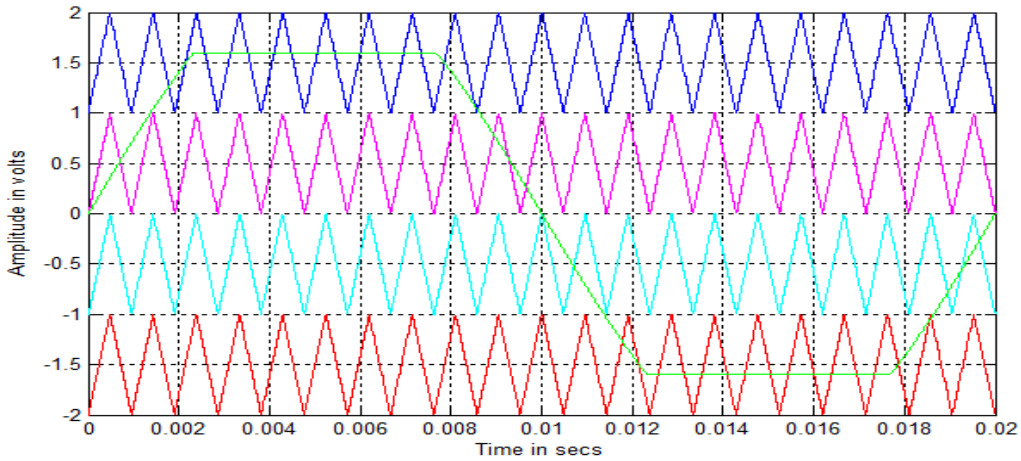

Figure 10. Sample Carrier Arrangement for Equal Amplitude Carriers with PDPWM Strategy (Trapezoidal Reference for m_a = 0.8 and m_f =20)

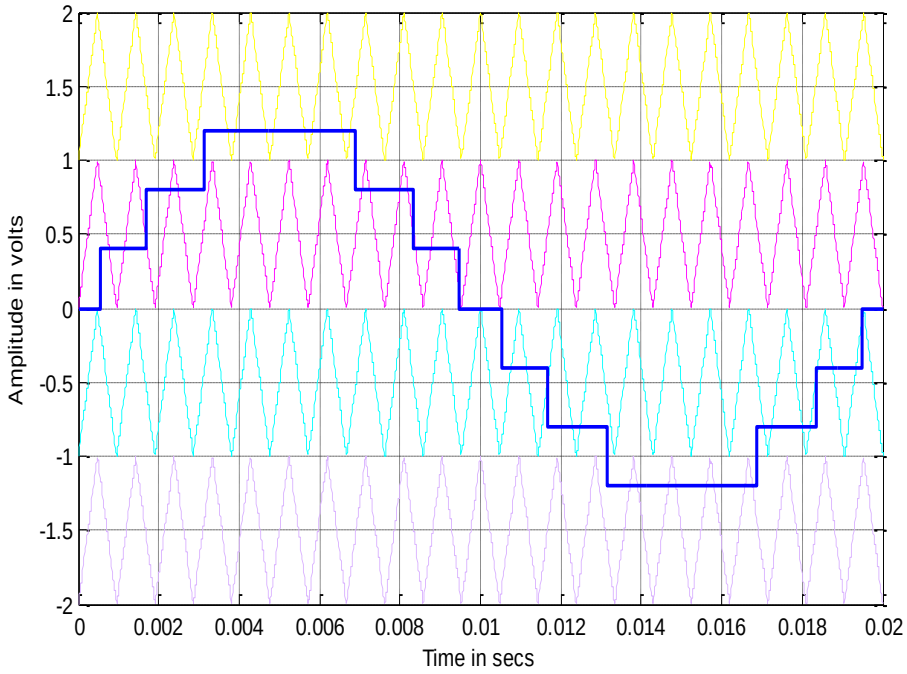

Figure 11. Sample Carrier Arrangement for Equal Amplitude Carriers with PDPWM Strategy (Stepped Wave Reference for m_a = 0.6 and m_f =20)

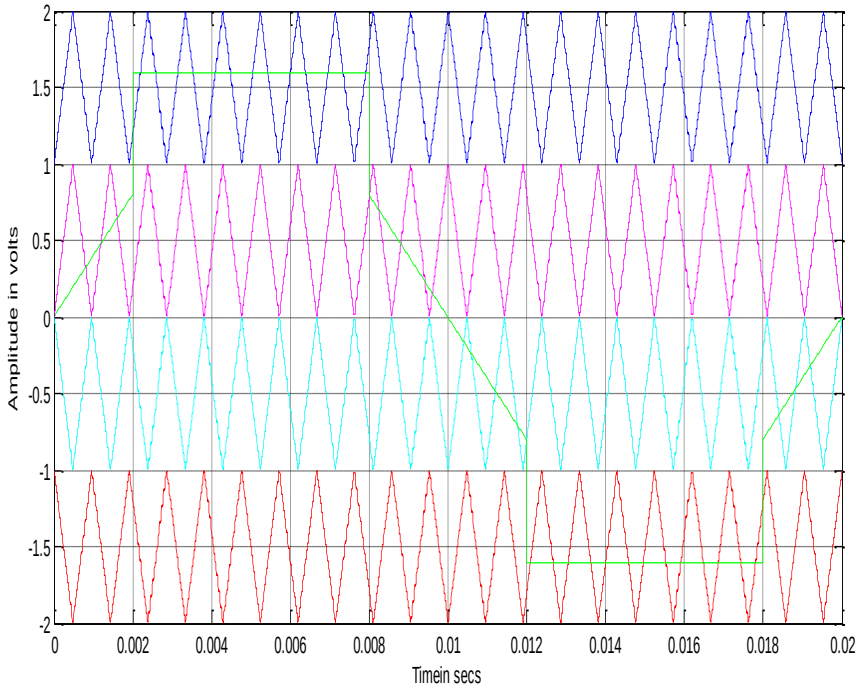

Figure 12. Sample Carrier Arrangement for Equal Amplitude Carriers with PDPWM Strategy (TAR Reference for m_a = 0.8 and m_f =20)

Table 1. THD for Five Level Output Voltage based on Equal Amplitude and un Equal Amplitude Carriers with Various Modulation Indices

Ref.	m_a	% THD for 5-level inverter											
		PDPWM		PODPWM		APODPWM		COPWM		PSPWM		VFPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	CO	UEACO	PS	UEAPS	VF	UEAPD
Sine reference	1	26.79	27.53	26.80	27.70	26.80	27.70	33.63	30.20	26.85	26.65	26.77	28.19
	0.9	32.98	31.46	33.01	31.67	32.02	31.64	38.56	34.43	33.73	29.83	33.39	32.13
	0.8	38.29	34.99	38.29	35.13	38.29	35.13	43.90	37.90	38.22	32.47	38.22	35.44
	0.7	41.81	38.04	41.82	38.08	41.82	38.08	49.39	40.43	42.12	34.97	42.17	38.27
	0.6	44.35	39.39	44.36	39.39	44.36	39.39	58.98	43.43	43.88	37.07	44.58	39.75
	0.5	3-level	40.38	3-level	40.39	3-level	40.39	3-level	46.10	3-level	40.49	3-level	40.43
	0.4		40.32		40.33		40.33		49.03		44.22		40.44
	0.3		42.49		42.50		42.50		59.32		63.56		42.72
THI reference	1	27.45	32.15	27.76	32.27	27.76	31.36	33.28	33.53	29.45	32.27	28.19	31.29
	0.9	35.37	35.61	35.56	35.65	35.56	34.29	37.75	37.79	35.80	35.65	35.80	36.21
	0.8	41.14	39.75	41.20	39.83	41.20	37.49	41.46	41.34	41.27	39.83	41.33	40.42
	0.7	43.84	43.13	43.84	43.24	43.84	39.80	45.66	44.75	44.13	43.24	44.09	43.79
	0.6	42.62	45.02	42.62	45.17	42.62	41.08	52.50	47.16	42.40	45.17	42.84	45.68
	0.5	3-level	45.49	3-level	45.76	3-level	43.30	3-level	48.73	3-level	45.76	3-level	46.26
	0.4		44.47		44.53		42.95		48.34		44.53		44.84
	0.3		38.88		38.89		54.90		51.54		38.89		39.21
Trapezoidal reference	1	22.41	26.53	22.48	26.57	22.48	26.57	29.38	29.28	22.54	27.53	22.67	27.22
	0.9	31.49	32.11	31.50	32.17	31.50	32.17	34.28	33.97	31.46	31.33	31.61	32.75
	0.8	37.37	36.67	37.33	36.76	37.33	36.76	39.55	38.39	37.85	34.59	37.66	37.26
	0.7	41.76	40.03	41.73	40.13	41.73	40.13	44.18	42.15	41.40	37.01	41.83	40.64
	0.6	41.97	42.33	42.03	42.54	42.05	42.54	48.60	44.94	42.69	38.73	42.41	42.98
	0.5	3-level	43.89	3-level	43.98	3-level	43.98	3-level	46.57	3-level	40.09	3-level	44.22
	0.4		42.75		42.75		42.75		47.79		42.53		43.15
	0.3		37.46		37.48		37.48		58.85		64.91		37.66
Stepped wave reference	1	40.15	34.86	37.77	34.90	37.77	34.90	48.10	41.17	37.46	34.44	37.76	34.86
	0.9	43.61	37.87	43.68	37.88	43.68	37.88	52.46	43.47	43.19	36.93	44.03	37.87
	0.8	47.70	39.94	47.65	39.97	47.65	39.97	56.06	45.11	47.23	38.34	48.53	39.94
	0.7	48.80	41.19	48.74	41.20	48.74	41.20	69.01	46.83	48.24	38.11	49.47	41.28
	0.6	60.24	41.08	60.40	41.14	60.40	41.14	82.63	47.95	60.25	3.24	60.71	41.11
	0.5	3-level	38.66	3-level	38.79	3-level	38.79	3-level	53.19	3-level	48.08	3-level	38.78
	0.4		45.39		45.34		45.34		56.79		59.99		46.27
	0.3		60.24		60.40		60.40		83.31		90.09		60.71
TAR reference	1	23.08	20.40	23.06	20.48	23.06	20.48	29.94	23.97	23.12	20.90	23.11	20.90
	0.9	33.66	27.57	33.69	27.58	33.69	27.58	36.12	29.86	33.04	26.13	33.53	27.79
	0.8	41.18	32.79	41.21	32.82	41.19	32.82	41.37	35.11	40.42	30.75	40.83	32.94
	0.7	45.72	36.74	45.80	36.72	45.80	36.72	46.19	39.91	45.37	35.37	45.51	37.06
	0.6	45.77	40.39	45.82	40.45	45.88	40.45	50.21	44.12	46.55	39.77	45.75	40.43
	0.5	3-level	42.94	3-level	43.03	3-level	43.03	3-level	48.02	3-level	43.30	3-level	43.09
	0.4		44.54		44.59		44.63		50.75		46.16		44.27
	0.3		41.55		41.60		41.60		52.58		50.74		41.56

Table 1 and 2 shows the THD and V_{RMS} values for the proposed five level inverter. In Tables it is represented as 3-level for m_a = 0.5 to 0.3. The equal amplitude carrier methods will give five levels only up to m_a = 0.59 but the UEAC method will give five levels up to m_a = 0.26. The Tables compare the total harmonic distortion and Voltage in terms of RMS for various references and carriers.

Table 2. V_{RMS} Fundamental for Five Level Output Voltage based on Equal Amplitude and un Equal Amplitude Carriers with Various Modulation Indices

Ref.	m_a	V_{RMS} for 5-level inverter											
		PDPWM		PODPWM		APODPWM		COPWM		PSPWM		VFPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	CO	UEACO	PS	UEAPS	VF	UEAPD
Sine reference	1	141.5	153.6	141.5	153.5	141.5	153.5	151.5	155.2	141.9	157.2	141.6	153.5
	0.9	127.3	144.2	127.3	144.1	127.3	144.1	141.6	145.8	127.2	148.6	127.1	144
	0.8	113.2	134.7	113.2	134.7	113.2	134.6	130.8	139.6	113.5	140.8	113.3	134.6
	0.7	98.89	124.4	98.89	124.4	98.89	124.4	119.8	127.6	98.18	130.3	98.72	124.6
	0.6	84.92	114.9	84.91	114.9	84.91	114.9	106	117.8	84.87	120.6	84.99	114.8
	0.5	3-level	104.7	3-level	104.7	3-level	104.7	3-level	108	3-level	106.5	3-level	104.8
	0.4		93.53		93.53		93.52		96.64		84.66		93.63
	0.3		80.23		80.23		80.28		80.93		64.1		80.36
THI reference	1	164	169.2	163.9	169.2	163.9	170.4	168.3	169.2	163.4	169.2	163.8	169
	0.9	147.7	157.9	147.7	157.9	147.7	162.5	157.8	159	147.6	157.9	147.7	158.2
	0.8	131.2	146.8	131.1	146.8	131.1	153.9	147.3	148.7	130.9	146.8	131.3	147
	0.7	114.6	135.9	114.6	135.9	114.6	144.5	136.2	138.4	114.6	135.9	114.6	136.1
	0.6	98.06	124.8	98.09	124.7	98.09	135.3	122.8	128.3	97.95	124.7	98.18	124.7
	0.5	3-level	114.1	3-level	114	3-level	122.7	3-level	117.5	3-level	114	3-level	113.9
	0.4		102.5		102.5		98.4		106.6		102.5		102.7
	0.3		90.17		90.16		73.81		92.43		90.16		90.26
Trapezoidal reference	1	165.8	170	165.7	170	165.7	170	169.3	170.6	165.8	171.3	165.8	170.3
	0.9	149.2	158.9	149.2	158.8	149.2	158.8	158.6	160.1	149.2	162.6	149.3	159.1
	0.8	132.3	147.8	132.4	147.8	132.4	147.8	147.3	149.7	132.8	153.7	132.3	148
	0.7	115.8	136.5	115.9	136.5	115.9	136.5	136.2	139.3	115.8	144.6	116	136.6
	0.6	99.39	125.6	99.35	125.5	99.36	125.5	124.2	128.4	99.39	134.9	99.19	125.4
	0.5	3-level	114	3-level	114	3-level	114	3-level	117.6	3-level	124.3	3-level	114
	0.4		102.4		102.4		102.4		106.3		99.58		102.3
	0.3		85.36		85.36		85.36		83.58		65.99		85.46
Stepped wave reference	1	166.7	130.7	153.1	130.7	153.1	130.7	177.3	132.3	153.7	137.7	153	130.7
	0.9	138.5	123	138.4	123	138.4	123	164.7	124.8	138.4	128.2	138.1	122.9
	0.8	128.8	115.6	122.9	115.7	122.9	115.7	153.2	117.8	122.9	119.3	122.2	115.6
	0.7	107.5	107.9	107.5	107.9	107.5	107.9	134.7	11.3	107.9	110.8	106.9	107.8
	0.6	92.33	99.92	92.27	99.9	92.27	99.9	115.5	104.1	92.13	97.11	91.85	99.91
	0.5	3-level	91.81	3-level	91.77	3-level	91.77	3-level	93.45	3-level	81.51	3-level	91.77
	0.4		80.06		80.1		80.1		83.02		64.96		79.58
	0.3		65.29		65.24		65.24		63.98		48.89		64.95
TAR reference	1	157	164.1	157.1	164	157.1	164	159.8	164.4	157.1	161.9	157.2	164
	0.9	141.5	153.7	141.6	153.7	141.6	153.7	149.6	154.9	141.6	153.2	141.6	153.7
	0.8	125.3	143	125.4	143	125.4	143	139.4	144.8	126.1	145	125.6	143
	0.7	109.4	131.8	109.8	131.9	109.5	131.9	128.7	134	110.4	136.4	109.6	131.7
	0.6	93.57	120.1	93.55	120.1	93.59	120.1	117.8	122.8	95.04	128	93.61	120.2
	0.5	3-level	108.2	3-level	108.2	3-level	108.2	3-level	111.1	3-level	119.1	3-level	108.3
	0.4		95.57		95.55		95.6		99.87		95.2		95.94
	0.3		84.18		84.16		84.16		89.45		71.23		84.22

4. Conclusion

The proposed work compares the various multicarrier based Pulse Width Modulation techniques for the chosen single phase CMLI. For all the PWM methods and references the UEAC produces less THD and higher fundamental RMS (Root Mean Square) values except for m_a =1. For m_a =1 the EAC provides less THD (Total Harmonic Distortion) and higher fundamental RMS (Root Mean Square) values for all the PWM methods and references.

If the equal carrier waves are chosen means the THD will be slightly more and V_{rms} will be slightly less. For the equal amplitude carriers if the amplitude modulation index ma is varied from 1 to 0.6 means the five level output will be maintained and the m_a is varied from 0.5 to zero means it will work as a three level inverter. But in the case of unequal amplitude carriers if the amplitude modulation index is varied from one to 0.26 it will work as a five level inverter and the amplitude modulation index is varied from 0.25 to zero it will work as a three level inverter. So the THD will be reduced and V_{rms} will be

increased compared to equal amplitude carriers. The specific applications of the variable amplitude PWM method are in the area of UPS (Uninterruptible Power Supply). The proposed PWM methods with less THD and higher RMS voltage can be implemented in industrial applications such as AC Power conditioners, static VAR compensators, drive systems, *etc.* and in power generation industries.

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