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The Design and Implementation of Hot Spots Detection about Infrared Thermal Imaging Based on SOPC

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Abstract

A kind of hot spots detection alarm device and method is proposed in the paper about infrared thermal imaging, including the hardware design, algorithm, software realization. The hardware mainly includes the infrared thermal imaging camera and intelligent analysis board; the algorithm uses connected component detection method based on run length to extract target rectangle coordinates. This design uses the simple character overlapping circuit and superimposes the alarm target rectangle on the composite video. It has high integration level, simple circuit, and can effectively deal with more than 12 bit pixel data. Because FPGA uses the parallel processing, greatly improving the graphics processing speed, it is suitable for embedded applications in high real-time.

Keywords: *Infrared Thermal Imaging, SOPC, Connected Component Detection, Run Length*

1. Introduction

In recent years, infrared thermal imaging technology [1] has been widely applied in the forest fire warning system, and effectively prevents the occurrence of forest fires. Infrared thermal imaging system receives the infrared radiation energy distribution graph of the measured target using infrared detector, optical lens, and reflects on the thermo sensitive element of the infrared detector. The infrared radiation can be converted into electrical signals by the detector, and then obtain the thermo gram of the object surface

Infrared thermal imaging instrument output the composite video signal such as PAL etc. and LVDS signal interface, and output the original thermal imaging data of 12 bit or 14 bit by LVDS interface. The image processing device after the thermal infrared imaging instrument acquires and processes the image data using infrared image processing technology. Image data belongs to the two-dimensional array, so the calculation of its processing needs high complexity.

DSP digital image processing chip can complete some complex graphics computing, but the interface is not flexible enough, and the image data acquisition requires LVDS converting circuit to realize difference conversion signal or jointly complete with FPGA, this increases circuit complexity. Although superposition of hot outer rectangle on composite video signal can use the OSD function of the DSP itself, but we first need to decode the composite video of infrared thermal imager, this adds complexity circuit. Processing more than 12 bit pixel data is a challenge for DSP. At the same time, DSP uses serial processing on image processing, reduces the image processing speed and can not satisfy the requirement of embedded application about high real-time.

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In order to achieve the original image data acquisition and processing and superimpose alarm target rectangle on the composite video signal of thermal infrared imager, and overcome the shortcomings of DSP processor, the design proposes a hotspot detection alarm device and method based FPGA on infrared thermal imaging. The design has the advantages of high integration degree, simple circuit, fast processing speed.

2. Hardware Structure of System

2.1. Structure and Composition of the System

The structure of system is shown in Figure 1. It concludes three parts, and each part is introduced as follows.

(1) Infrared thermal imaging cameras, generating the original image and outputting composite video signal and LVDS signal.

(2) Intelligent analysis card, receiving a composite video signal and LVDS signal from the infrared thermal imaging camera, completing analyzing and processing the LVDS signal, and the composite video signal is transmitted to the display and control terminal;

when the Intelligent analysis card analysis the alarm target detected LVDS signal , it superimposes warning target rectangle on a composite video signal and transmits composite video signal to the display and control terminal, at the same time, the number of target and the coordinate value of alarm target rectangle transmit to the display and control terminal, and display the alarm target position in the display and control terminal .

(3) Display and control terminal, it displays the infrared thermal imaging video and sends the setting information to the intelligent analysis board.

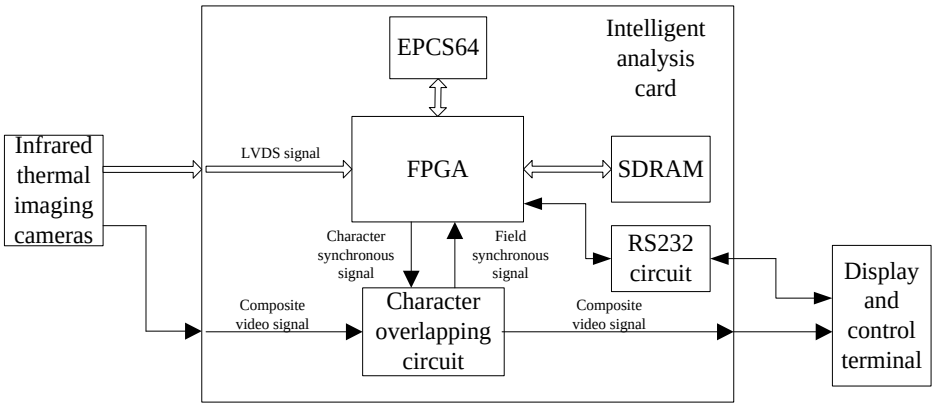

Figure 1. The Structure of the System

2.2. Implementation of Intelligent Analysis Card

The core of system is the intelligent analysis card. It concludes five parts, and each part is introduced as follows.

(1) FPGA [2], it receives the LVDS signal from the infrared cameras, and finishes the analysis and processing of LVDS signal. When the LVDS signal detects the alarm target, FPGA sends alarm target number and alarm target rectangle coordinate value to the display and control terminal through the serial communication circuit. FPGA also receives the field synchronous signal from the character overlapping circuit, and outputs the character control signal to the character overlapping circuit;

FPGA is configured as a SOPC system based on NIOSII embedded soft core. The system includes image acquisition, OSD unit, NIOSII [3] microprocessor unit, SDRAM control unit, Avalone bus [4] unit, asynchronous serial port UART unit, serial storage unit EPCS, timer Timer unit. The preprocessing unit of image acquisition and the OSD unit is a custom peripherals, this can make full use of the parallel processing ability of FPGA.

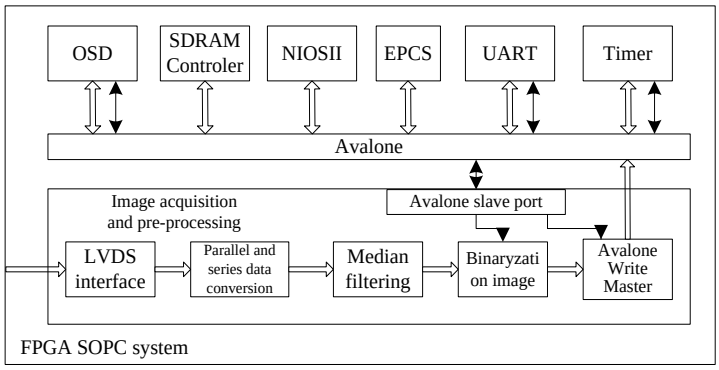

Figure 2. Internal Functional Units of the FPGA

(2) Character overlapping circuit, it receives the composite video signal from the infrared thermal imaging camera, and generates the field synchronous signal, then the signal is sent to the FPGA. When the LVDS signal detects the alarm target, character overlapping circuit outputs the composite video signal of the warning target rectangle to the display and control terminal.

Character overlapping circuit schematic diagram is shown in Figure 3, including video amplifying circuit and line field synchronous signal separation circuit and analog signal selection circuit.

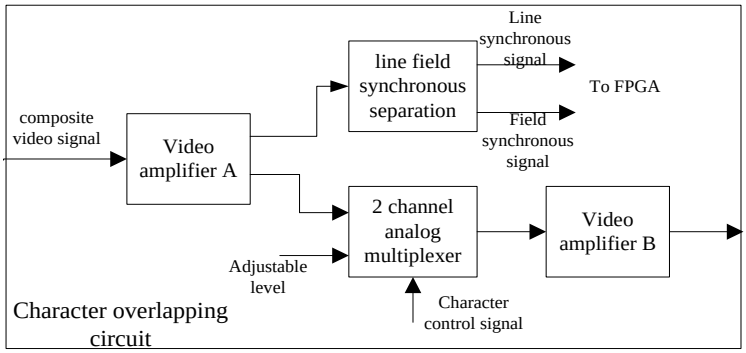

Figure 3. Character Overlapping Circuit Schematic Diagram

3. Extraction of Fire Point Coordinates Feature

3.1. Target Separation and Binaryzation Image

Before the target signature analysis we need separate the target and background, because the heat radiation value of the fire point is much higher than the background value, so we can simply compare the current pixel value and the radiation data mean. When the D-value is

greater than the threshold value, we will change the current pixel value to 255, in contrast to 0.

3.2. Extraction of Target Feature

Based on run-length, an algorithm for connected component detection [5-8] is proposed to extract the target rectangle coordinates. The algorithm runs fast and can complete the statistic of target number and the extraction of target characteristics through scanning binaryzation image data for one only time can. Multiple target point of a continuous line is as a run length, according to the connected relationship between the current line and top line, we mark the current run-length and feature modification according to specific rules [6]. Different feature modification ways is caused by different marking rules. The rule "STEP7" of the reference [5] treats different types of run-length of top line. The method is to record the equivalence relation in equivalent array and update the first feature of run-length. Did not compare run-length label size. The algorithm of the comparative label size reference is also not adopt in reference [6], resulting in the increase of the multi-tree depth, accordingly increasing the feature modification depth.

The basic data structure of connected domain detection method based on run length:

```
//structure of run length
typedef struct _line{
    long index;
    unsigned short colthOfStart,colthOfEnd;
}line;
//connected domain characteristics
typedef struct COMPONENT{
    unsigned short left,top,right,bottom;// external rectangle
    long area;//area
}_Com;
// modular construction
typedef struct _node{
    long flag;
    _Com ComAttr;
}node;
```

3.3. Algorithm Implementation

We define two run-length array, the array size is half of the rows of pixels, for example line Array1[WIDTH/2],Array2[WIDTH/2]. Then we define two run-length pointers, one is for the access of current line arrays, another is for the access of top line arrays, for example line *curLine=Array1; line *preLine=Array2. The initialization of global run-length marks 1, that is label=1. The processing steps are as follows when detecting the run-length end:

1) If the run-length is not connected with the top line run-length

Update the run-length identification index as a global identification, then the global identification plus 1; The run-length data initialize its logo and point the unit features, the run-length label initialize the unit identification. That is:

nodeArray[*(curLine+cur_index).index].flag=*(curLine+cur_index).index; label++;

2) If the run-length is connected with the top line, there are three cases:

(1) If the current run-length does not mark, it is updated to the pointing unit label of top connected run-length. That is:

(curArray+cur_index).index=nodeArray[((preArray+pre_index).index].flag;

At the same time the current run-length mark is updated and point to the unit features.

(2)if the current run-length mark is greater than the top line, it is updated and point to the unit mark, the connected run-length mark of top line is also updated and point to the unit features. That is:

nodeArray[*(curArray+cur_index).index].flag = *(preArray+pre_index).index;

nodeArray[*(preArray+pre_index).index].ComAttr need nodeArray[*(curArray+cur_index) .index].ComAttr attribute update。

(3)if the current run-length mark is less than the top line, the connected run-length mark of top line is updated and point to the unit mark, the current run-length mark is also updated and point to the unit features. That is:

nodeArray[*(preArray+pre_index).index].flag = *(curArray+cur_index).index;

nodeArray[*(curArray+curArray_index).index].ComAttr need nodeArray[*(preArray+preArray_index).index].ComAttr attribute update。

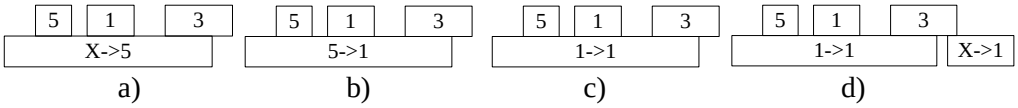

Figure 4. Run Length Label

Figure 4 a) current run length label updates 5, modify nodeArray [5] attribute；b) first update nodeArray [5].flag=1；and according to nodeArray[5] update nodeArray [1] attribute. run length label updates 1; c) according to nodeArray [3].flag=1, according to nodeArray [3] update nodeArray[1] attribute; d) nodeArray [3].flag update current run length label, update nodeArray [1] attribute.

3.4. Proof of Algorithm

The algorithm is tested under the VC environment, the two value image data about 324 x 256 is input, and rectangular image data is output. The test result is shown in Figure 5:

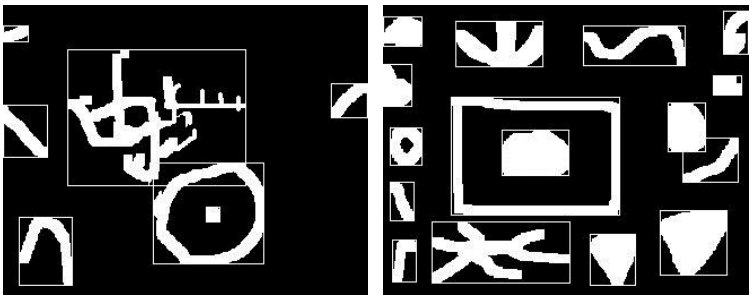

Figure 5. Test Result Chart

4. Software Realization

4.1. Realization of Custom Module

Image acquisition and preprocessing unit is a custom peripheral, it includes LVDS interface module, data serial to parallel conversion module, median filtering module, binaryzation image module, Avalone write master port module and Avalone slave port

module. The implementation of the binaryzation image is: the present pixel value and previous frame pixel average value calculate the difference, if the difference is greater than the set threshold value, then the current pixel value outputs 255, otherwise 0. The main port directly writes the binaryzation image data to the external SDRAM, after completion NIOSII microprocessor is received in the interrupt mode. The interrupt signal and preprocessing unit registers are defined in the Avalone slave module, including binaryzation threshold register, writing address register, data length register and peripheral control register.

4.2. NIOSII Program Flow

Flow chart of program design is shown in Figure 6:

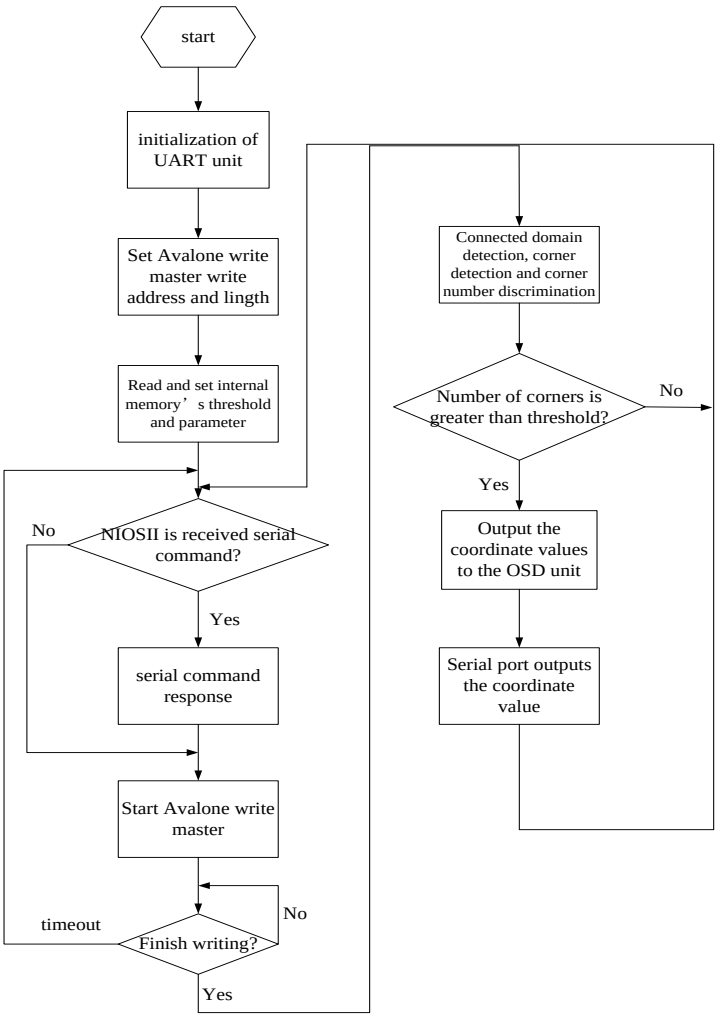

Figure 6. Flow Chart of Program Design

5. Conclusions

A kind of hot spots detection alarm device and method is realized in the paper about infrared thermal imaging, using FPGA system architecture for acquisition and processing of infrared image, relative to the DSP system architecture, This design uses the simple character

overlapping circuit and superimposes the alarm target rectangle on the composite video. It has high integration level, simple circuit, and can effectively deal with more than 12 bit pixel data. Because FPGA uses the parallel processing, greatly improving the graphics processing speed, it is suitable for embedded applications in high real-time.

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