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A Random Sequence Generation Method for Random Demodulation Based Compressive Sampling System

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Abstract

Random demodulation based compressive sampling technique is a novel approach that it can break through the Shannon sampling theorem for the sparse signal capturing. A major challenge in the random demodulation based sampling system is the random sequence generation. In this paper, we introduce an approach to generate the high-speed random sequence that meets the incoherence of compressive sampling. The proposed technique employs a field programmable gate array (FPGA). First, the random sequence is parallel stored in the memory of FPGA, and it is read out byte by byte using a low speed clock. Second, the low-speed byte sequence is converted to a high-speed bit sequence by a circuitry. This proposed approach can program the random sequence dynamically without making any change to the circuitry system. Experimental results indicate that, the random sequence generated by the proposed approach is feasible to sensing the signal, and the constructed system can compressively sample and reconstruct the sparse signal.

Keywords: *Random sequence generator, Incoherence, Parallel-to-serial, Compressive sampling*

1. Introduction

Compressive sampling (CS) [1-2] is a new signal processing theory that can break though the Shannon sampling theorem for the sparse signal capturing. The random demodulation technique makes applying CS to analog signal sampling possible. Based on random demodulation, Kirolos *et al*. [3-4] developed an analog-to- information converter (AIC), which can be used to sample the spectrally sparse analog signal at a sampling rate that is much lower than Nyquist rate. An analog signal is spectrally sparse if it consists of very few harmonics. Eldar *et al*. [5] developed a modulated wideband converter (MWC), which can work not only for spectrally sparse signal, but also for band sparse signal. For this family of analog signals, the CS theory ensures that very few random time samples will be sufficient to reconstruct the analog signal with great precision.

Both AIC and MWC require analog pre-processing. In particular, a pseudorandom sequence running at the Nyquist rate is needed to modulate the analog signal. During this process, the demodulator smears the signal tone across the entire spectrum of the pseudorandom sequence. Then the demodulated signal is lowpass filtered and sampled. Since each tone has a signature within the passband, the original signal can be reconstructed from the low rate samples. In the signal reconstruction, a measurement matrix should be constructed in the context of system. The measurement matrix is constructed by the pseudorandom sequence, and it must satisfy the restricted isometry property (RIP).

However, to realize high speed signal sampling, a high speed random sequence must be generated. The shift register [6] is a usual way to generate the random sequence. Generally, a shift register can generate a bits sequence with the length of 10 bits. In order to reconstruct signal with a high probability, a random sequence with long length would be required. If the random sequence is generated by the shift register, a large number of shift registers are needed. It would be a challenging task to place so many shift registers in the limited printed circuit board (PCB). The long length high speed ideal random sequence is hard to be implemented. In order to address this issue, Puy *et al.*, [7] proposed that the Hadamard vector is used to sensing signal. Zhao *et al.*, [8] suggested a measurement matrix for random equivalent sampling (RES) based on Shannon interpolation equation. These techniques can be easily implemented. However, it also introduces coherence in the measurement matrix, and it would degrade the reconstruction accuracy.

In this paper, we propose an implementable approach to generate the random sequence. Deferent from the conventional technique, the random sequence is generated using a field programmable gate array (FPGA) and a parallel-to-serial circuitry. The random sequence is stored in the memory of FPGA with byte format in advance. During sampling, it is read out by a low speed clock. Then, the byte sequence is converted to bit sequence using a parallel-to-serial circuitry. With this technique, the sequence could be designed with long length, and it can also be configured dynamically. The length of the random sequence is only limited by the memory capacity. Based on the proposed AIC architecture, a circuitry system is designed. The designed system is with 2 GHz equivalent sampling rate while it is implemented with an analog-to-digital convertor (ADC) with 20 MHz sampling rate.

The presentation of this article goes as follows. A brief background on CS is reviewed in Section 2. The property of the random sequence is evaluated in Section 3. A novel random sequence generation approach is proposed and implemented in Section 4. Experimental results are reported in Section 5. Further discussions are summarized in Section 6.

2. Review of CS Theory

CS holds the promise to process the sparse signal at its information rate [9]. Sparsity expresses the idea that a discrete time signal depends on a number of degrees of freedom that is comparably smaller than its length, or that the information rate of a continuous time signal may be much smaller than its bandwidth presented in the signal. More precisely, CS exploits the fact that many signals are sparse in the sense that they have concise representations when expressed in an appropriate basis, such as Fourier basis, wavelet basis, etc. According to the measurements done by FCC in the US [10], in many cases the current frequency usage exhibits sparsity because only a part of the allocated channels is active at a given time. For this family of signals, the CS theory ensures that very few random time samples will be sufficient to reconstruct signal with great precision.

In CS, the signal to be reconstructed is denoted by an N × 1 discrete time signal x. x is called K-sparse (K << N) in some sparsity basis matrix Ψ, which means that there exists a vector α with ||α||0 = K such that x = Ψα. Here the l0 norm ||·||0 counts the number of nonzero entries in vector α. Just the opposite, incoherence means that the measurement matrix Φ has dense representation in the basis Ψ, and Φ is independent of Ψ.

Most of signals have sparsity in the process of actual sampling. We can reconstruct the original signal by compressive sampling. For K-sparse signal x, we can find its $M = O(K\cdot\log(N/K))$ linear measurements, and its random projections $\boldsymbol{y} = \boldsymbol{\Phi x} = \boldsymbol{\Phi\Psi\alpha}$ (where $\Phi \in M \times N$ is the measurement matrix, $x = \Psi\alpha$， as the measured value $y \in M \times 1, M << N$, and y is the measurement vector with size of $M \times 1$), and the original signal $\boldsymbol{x}$ can be precisely recovered by solving l_0 norm optimization problem:

$$\min \|\boldsymbol{\alpha}\|_0 \quad s.t. \quad \boldsymbol{y} = \boldsymbol{\Phi}\ \boldsymbol{x} = \boldsymbol{\Phi\Psi}\boldsymbol{\alpha}\ . \tag{1}$$

Minimizing the l_0 norm of $\boldsymbol{\alpha}$ amounts to minimize the number of non-zero elements of the solution $\alpha^{\#}$ and therefore force the solution to be a sparse vector.

A sufficient condition for a sparse solution of α exists is that the matrix $\Theta = \Phi\Psi$ must satisfy RIP. Equivalently, the RIP condition can also be evaluated in terms of incoherence between the measurement matrix $\mathbf{\Phi}$ and the representation basis $\mathbf{\Psi}$ [11]. The coherence between $\mathbf{\Phi}$ and $\mathbf{\Psi}$ is defined as

$$\mu(\Phi, \Psi) = \sqrt{N} \cdot \max_{1 \le i, k \le N} \left| \langle \varphi_i, \psi_k \rangle \right| . \tag{2}$$

To ensure a sparse solution $\alpha^{\#}$ exists, $\mu(\mathbf{\Phi}, \mathbf{\Psi})$ should be as small as possible.

3. Properties of the Random Sequence

Based on the previous section analysis, the measurement matrix constructed by the random sequence should have small coherence with respect to the representation basis Ψ. In this section, we investigate the “hard implementable” random sequence and the “easy implementable” Hadamard vector.

Considering a spectral sparse signal, the sparse representation basis is constructed by Fourier basis vector. In order to reconstruct the signal in the digital domain, the Fourier basis is approximated by the discrete Fourier transform (DFT) vector. The longer random sequence means that more noise is added to each measurement. By itself, this does not affect the SNR (signal-to-noise ratio), since more signal is included in each measurement, but it also means that the noise included is more correlated [12], so it is more important to choose appropriate sequence length for this correlation according to recovery algorithms. Gaussian matrices, Fourier matrices and random Toeplitz matrix, random Bernoulli matrix, *etc.*, which has been shown to satisfy the RIP condition, in which the random Bernoulli matrix can be implemented in hardware circuit ,and the random Bernoulli matrix has got widely used. In this paper, we use the measurement matrices constructed by Shannon interpolation equation based on RES. According to Shannon interpolation formula, the m-th value of random samples and the original signal x satisfy the following relationship:

$$y(\Delta t_m) = \sum_{n=1}^{N} x(nT_e) \sin c \left(\frac{\Delta t_m}{T_e} - n \right) \tag{3}$$

where $1 \le m \le M$， $1 \le n \le N$, M is the number of random samples (M << N), Δt_m is the time interval of the m-th samples, the Eq.(3) establishes relationship between a known non-uniform random samples value and unknown uniform equivalence samples value, it can be further expressed as a matrix-vector expression:

$$\begin{bmatrix} y(\Delta t_1) \\ y(\Delta t_2) \\ \vdots \\ y(\Delta t_M) \end{bmatrix} = \begin{bmatrix} \phi_{1,1} & \phi_{1,2} & \cdots & \phi_{1,N} \\ \phi_{2,1} & \phi_{2,2} & \cdots & \phi_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ \phi_{M,1} & \phi_{M,2} & \cdots & \phi_{M,N} \end{bmatrix} \begin{bmatrix} x(T_e) \\ x(2T_e) \\ \vdots \\ x(N \cdot T_e) \end{bmatrix} \Leftrightarrow \quad \mathbf{y} = \Phi\,\mathbf{x} \tag{4}$$

where Φ is measurement matrix ,and the (m, n)’th element with the following expression:

$$\Phi(m, n) = \phi_{m,n} = \sin c \left(\frac{\Delta t_m}{T_e} - n \right) \tag{5}$$

Fig. 1 describes the coherence between the measurement matrices and the representation basis (M = 64, N = 128). The measurement matrices are constructed by the Hadamard vector, Shannon interpolation equation based on RES, and random sequence, respectively. We can clearly note that, the measurement matrix based on the random sequence introduces much lower coherence, and it is also stable.

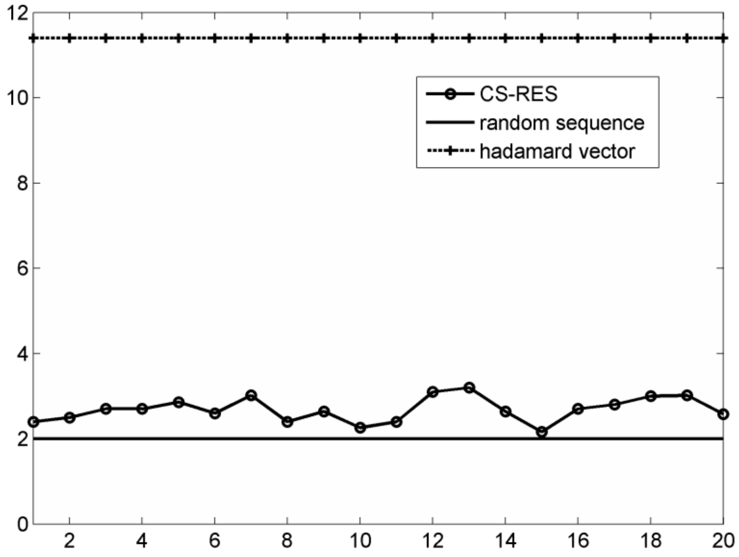

Figure 1. Coherrence Caparison

4. Parallel-to-Serial Random Sequence Generation

Random sequence results in a lower coherence compared to the Hadamard vector, and it has been wildly applied in CS implementation. However, it is hard to generate a random sequence with high speed and long length. In this paper, we suggest a parallel-to-serial based random sequence generation approach. A block diagram of compressive sampling system with the proposed random sequence generation is shown in Figure 2.

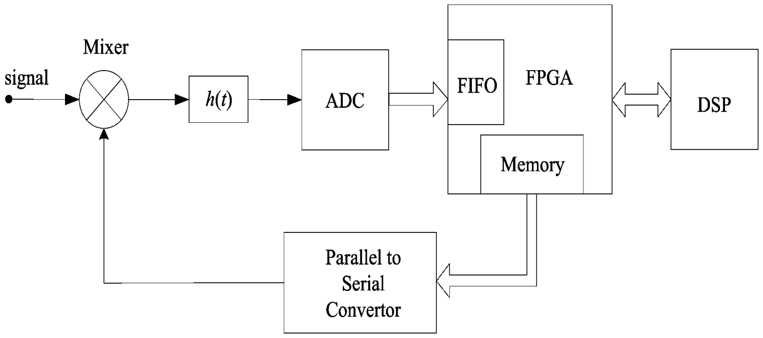

Figure 2. Block Diagram of Compressive Sampling System with the Random Sequence Generated by the Parallel to Serial Technique

The compressive sampling system consists of 6 parts: mixer, lowpass filter h(t), ADC, FPGA, digital signal processor (DSP) and parallel to serial convertor. Signal mixed with the random sequence output from the parallel to serial convertor that is controlled by FPGA. The mixed signal lowpass filtered and sampled using a low speed ADC. The samples are fed into the first in first out (FIFO) memory, and read out and reconstructed by DSP. In this paper, our focuses are FPGA and parallel to serial convertor circuitry.

In this work, FPGA is used to receive samples and generate random sequence. The FIFO control is simple, and we only discuss the random sequence part. Random sequence is generated using Matlab software, and it is a bit stream with values of “+1” and “0”. In order to reduce the rate of the sequence output, the bit stream is transferred to byte format and stored in the random access memory (RAM) of FPGA. Figure 3 shows the scheme of the random sequence storage. The process of format transform is carried out in DSP, and the random bytes are written into RAM by DSP.

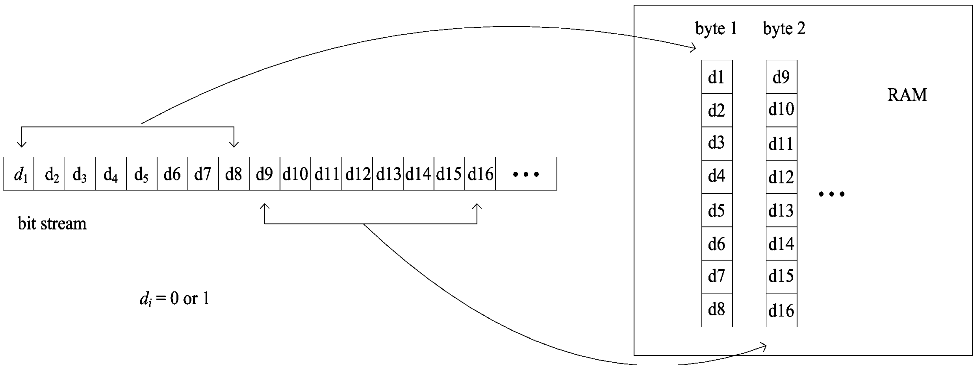

Figure 3. Scheme of the Random Sequence Storage

After stored in RAM, the random bytes are read out under the control of the clock that is output from the parallel to serial convertor. Figure 4 depicts the reading process of random bytes. The random bytes are written into RAM though “Input bus”. The “Address generator” is used to generate the output address, and it is controlled by the enable signal “cnt_en” and the clock “clock_ref”. The address generator starts to count with increment of “1” at the moment of rising edge of the “clock_ref” while the cnt_en is high level. In order to hold the promise that, the output address is valid at the moment of rising edge of read clock “rdclock”, the “clock_ref” is inverted to get the “rdclock”.

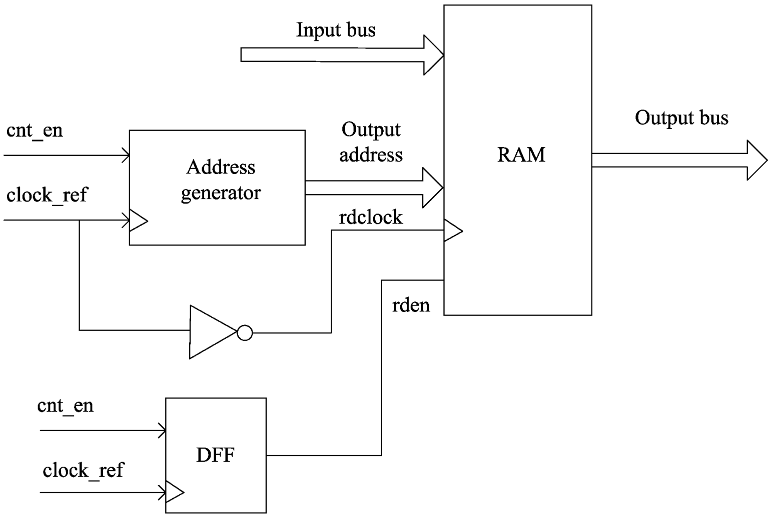

Figure 4. Scheme of Output Process of Random Bytes

The reading process should be triggered after the valid address obtained. RAM outputs a byte under control of the “rdclock” and the enable signal “rden”. If we use the “cnt_en” to enable reading process of RAM, due to the asynchronism between the “rdclock” and “cnt_en”, the falling edge of “clock_ref” may occur after “cnt_en” changing to high level. At this moment, the address is invalid. However, a reading process would be triggered duo to the rising edge of “rdclock”. In this work, a D-flip-flop (DFF) is used to synchronize the enable signal and “rdclock”. With the help of DFF, the first edge change of “rdclock” would be always the falling edge after “rden” changing to high level.

After the random byte output from FPGA, it is fed into the parallel to serial convertor circuit. Figure 5 show parallel to serial convertor circuit. In this work, it is implemented by

MC100EP446. The byte stream is converted to bit stream under control of the high speed clock "8Xclock". A clock with rate of 1/8 of 8Xclock is generated and output, and it is fed into FPGA to get "clock_ref". Then, the rate of clock would be significantly dropped.

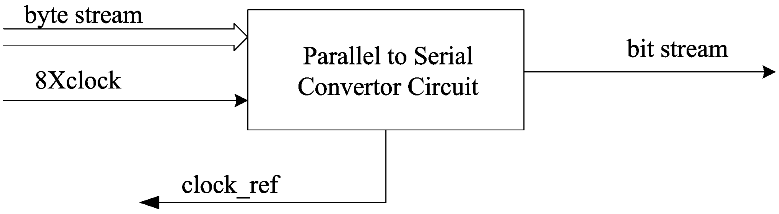

Figure 5. Scheme of Parallel to Serial Convertor

The random bit stream is with the values of "+1" or "0". If the signal is mixed with "0", the energy would not be connected. In order to address this challenge, the bit stream is coupled by a capacitor.

5. Experimental Results

Based on the proposed architecture, an AIC circuitry system is built. Considering the further work, four sampling channels are incorporated in the system. The random sequence is generated by a parallel to serial device MC100EP466 whose frequency range is 0 ~ 3.2 GHz. By employing MC100EP466, a byte format random sequence with 250 MHz is converted to a bit format random sequence with 2 GHz (8bit × 250MHz). The mixing part is realized by MC13143 whose frequency range is 0 ~ 2.4 GHz. The demodulated signal is captured using an ADC with sampling rate of 20 MHz, which is implemented by AD9288 from ADI Company. Fig. 6 shows the implemented AIC circuitry system. The random samples are captured by the designed system and transferred to a computer, where the original signal is reconstructed by recovery algorithm.

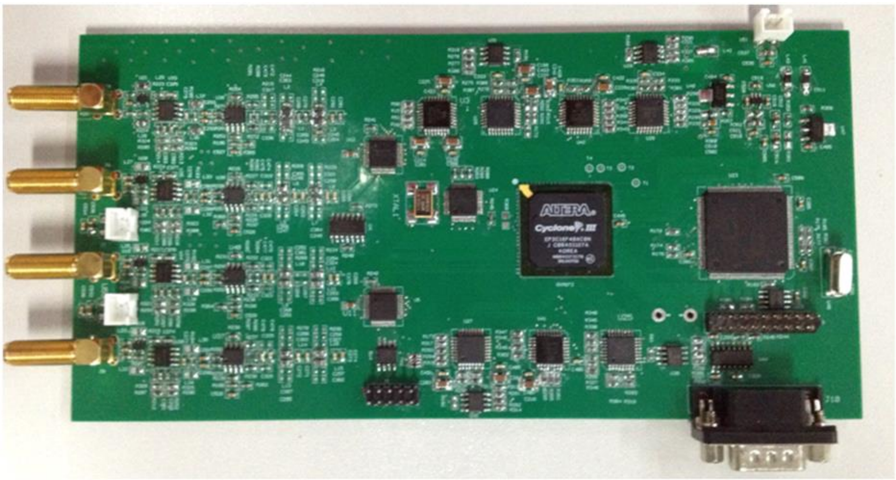

Figure 6. Scheme of the Implemented AIC System

In this section, experiments are carried out to evaluate the proposed system. Since the main contribution of this work is to generate a high speed random sequence, in the first experiment, we evaluate the feasibility of this part.

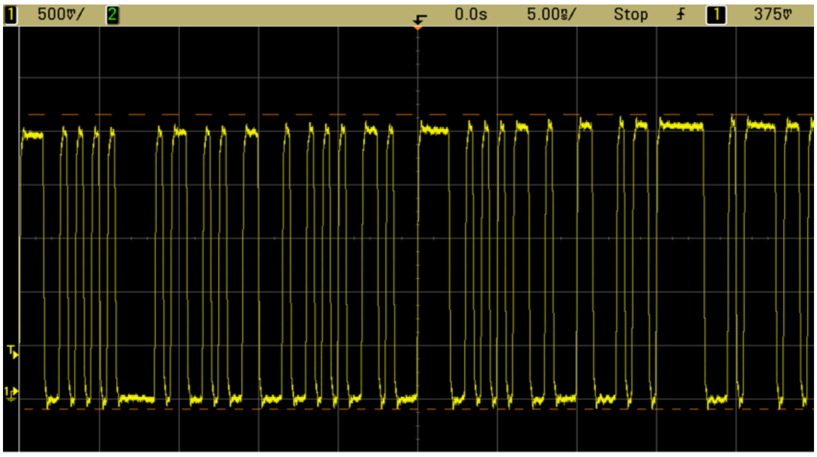

Figure 7. Generated Random Sequence

We generate a random sequence with byte format {A8D72A82CA6254D1E55918 B7E2F69B7C3} in FPGA. It is read out with a rate of 250 MHz, and fed into parallel to serial convertor. After converting into a bit random sequence, it is measured by a digital storage oscilloscope and depicted in Figure 6. Obviously, the feasibility of the proposed parallel to serial technique is demonstrated.

AIC holds the promise to perfect reconstruct the original signal from the collected sub-Nyquist samples for sparse signal. In this experiment, we used the implemented system to sample a sine-wave signal with frequency of 200 MHz. The signal is fed into one channel of system, and sampled by an ADC clocked at 20 MHz, and it is much lower than the signal's Nyquist frequency. Figure 8 shows the reconstructed signal and the measured signal (measured by a MSO6102A from Agilent). Signal is reconstructed from the sub-Nyquist samples by root-MUSIC algorithm [13]. From Figure 8 we can clearly note that, the implemented system is feasible, and signal is almost perfectly reconstructed.

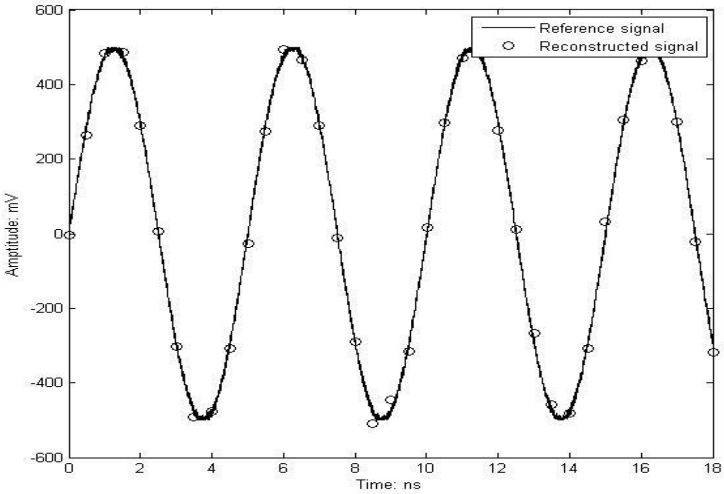

Figure 8. Signal Reconstruction Comparison

6. Conclusion

AIC is a most successful application of CS theory in analog signal sampling. In this work, we implemented AIC with off-the-shelf devices. Parallel to serial technique is adopted to generate high-speed random sequence. The proposed system can be dynamically configured with variational length and type of random sequence. We tested the implemented system with satisfactory results.

In the next steps, we will do experiments on two ways. One is Multiple channel sampling. From a theoretical point-of-view, more channels are better. The matrix representation **Φ** of such a system closely approximates a signed Bernoulli matrix, which is known to be incoherent with any basis. In contrast, a single channel operating at a fast rate becomes closer to a simple underclocked regular ADC, which is not a good measurement system. Another one is the choice of the sequence, which we refer to synonymously as the PRBS (pseudo-random bit sequence). The generated sequence is periodic, but we will consider both periodic and infinite sequences for the sake of analysis.

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