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Design of Dual-channel Sine Wave Generator with Tunable Phase Difference

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Abstract

Signal source is an important part of modern electronic system and has a wide range of applications in the fields of communication, measuring & control, navigation and medical care. This project developed a new dual-channel sine wave generator with Tunable Phase Difference on the basis of the direct digital frequency synthesis (DDS) technology. Design was accomplished using STC89C52 MCU and FPGA as the control center, integrating basic operation circuit and employing low-pass filter and the necessary software algorithm. The experimental results showed that the system can produce dual sine waves with tunable phase difference in 0~359° range. The system is stable in work and it is easy to adjust parameters.

Keywords: *Filter, FPGA, DDS technology, Tunable Phase Difference, Sine wave generator*

1. Introduction

Sine wave generator has an irreplaceable position as a common signal source in design and production fields of the modern electronic product. Its main function is to supply all sorts of equipments and measuring devices with sine waves of different amplitudes, frequencies and phase differences. This project developed a new dual-channel sine wave generator with higher precision and cost-performance ratio on the basis of comparing a variety of sine wave generators' principals. The phase difference ranges from 0° to 359°. Output frequency is adjustable between 1 Hz to 1 KHz with a step of 1Hz and frequency accuracy greater than 0.1%. In practical applications, dual-channel sine wave generator with tunable phase had become a very important demand. This project achieved all the functions of Digital Frequency Synthesis (DDS) using FPGA devices manufactured by ALTERA[1-5]. In the design, no DAC device was used in the analog circuit unit and control logic unit did not have any memory. The signal generator can be used in each channel separately or in double channels producing sine waves with a phase difference. The generator has high frequency resolution, tunable phase, output frequency stability and low cost.

2. Generation

System structure for dual-channel sine wave generator with tunable phase is shown in Figure 1. The signal generator system was divided into three parts, which were microprocessor unit, control logic unit and analog circuit unit.

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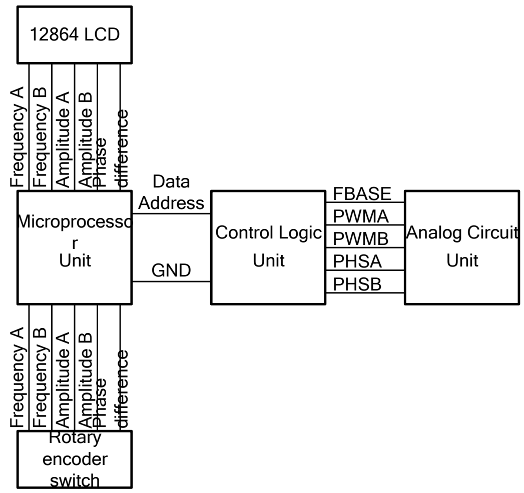

Figure 1. The System Structure Diagram of Sine Wave Generator

A microprocessor unit has three main functions. The first one is the setting function. Parameters such as amplitude, frequency and phase difference can be set by the rotary encoder switch. The second one is the display function. Sine wave generator can display all kinds of parameters by the LCD 12864. The third function is to send parameter control keys (*e.g.*, frequency, amplitude and phase difference) in series to the control logic unit. The main function of control logic unit is to produce several stable pulse signals and then send to the analog circuit unit. Analog circuit unit has two functions which are implementing a series of signal transformations and outputting a one-way sine wave or two-way sine waves with tunable phase difference.

3. Implementation of Amplitude Modulation and Frequency Modulation

The diagram of amplitude modulation and frequency modulation of sine wave generator is shown in Figure 2. Based on DDS technology and using the square wave from control logic unit, the system is able to complete these two functions though 74HC4053 and interrelated circuit in analog circuit unit [6].

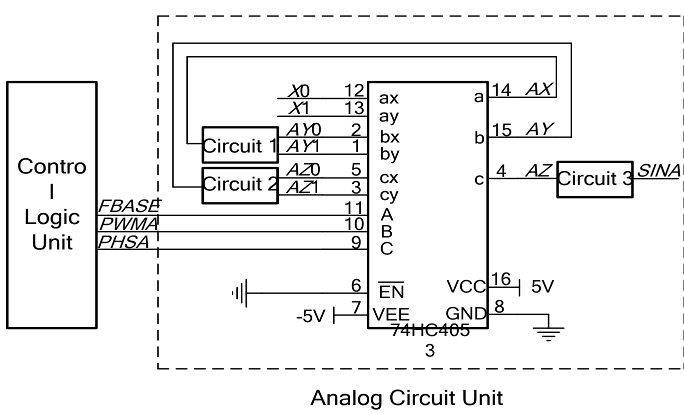

Figure 2. The Diagram of Amplitude Modulation and Frequency Modulation

3.1. The Design of Amplitude Modulation Function

The following is as an example for requiring a sine wave with amplitude of *A* to show how the system is to realize the amplitude modulation function.

As shown in Figure 2, *X*0 and *X*1, the first group of input signals for 74HC4053 are reference DC signals, their values are 5v and -5v[8]. Corresponding selection signal is a square wave signal *PWMA* with a duty ration of *Q* and frequency of 10 KHz provided by the control logic unit. When *PWMA* is in high level, output of *AX* is signal *X*1, which is, 5v high level signal (expressed as V_{ref}); And when *PWMA* is in low level, output of *AX* is signal *X*0, which is, -5v low level signal (expressed as V_{neg}), the duty ration of signal *AX* is constant as *Q*.

After signal *AX* goes through circuit 1, two DC signals *AY*0 and *AY*1 whose amplitudes are *A* and –*A* can be obtained. Circuit 1 is shown in Figure 3. The figure shows that after signal *AX* goes through three order low-pass filter circuit, two signals *AY*0 and *AY*1 can be obtained. *AY*1 is a DC signal with amplitude of *A*, and *AY*0 is a DC signal with amplitude of -*A*. The amplitude *A* can be calculated as follows:

$$A = V_{ref} Q + V_{neg} (1 - Q) \quad (1)$$

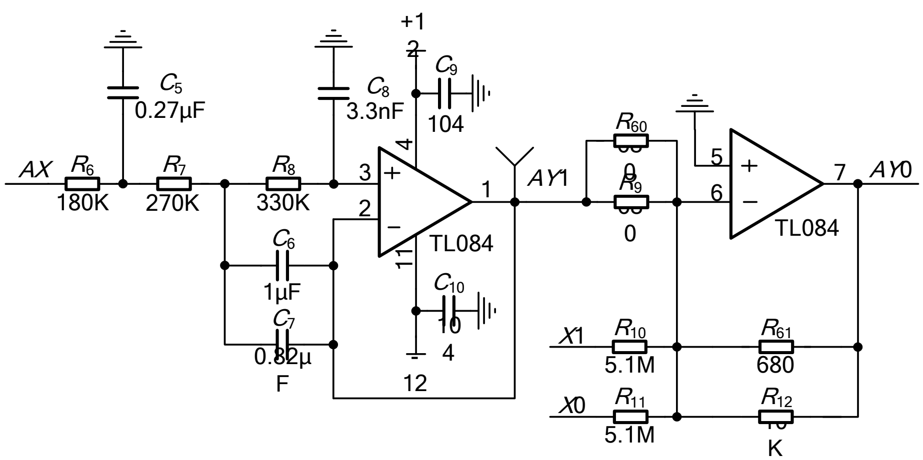

Figure 3. The Amplitude Modulation Circuit

Two DC signals of *AY*0 and *AY*1 are input to 74HC4053 as the second group of input signals. Corresponding selection signal is a square wave signal *FBASE* generated by the control logic unit with a duty ration of 50% and frequency of 10 KHz. Similarly, the output signal *AY* is a square wave signal. Its high-level and low-level magnitudes are *A* and –*A* respectively. The duty ration is 50%. The signal *AY* goes through a series of signal modulations in analog circuit unit will eventually become a sine wave that meets the requirements. The amplitude of the sine wave *A* is obtained here.

3.2. The Design of Frequency Modulation Function (Channel A for an Example)

The diagram of frequency modulation function is shown in Figure 2. After signal *AY* goes through the circuit 2, two sine waves *AZ*0 and *AZ*1 whose frequencies are both 10 KHz and amplitudes are *A* and –*A* will be obtained respectively. Functions of circuit 2 are as follows:

The square wave can deploy into superposition of sine waves of different frequencies, so after *AY* goes through three order low-pass filter set in the circuit 2, the higher harmonics of *AY* are filtered away, and only the fundamental wave is left. Finally a sine wave *AZ*0 with amplitude of *A* and frequency of 10 KHz can be obtained. After *AZ*0 goes through an inverter, *AZ*1 can be obtained.

The sine wave *AZ*0 can be expressed as follows:

$$-A sin[(2\pi f_0)t] \quad (2)$$

The sine wave *AZ*1 can be expressed as follows:

$$A sin[(2\pi f_0)t] \quad (3)$$

Where, f_0 =10 kHz.

*AZ*0 and *AZ*1 are the third group of input signals, and the corresponding selection signal is an square wave signal *PHSA* with an duty ration of 50% and frequencies of 10~11 kHz generated by the control logic unit.

The square wave signal *PHSA* can deploy into superposition sine waves of different frequencies and its expansion is as formula (4).

$$PHSA = \frac{2}{\pi}\left[\cos(2\pi f_p t) + \frac{1}{3}\cos(6\pi f_p t) + \frac{1}{5}\cos(10\pi f_p t) .... + \frac{1}{n}\cos(2n\pi f_p t)\right] \quad (4)$$

Where, f_p =10~11KHz.

After signal *AZ* goes through the circuit 3, a sine wave *SINA* can be obtained. Functions of circuit 3 are as follows:

After *AZ* goes through the three order low-pass filter set in the circuit 3, the higher harmonics of *AZ* are filtered away, and only fundamental wave is left, *i.e.*, signal *SIG* [9]. Its mathematical expression is as follows (5).

$$SIG = \frac{2}{\pi}\cos(2\pi f_p t) \times A\sin(-2\pi f_0 t) \quad (5)$$

Product to Sum Formula is expressed as follows:

$$\sin\alpha\cos\beta = \frac{1}{2}[\cos(\alpha+\beta) + \sin(\alpha-\beta)]$$

The following equation will be obtained:

$$SIG = \frac{A}{\pi}\left[\cos[2\pi(f_p - f_0)t] - \sin[2\pi(f_p + f_0)t]\right]$$

Signal *SIG* goes through a suitable low-pass filter again, and the higher harmonics of *SIG* are filtered away, leaving the low frequency part, *i.e.*, a sine wave with a frequency of (f_p - f_0). So far, the function of frequency modulation has been accomplished.

f_0 is a constant value of 10 KHz, f_p is the frequency of square wave signal *PHSA* produced by control logic unit whose values can be anywhere between 10 and 11 KHz depending on what the project want the frequency of a sine wave to be [10]. For example, in order to get a sine wave with a frequency of 0.5 kHz, only need to set the frequency of square wave signal *PHSA* as 10.5 kHz in the control logic unit.

3.3. The Design of Three Order Low-Pass Filter

The schematic of three order low-pass filter is shown in Figure 4.

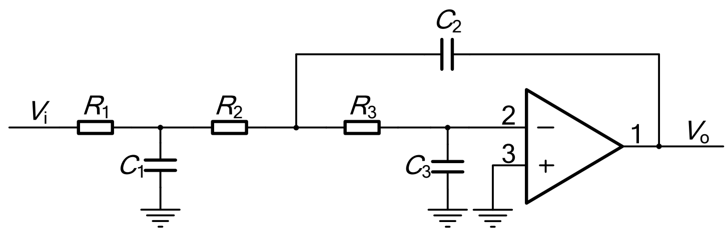

Figure 4. The Schematic of Three Order Low-Pass Filter

The design of three order low-pass filter uses normalized principle, and the cut-off frequency f_z is 5 Hz. The normalized conditions are as follows:

$$R_1 R_2 R_3 C_1 C_2 C_3 = \frac{1}{\omega^3}$$

$$(R_1 + R_2) R_3 C_2 C_3 + R_1 (R_2 + R_3) C_1 C_3 = \frac{2}{\omega^2}$$

$$(R_1 + R_2 R_3) C_3 + R_1 C_1 = \frac{3}{\omega}$$

$$\omega = 2\pi f_c$$

For given resistance values R_1, R_2 and R_3, the values of capacitance C_1, C_2 and C_3 can be obtained [11].

4. Software Design of Phase Modulation and Related Variable Description

Microprocessor unit first converts phase difference to the corresponding phase control key, then microprocessor unit transmits it to control logic unit in a serial transmission way. Control logic unit produces two square wave signals with the same frequency where one signal has an advanced or delayed vector over another, and then control logic unit will output these two square wave signals to the analog circuit unit. Analog circuit unit makes signal modulation and outputs two-way sine waves with the same frequency and phase difference.

4.1. The Determination of Accumulator Length

Functions of all parts of the DDS are achieved by using FPGA device. The frequency of control logic unit is 50MHz, expressed as f_c. The objective of this project is to control the step of frequency increment to be less than 1 Hz and the accuracy of the frequency to be greater than 0.1%. Usually the increment of frequency is used to express the resolution of the frequency. If the length of accumulator is N bits, the minimum resolution of DDS is:

$$\Delta f = \frac{f_c}{2^N} < 1\text{Hz} \times 0.1\%$$

When the value of N is 36 (the minimum integer value), it can meet requirement.

4.2. The Calculation of Frequency Control Key

In DDS system, frequency control key F_{sw} is regarded as the accumulated value of accumulator. The accumulator is similar to a simple number counter. When each clock pulse comes, the accumulator will accumulate frequency control key one time. So the output frequency of DDS can be calculated as follows:

$$f_{out} = \frac{f_c}{2^{36}} \times F_{sw}$$

f_{out} is the frequency of square wave signal that the control logic unit outputs. The frequency f_{out} and the frequency control key F_{sw} have corresponding relationship. From above equation, it turns out that if the f_{out} is determined, the F_{sw} will be established. The F_{sw} can be calculated as follows:

$$F_{sw} = \frac{f_{out} \times 2^{36}}{f_c}$$

4.3. The Calculation of Phase Control Key

This project requires that phase difference is tunable in the 0~359° range, and the resolution of phase difference is no greater than 1°, so:

$$\Delta\theta = \frac{360^\circ}{2^x} < 1^\circ$$

Where, x is the length of phase control key, a length of 16 bits is desirable after calculation. So in order to get two-way sine waves with a phase difference for of (PA-PB)°, the phase control key phase that microprocessor unit sends to control logic unit should be:

$$phase = \frac{(PA\text{-}PB)}{360} \times 2^{16}$$

4.4. The Principle of Phase Modulation

A phase difference is, substantially, an advanced or delayed vector of one signal to another. When two-way sine waves with a phase difference need to be output, only need to let corresponding square wave signals that the control logic unit supplies to A and B have the same advanced or delayed vector.

The microprocessor unit converts the phase increment of A-B into the corresponding phase control key *phase*. Then the microprocessor unit will send phase control key *phase* to the control logic unit in a serial way. The control logic unit uses this phase control key to produce two-way square wave signals with the advanced or delayed vector. The flow chart is shown in Figure 5.

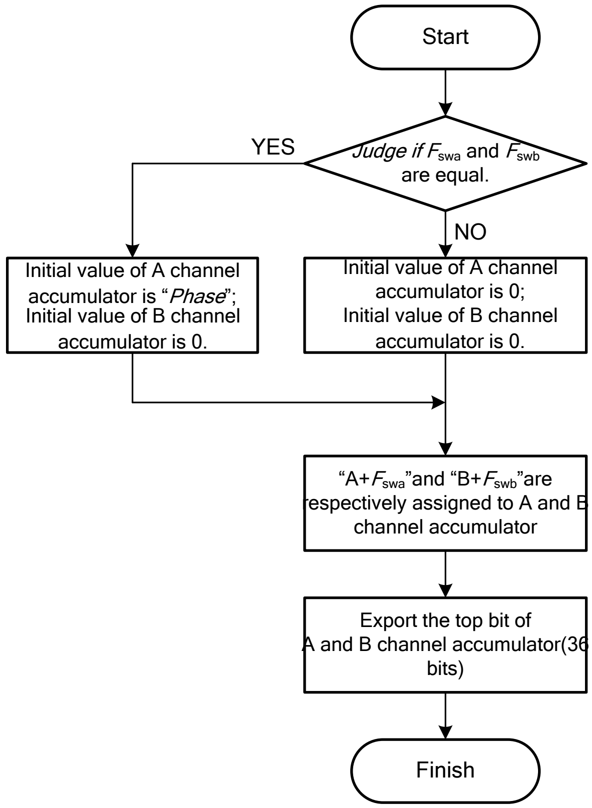

Figure 5. The Simple Flow Chart of Phase Modulation

Only when frequencies of two-way sine waves are equal, there is a phase difference. So, before programming, the first job is to make sure that frequencies of two-way signals are equal. In determining whether the frequencies of two ways of signals are equal or not, only need to check whether the frequency control keys are equal.

When frequency control keys of two signals are equal, the phase control key phase will be assigned to accumulator an as initial value (and the initial value of accumulator B is 0). Then, two accumulators make accumulations with same step *(i.e.*, frequency control key). Finally, the highest bits of two accumulators will be the outputs. So, the control logic unit will get two-way square wave signals where one signal has an advanced or delayed vector over another. The control logic unit sends these two square wave signals to the analog circuit unit in order to make signal modulation. Finally the analog circuit unit will input two channels of sine waves with the same frequency and phase difference for (*PA* - *PB*).

5. Conclusion

Based on the basic principle of DDS and using FPGA and MCU as the control center, this project developed a dual-channel sine wave generator with tunable frequencies, amplitudes and phases in 0 ~ 359. The results showed that the system can produce two-way sine waves which are stable, distortionless and phase tunable with expected accuracy. The operation of system is simple and the system has good performance.

Acknowledgements

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