International Journal of Signal Processing, Image Processing and Pattern Recognition
Vol.7, No.3 (2014), pp.371-384
http://dx.doi.org/10.14257/ijsip.2014.7.3.30

Study on Technology of Carrier Synchronization based on QPSK

Chan Xin

Heilongjiang University
Cheng224@163.com

Abstract

The technology of carrier synchronization is an essential unit in the demodulation technology. This article introduced the related theory of FPGA development, has produced the overall system design and each module function of launches and the carrier synchronization subsystem as well as giving the realization details on the QUARTUSII. And has carried on the function simulation and the succession simulation, has produced the simulation result. After the system simulation, the system design basically reached the target which prearranged.

Keywords: *QPSK modulation, Carrier synchronization, decision feedback loop, FPGA*

1. Introduction

The modern communications system requests signal distance far, message capacity big, transmission quality good, the secrecy is strong. The technology of carrier synchronization is an essential unit in the demodulation technology, it compensated the displacement and the phase deviation which created in the channel transmission and the demodulation process [1]. The subsequent signal processing will not work if the carrier synchronous performance is not good. Therefore the performance of the system will be directly affected by the estimation performance. Carrier synchronization system should have high efficiency and precision, in other words it should have faster synchronization setting time and longer holding time. In engineering practice, in order to achieve results of carrier synchronization, we usually use the phase-locked loop to acquire and track the carrier component, then solving the received signal.

Phase locked loop can track the input signal phase, is an automatic tracking system. It is widely used in various fields of radio, has become an indispensable part of many equipments, such as communication, radar, navigation, electronic equipment, *etc.*, The PLL have some characteristics such as carrier tracking, modulation tracking and high frequency stability, its performance has important significance in the electronic design. So it not only has certain significance but also is a challenging topic.

2. Study on the Loop of Carrier Synchronization

Though decision feedback loop and four-phase inverse modulation ring has identical phase characteristics, but decision feedback loop has omitted secondary modulation and all the nonlinear processing is carried out at base band, so that its circuit is simpler. The structure is illustrated in Figure 1.

ISSN: 2005-4254 IJSIP

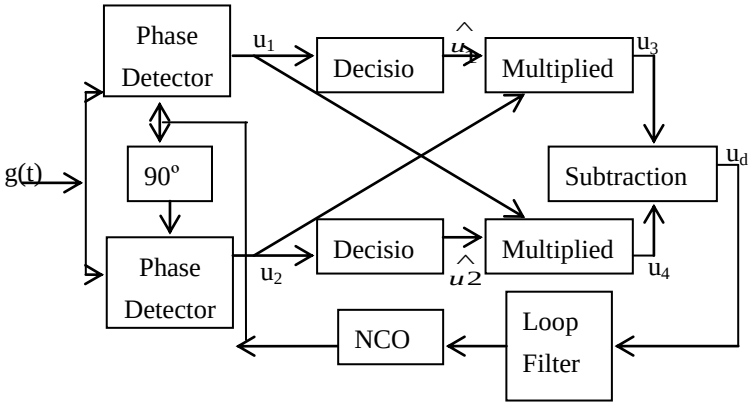

Figure 1. The Structure of Decision Feedback Loop

The output from phase detector is:

$$u_1 = \frac{x(t)}{2}\sin\varphi + \frac{y(t)}{2}\cos\varphi \tag{1}$$

$$u_2 = \frac{x(t)}{2}\cos\varphi + \frac{y(t)}{2}\sin\varphi \tag{2}$$

After Decision, these two base band signals should have met:

$$g(t) = \begin{cases} A, & 0 \le t \prec \dfrac{t_S}{2} \\ -\mathrm{A}, & \dfrac{t_S}{2} \le t \le t \end{cases} \tag{3}$$

Then:

$$u_3 = k_m \hat{u}_1 u_2 = k_m \hat{u}_1 \left[\frac{x(t)}{2}\cos\varphi - \frac{y(t)}{2}\sin\varphi \right] \tag{4}$$

$$u_4 = k_m \hat{u}_2 u_1 = k_m \hat{u}_2 \left[\frac{x(t)}{2}\sin\varphi - \frac{y(t)}{2}\cos\varphi \right] \tag{5}$$

The output of the subtraction is:

$$\begin{aligned} u_d &= u_4 - u_3 \\ &= \frac{k_m}{2}\left[\hat{u}_2 x(t) + \hat{u}_1 y(t)\right]\sin\varphi \\ &\quad + \frac{k_m}{2}\left[\hat{u}_2 y(t) - \hat{u}_1 x(t)\right]\cos\varphi \end{aligned} \tag{6}$$

Finally achieved:

$$u_d = \begin{cases} \mathrm{k}_d \sin\varphi & (\varphi \in 1,4,5,8) \\ -\mathrm{k}_d \cos\varphi & (\varphi \in 2,3,6,7) \end{cases} \tag{7}$$

The phase characteristics of the loop are shown in the Figure 2.

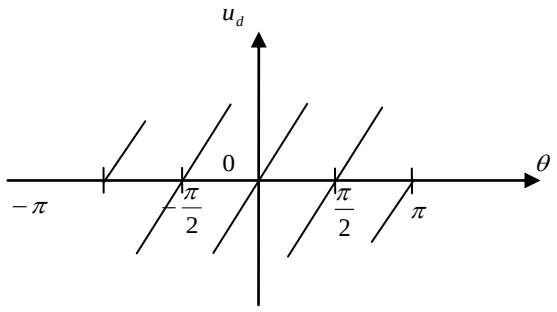

Figure 2. The Phase Characteristics of the Loop

The carrier frequency offset and phase offset is needed to be extracted from the input signal by feedback loop. Its principle is: First demodulate the received signal, and then the phase error information in the received signal should be offset by the demodulated signal. So we can get the correct digital signal through the offset carrier error method. In turn the carrier offset estimate which is extracted by PLL available for the previous coherent demodulation.

3. Study on the Principle of QPSK Demodulation

We usually use coherent demodulation for QPSK signal, the block diagram is shown in Figure 3.

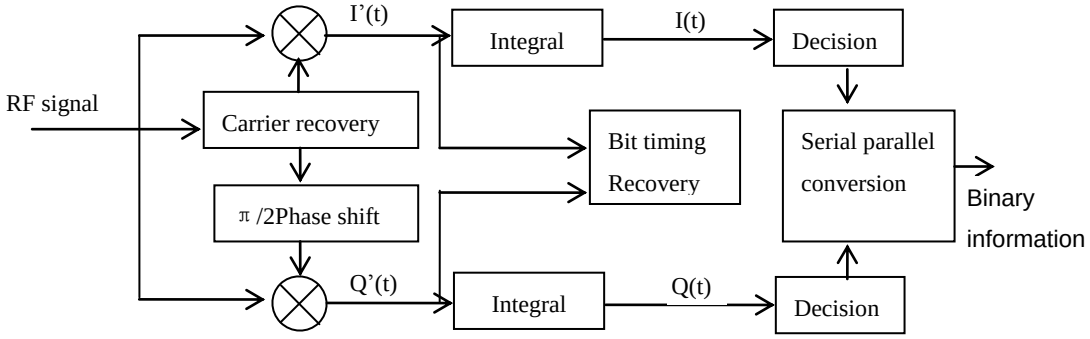

Figure 3. The Principle Diagram of Coherent Demodulation

From the figure we can see that multiply the received RF signal by local recovery carrier, than go through the low-pass filtering, we obtained two signals which are the in-phase signals and orthogonal signals ,that is I'(t) and Q'(t). The original information can be restored after level decision and conversion. Of course, there should have a process of differential decoding during demodulating if modulation is the differential coding.

If the received RF signal is:

$$S(t) = A(t)\cos\omega_c t + B(t)\sin\omega_c t \tag{8}$$

A (t) is the branch of in-phase signal; the B (t) is orthogonal signal branch, ω_c is carrier frequency, then the value of $I'(t)$ and $Q'(t)$ is

$$\begin{aligned} I'(t) &= S(t).\cos\omega_c t \\ &= [A(t)\cos\omega_c t + B(t)\sin\omega_c t].\cos\omega_c t \\ &= A(t)\cos^2\omega t + \frac{B(t)\sin\omega_c t}{2} \\ &= \frac{A(t)}{2} + \frac{A(t)\cos 2\omega_c t}{2} + \frac{B(t)\sin 2\omega_c t}{2} \end{aligned} \quad (9)$$

$$\begin{aligned} Q'(t) &= S(t)\cdot\sin\omega_c t \\ &= \left[A(t)\cos\omega_c t + B(t)\sin\omega_c t\right]\cdot\sin\omega_c t \\ &= \frac{A(t)\sin 2\omega_c t}{2} + B(t)\sin^2\omega_c t \\ &= \frac{A(t)\sin 2\omega_c t}{2} + \frac{B(t)}{2} + \frac{B(t)\cos 2\omega_c t}{2} \end{aligned} \quad (10)$$

After Integral (low pass filter), the value of $I(t)$ and $Q(t)$ is shown in formula (11):

$$\begin{cases} I(t) = \dfrac{A(t)}{2} \\ Q(t) = \dfrac{B(t)}{2} \end{cases} \quad (11)$$

After verdict use the formula (11), we can obtain the results which are shown in Table 1, the ”1” is corresponds 0 and the “-1” corresponds to the 1 binary signal.

Table 1. The Results of QPSK Demodulation

$A(t)$	$B(t)$	$I(t)$	$Q(t)$	in-phase branch after verdict	orthogonal branch after verdict
1	1	1/2	1/2	0	0
1	-1	1/2	-1/2	0	1
-1	1	-1/2	1/2	1	0
-1	-1	-1/2	-1/2	1	1

4. Overall Design on Carrier Synchronization System

4.1. Hardware Design

This system achieved a carrier synchronization system base on the FPGA chip-EP1C20 F400 which is made by Altera Corporation. The system of hardware structure is shown in Figure 4.

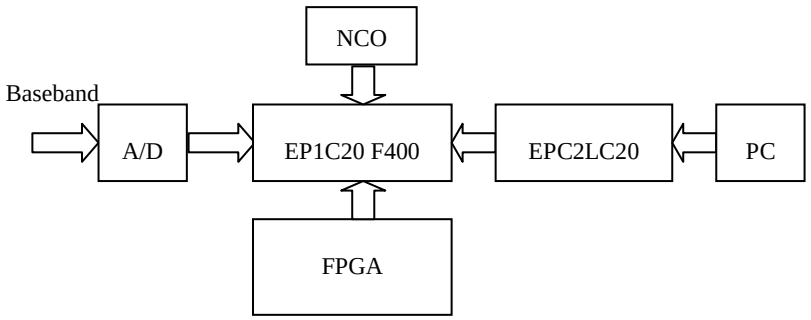

Figure 4. The Block Diagram of Hardware Structure System

The specific parameters of EPC2LC20 are as follows:
The rate of data signal code: 8kbps
The schemes of modulation: QPSK
The frequency of carrier: 700 kHz
The following is the working process of this system: First design and program the software on computer. Second download the program to EPC2LC20 after compiled simulation and validation function correctly, EPC2LC20 put the program configuration to FPGA chip each power. The System send the received signal which is collected by A/D to the FPGA, FPGA is responsible for modulation, carrier synchronization and decision finally output.

4.2. Design of Transmitter Subsystem

The overall block diagram of QPSK transmitter subsystem is shown in Figure 5. Transmitter subsystem generate QPSK modulated signal, the receiving portion sampled and demodulated the received signal. The focus of this study is to extract the synchronized carrier in the demodulation process.

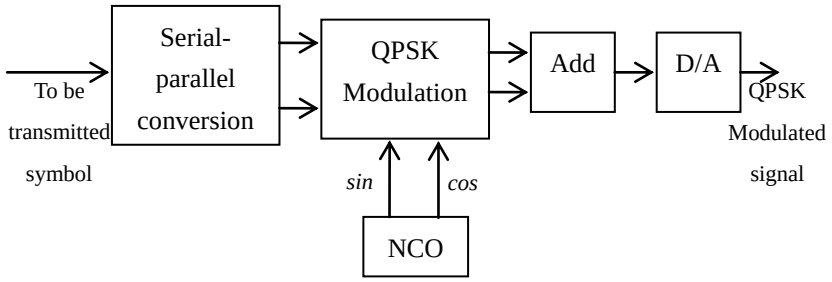

Figure 5. The Block Diagram of the Overall Design of the System

In transmit subsystem, the baseband signal first passes through the Serial-parallel conversion into two branches, one is odd symbols, the other is even symbols. At this time each branch symbol width as twice as usual. Then modulated each branch by QPSK demodulate. Actually, QPSK modulator is constituted by two multipliers, It is multiplied by module I which from serial-parallel conversion and the Q-channel data from NCO. Carrier phase of the two path is different, they are mutually orthogonal, one called-phase branch, *i.e.*, I branch; another called quarter branch, *i.e.*, Q branch. After have modulated two branches respectively, added the modulated signal, converted into an analog signal through D/A, then the signal has be modulated.

4.3. Design of Carrier Synchronization Subsystem

The system of carrier synchronization is a complex digital signal processing, its main functions is: the analog-to-digital conversion, the conversion of the digital IF signal to the baseband and carrier synchronization, and the string conversion. The input signals of carrier synchronization system are modulated analog IF signal, therefore the reception signals need for analog-to-digital conversion process before entered into the system. The course of their work are as follows: first AD9054 converting the analog IF signal into a digital signal, the signals diverged into two legs to digital down-conversion, then multiplied with the two orthogonal carriers from NCO, and then integrated, decision , finally the original signal have be restored. The block diagram of carrier synchronization subsystem is shown in Figure 6.

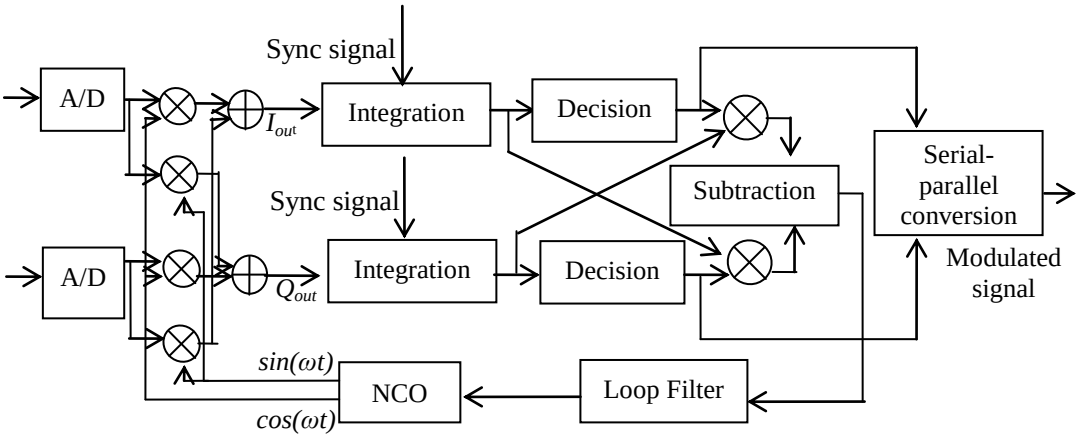

Figure 6. The Block Diagram of Carrier Synchronization Subsystem

Assuming the IF signal received by I-channel is:

$$I_{in}(t) = \cos(\omega t + \varphi) \tag{12}$$

The IF signal received by Q-channel is:

$$Q_{in}(t) = -\sin(\omega t + \varphi) \tag{13}$$

The frequency of this IF signal is lower, at about a few hundred hertz. Multiplied by low-IF which is produced by FPGA, then cross sum, the two signals I, Q is

$$I_{out} = \cos(\omega t + \varphi).\cos(\omega t) + \sin(\omega t + \varphi).\sin(\omega t) = \cos\varphi \tag{14}$$

$$Q_{out} = -\sin(\omega t + \varphi).\cos(\omega t) + \cos(\omega t + \varphi).\sin(\omega t) = -\sin\varphi \tag{15}$$

The data rate of signal of the I, Q is 33M, after the accumulation, we get the digital signal I_{Σ} and Q_{Σ} ,then send them into the module of carrier tracking , adjust the frequency of the NCO, so that the two achieve synchronization, and then the final result should be get after the serial-to-parallel conversion is completed.

The main parameters of the carrier synchronization system:

Data Rate: 8kbps

Carrier frequency: 700 kHz

Capture bandwidth: $\pm$ 1 kHz

Modulation: QPSK

NCO clock: 33MHz
A/D sampling rate: 33MHz

5. Software Implementation of Transmitter Subsystem

5.1. A Design and Implementations of the Serial-parallel Conversion

The non-return-to-zero binary sequence is divided into parity two, each symbol width expansion by Tb to 2Tb. The odd number of branch entering data channel after a Tb delay, the even branch data directly into the channel. The simulation results are shown in Figure 7.

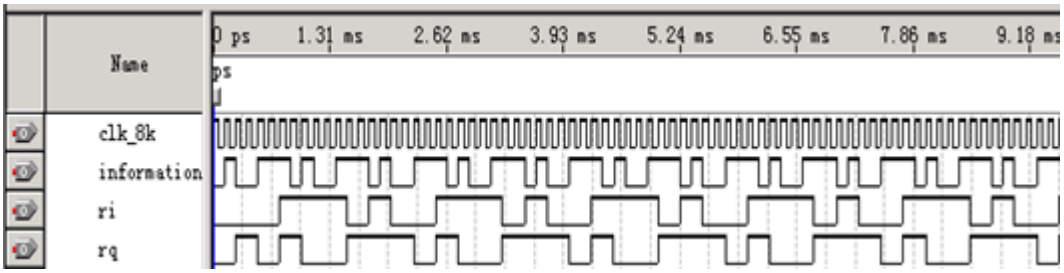

Figure 7. Simulation Results of Serial-parallel Conversion

The 'information' is before the serial-to-parallel conversion signal, Data rate is 8kbps; ri and rq is the I, Q which is obtained after the serial-parallel conversion, their data rate is 4kbps. Serial-to-parallel conversion results meet design requirements.

5.2. Design and Implementations of the NCO

NCO (Numerically Controlled Oscillator) obtains a low frequency oscillation signal by phase accumulation based on a given high frequency clock. It needs to satisfy the Nyquist sampling theorem, that is produced carrier frequency is lower than the clock frequency 1/2. Generally, NCO is composed of the phase word register, the phase accumulator and sine lookup Table. Its schematic diagram is shown in Figure 8.

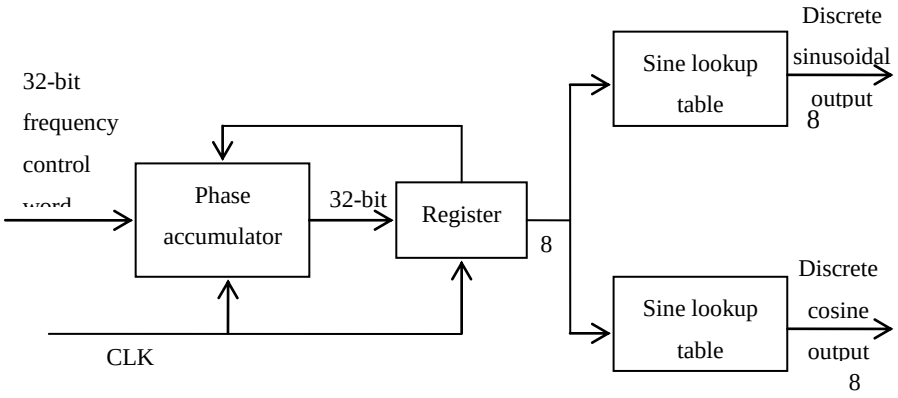

Figure 8. Schematic Diagram of NCO

Under the control of the clock pulse, NCO accumulated on the input of the frequency control word, the phase accumulator will overflow when the accumulation is full. At that moment, output of accumulator corresponds to the phase of synthetic cycle signal, and the phase is periodically changed within the range of $0 \sim 2\pi$. The phase accumulator median is N, the maximum output is $2^N - 1$, according to the phase of 2π, accumulator outputs a corresponding phase code, obtained the amplitude of the sinusoidal signal through look-up the Table. The frequency control word is K that is incremental Steps of the phase accumulator, after $2^N / K$ times accumulate, the phase accumulator overflowed, then a cycle action is completed. The relationship between output frequency f_0 with the clock frequency $f_{\_CLK}$ satisfied:

$$f_0 = \frac{K}{2^N} f_{\_CLK} \tag{16}$$

The minimum frequency resolution of DDS is up to $\frac{1}{2^N} f_{\_CLK}$. In this design, the value of N is 32-bit, f_0 is 700kHz, $f_{\_CLK}$ is 33MHz, then

$$K = \frac{f_0}{f_{CLK}} \times 2^N = \frac{700}{33000} \times 2^{32} = 91105366 \tag{17}$$

The simulation results shown in Figure 9

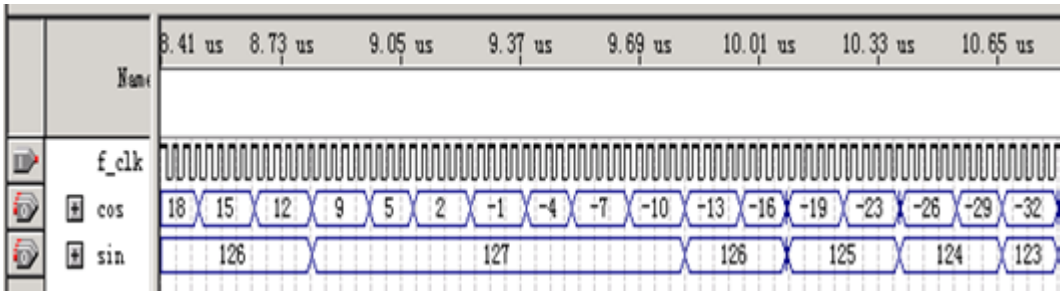

Figure 9. Simulation Results of NCO

5.3. Design and Implementations of QPSK Modulator

In design of QPSK modulator module, we mainly consider the level conversion, the two multipliers and an adder. The multiplier and an adder both have arithmetic overflow, it is generated in the case of the same number sum or subtraction of two different numbers. To the addition operation, there is will occurred overflow when if second highest bit carried to the most highest bit, but the maximum bit doesn't has carry output bit, or even if second high doesn't carry to the most significant bit ,but the most significant bit has carry output, in other words two positive numbers added, the result is out of range, become negative. Similarly, two negative subtracted, the result is out of range, become a positive number. So, it is necessary to consider the problem of overflow when designs numerical computation.

The implement of multiplier is relatively simpler, let '0' corresponds to the low level '+1', and '1' corresponds to the high level '-1'. So the carrier multiplied with '+1' or '-1' by judging the send signal is 0 or 1. First judged the two-way signal I and Q, if its value is '1', seek the

complement code of 8 bit carrier signal, and then output, otherwise if the value is '0',then output these 8-bit digital signal directly.

The adder has been achieved by macro function module of LPM_ADD_SUB. In order to prevent an overflow in the arithmetic, the data sent by the multiplier must be processed. After multiplied, the signal is expanded from 8 bit to 9, then, truncating the last bit, thus, the data fed to the adder module is still 8 bit, halved in size, but the sign bit unchanged. Call adder macro module LPM_ADD_SUB by way of instantiation, and then setting instance parameters.

The simulation results are shown in Figure 10.

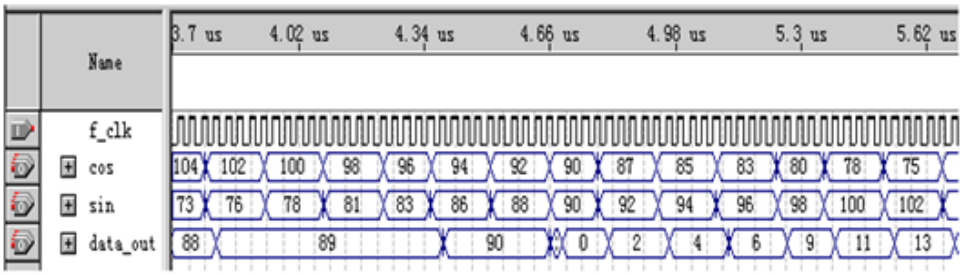

Figure 10. The Simulation Results of QPSK Modulation

6. Software Implementation of Carrier Synchronization System

6.1. Design and Implementations of the Mixer Module

The module of mixer is two multipliers which is eight multiplied by eight, the eight-bit data of the A/D output respectively multiplied by the orthogonal carrier of NCO output, and then obtained two orthogonal signal after cross the adding and subtracting. The result is a signed 16-bit.

6.2. Design and Implementation of Data Symbol Integrator

The data from mixer module into the data symbols integrator, its role is to low pass filtering. Here, we does not consider the problem of timing synchronization, the synchronizing signal is replaced by the system clock, control signal of the integrator to be seen as the system clock signal, there while be a synchronizing signal in every clock cycle. The structure is shown in Figure 11.

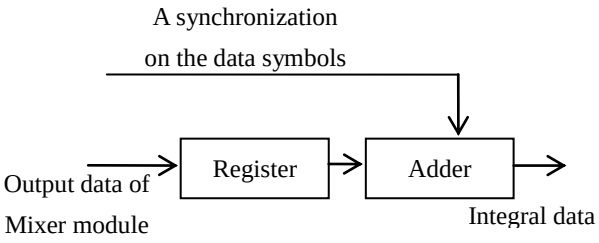

Figure 11. The Structure of Data Symbol Integrator

6.3. Design and Implementation of Feedback Control Module

This article used the decision feedback loop to achieving carrier synchronization, If the frequency phase of the NCO output signal is different from the IF carrier, the frequency of the NCO can be adjusted through the phase difference of the demodulated output, so that achieved the purpose of synchronization. As follows:

Assuming the frequency difference of the IF signal which is output by NCO is: $\Delta\omega$, the phase difference of beginning is $\Delta\varphi$, the total phase error is: $\Delta\phi_e = \Delta\omega t + \Delta\phi$.

$$I_\Sigma(k) = A_\Sigma \cos(\phi(k) - \Delta\phi_e + 4/\pi) \tag{18}$$

$$Q_\Sigma(k) = -A_\Sigma \sin(\phi(k) - \Delta\phi_e + 4/\pi) \tag{19}$$

The algorithm to generate a control signal of error based on QPSK is:

$$S_d = Sign[I_\Sigma(K)]Q_\Sigma - Sign[Q_\Sigma]I_\Sigma \tag{20}$$

Put $\phi(k) = 0, \pi/2, \pi, 3\pi/2$ into the equation obtained that:

$$S_d = \sqrt{2}A_\Sigma \sin\Delta\phi_e \tag{21}$$

The signal feedback control the oscillation frequency of NCO after has passed the loop filter, make the value of $\Delta\phi_e$ tends to 0, then can achieve synchronization coherent process. The transfer function of loop filter is:

$$F_n = K_1 + \frac{1}{4}K_2 \frac{Z^{-1}}{1 - Z^{-1}} \tag{22}$$

The block diagram of feedback control shown in Figure 12

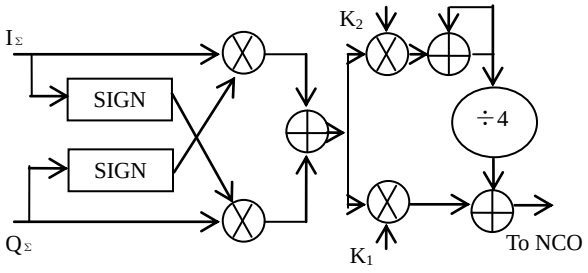

Figure 12. The Block Diagram of Feedback Control

Wherein $\frac{Z^{-1}}{1 - Z^{-1}}$ illustrates the output of the adder has a delay in the K_2 branch, K_1 and K_2 is inputted by the external, the branch of K_1 (direct channel) affect the speed of change into loop track wave frequency, the branch K_2 (integral channel) not only affects the speed of the input frequency tracking of carrier, but also inhibition of input noise certainly.

6.4. Design and Implementation of Decision Module

This module primarily responsible for judgment of the two-way data which is outputted by integrator, thus restoring the two-way original data of I and Q , the original input data can be obtained through parallel-to-serial conversion. If the value of I_{Σ} and Q_{Σ} is greater than zero output '1' ,otherwise output '0', serial output the verdict at rate of 2 times , and then the original input data is got.

7. The Simulation Results of Carrier Synchronization System

Here the carrier synchronization loop is effective within the scope of $-\frac{\pi}{4} \sim +\frac{\pi}{4}$, the rate of data transmission is 8kHz, so the transmission rate of each channel QPSK signal is 4kHz, the frequency offset can be captured is ± 500Hz. The integration time should be shortened to a quarter of the original, *i.e.*, 16 kHz. In theory the maximum bandwidth the design of carrier synchronization loop of this paper can capture up to ± 2 kHz, it can meet the requirements of system which ask ± 1 kHz capture bandwidth.

Figure 13 is a simulation result of the carrier synchronization loop, in which M_add is the word of frequency control, safc is the output of the phase discriminator, M1 is the output of the filter. The carrier frequency of the transmitting side is set to 703 kHz.

According to equation (17)

$$K = \frac{f_0}{f_{CLK}} \times 2^N = 91495818$$

The value of K is 91495818.

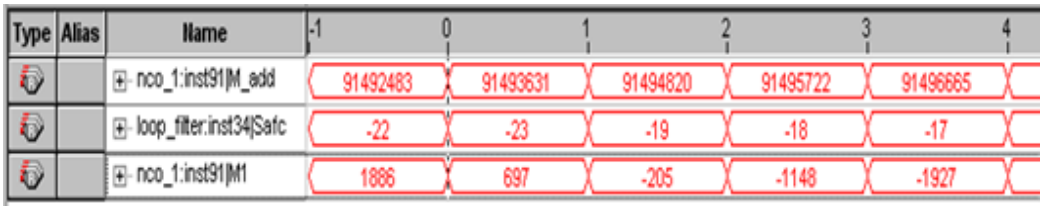

Figure 13. The Simulation Results of Carrier Synchronization Loop

From the figure can be seen that the output of the phase detector changes within a small range, the carrier of receiving end and transmitting side have achieved synchronization.

When the transmitting side center of the carrier frequency is varied within a range of 703 kHz $\pm$ 1 kHz, the results of simulation show that the carrier synchronization loop can achieve carrier phase lock correctly.

Figures 14 and 15 show that the received carrier can be synchronized with the transmitting side carrier when the carrier frequency of the transmitting side is 703.5 kHz and 704 kHz, *i.e.*, increase of 500 HZ and 1 kHz respectively. According to the equation (17)

Shows that the value of K (the word of frequency control word) is 91560893 and 91625968.

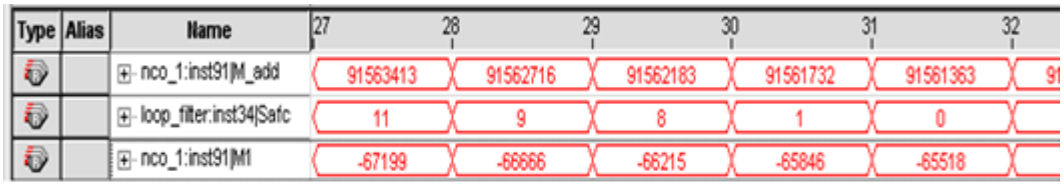

Figure 14. +500 Hz Carrier Deviation from the Center Frequency

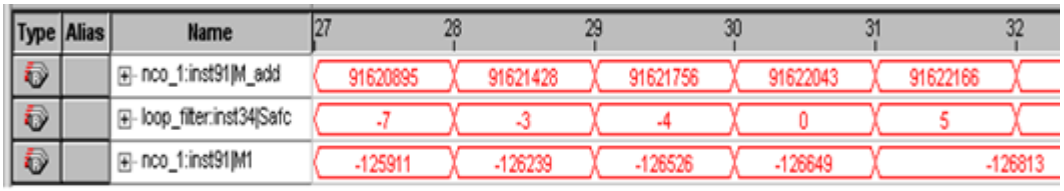

Figure 15. +1k Hz Carrier Deviation from the Center Frequency

Figures 16 and 17 show that the received carrier can also be synchronized with the transmitting side carrier when the carrier frequency of the transmitting side is 702.5 kHz and 702 kHz, *i.e.*, reduce of 500 HZ and 1 kHz respectively. We can calculate the value of K (the word of frequency control word) according to the equation (17)

The value of K is 91430743 and 91365667.

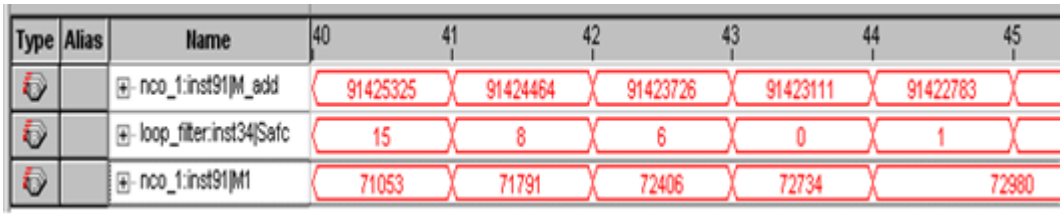

Fig.16. -500 Hz Carrier Deviation from the Center Frequency

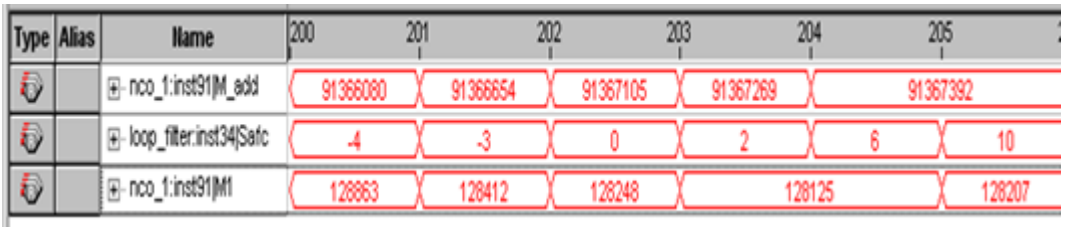

Figure 17. -1k Hz Carrier Deviation from the Center Frequency

The simulation results show that the capture bandwidth of carrier synchronization loop has achieved 1 kHz, to meet of system design requirements on frequency offset lock.

8. Conclusion

This paper discusses how to achieve carrier synchronization through digital phase-locked loop methods, design of the structure and parameters of the carrier synchronization loop system based on a digital decision feedback loop, given the calculation process of various parameters. Designed of the time domain model of carrier synchronization loop by QUARTUS II, simulated the working process of the various components of the loop. This

paper proved the correctness and feasibility of the algorithm, laid a foundation for the next study of the software receiver.

References

[1] H. Liu and N. Zhang, "The simulation study of QPSK signal coherent carrier extraction Systems," Engineering and Electronics, vol.4, **(2003)**, pp. 394-396.
[2] L. Tao, Z. Yu and X. Wang, "The implementation of QPSK modulator base on FPGA", Communications technology, vol. 1, no. 12, **(2002)**, pp. 23-24.
[3] H. Yan, "Research on Some Key Technologies of Carrier Recovery in Wireless Communication", Ph.D. Thesis, Dept. University of Electronic Science and Technology of China, Hefei, **(2012)**.
[4] Z. Ye, "Design and Implementation on Algorithm of Digitized Carrier Synchronization Loop", MA.Sc. Thesis, Dept. Harbin Institute of Technology, china, Harbin, **(2006)**.
[5] W. Cheng, et al., "A 3b 40GS/s ADC-DAC in 0.12 μmSiGe, ISSCC Dig.", Tech. Papers, **(2004)**, pp. 262-263.
[6] H. F. Haunstein, W. Sauer-Greff, A. Dittrich, K. Sticht and R. Urbansky, "Principles for electronic equalization of polarization-mode dispersion", Journal of Light wave Technology, vol. 22, **(2004)**, pp.1169-1182.
[7] J. Wang and J. M. Kahn, "Performance of electrical equalizers in optically amplified OOk and DPSK systems", IEEE Photonics Technology Letters, vol. 16, **(2004)**, pp. 1397-1399.
[8] Y. Zha, B. Goebel, M. Kuschnerov, N. Hanik, "On the effect of polarization-mode dispersion onthe channel capacity of coherent fibre-optic communication systems", International Conferenceon Transparent Optical Networks, vol. 9, **(2007)**, pp. 155-159.

Authors

Chan Xin, 1978-12, Electronics and Communication Engineering Master's degree, major field is Carrier synchronization and Digital receiver.