International Journal of Signal Processing, Image Processing and Pattern Recognition
Vol.7, No.2 (2014), pp.177-186
http://dx.doi.org/10.14257/ijsip.2014.7.2.17

Research of High-Speed and Stable Photodetector of Monolithic Optocoupler Chip

Lei Tian[1,2] and Xinquan Lai[1,3]

[1]*Institute of Electronic CAD, Xidian University, Xi'an, Shaanxi 710071, PR China*
[2]*School of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an, Shaanxi 710121, China*
[3]*Key Lab of High-Speed Circuit Design and EMC, Ministry of Education, Xidian University, Xi'an, Shaanxi 710071, China*
tianlei@xupt.edu.cn

Abstract

Designed and fabricated a monolithically integrated high-speed optical receiver module optocoupler chip, which contains "N_{well}-$P_{epitaxial}$-P_{sub}" model for the photoelectric detector (PD), the transimpedance amplifier (TIA) and the subsequent processing circuits. Clarify the circuit structure of the TIA and the adjustable gain theory. Detailed analysis the frequency response of the PD models and simulated the PD theoretical analysis. Simulation results showed that when the temperature is constant and the photocurrent change from 5uA to 80uA, the response speed of the PD and TIA module change quickly. When the photocurrent (I_{ph}) unchanged and the test temperature (T) change from -25 ℃ to 125 ℃, the delay time does not exceed 10ns. Tape-out with the 1P3M 0.35um BCD process and the test results showed when the T is 25 ℃ and the I_{ph} is 20uA, the delay time of the whole chip are 155ns and 205ns. When the T is125 ℃ and the I_{ph}h kept constant, the delay time of the whole chip are 153ns and 220ns.The results show that the photodetector design with high-speed response capability, combined with the TIA gain adjusted in real time, the high-speed monolithic integration optocouplers can be established.

Keywords: *photodetector; optocoupler; TIA; response time*

1. Introduction

Optocoupler provides an effective means for the electrical isolation between the microelectronic signals [1]. It is widely used in military and aerospace requirements of high reliability field advantages of small size, long life, non-contact, anti-interference ability. At present, high-performance, low-cost and compatible monolithically integrated optical receiver chip is very active [2], optoelectronic integrated circuits (OEIC, Optoelectronic Integrated Circuits) has become a hot research topic [3].

Saša Radovanović [4] used CMOS processes developed high-speed light receiving detector can achieve high performance PD module, but could not achieve it through a low-cost business process. Yang Yang [5] using fullerene to construct the PD module, although a substantial improvement of the response speed optocoupler, but did not consider the circuit structure in depth which can not meet the real-time adjustment of the TIA. Nowadays, high speed integrated optical receiver chip is in the research stage [6-8] and some researchers arer also working to develop it [9-11]. There are still many urgent problems in developing the high performance PD and its subsequent processing circuit [12].

In this paper, based on the 1P3M 0.35umBCD process designed integrated optical receiver chip which can be used in 840nm control. The PD model with the N_{well}-$P_{epitaxial}$-

ISSN: 2005-4254 IJSIP

P_{sub} structure has a faster response can greatly shorten the response time from the photons incident to the photocurrent generated [13]. The TIA is the differential transimpedance amplifier, its high sensitivity can be larger to improve the response speed of the chip and reduce the entire chip delay from input to output.

2. Optical Receiver Structure

2.1. Receiver Circuit Structure

The system block diagram of the optical receiver chip is shown in Figure 1. In the process of transmission of the light, the signal became very weak when it reached the receiver. PD under the reverse voltage received the photons and the photocurrent is generated. The photocurrent flowed through the TIA and the subsequent circuits. In order to achieve a good match with the PD, obtain a lower noise and greater bandwidth, the gain of the preamplifier can not be too high and could adjust according to the threshold of the preceding stage noise. The range of the output voltage of the preamplifier is approximately several to tens of mill volts.

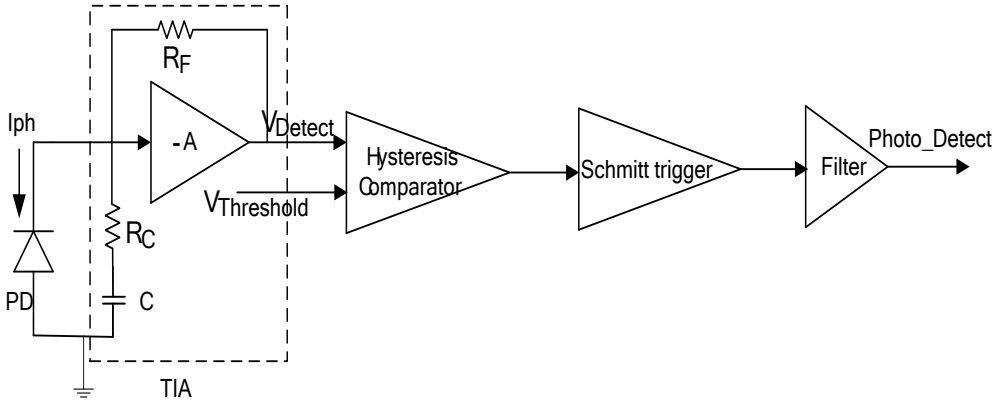

Figure 1. Optical Receiver System Block Diagram

This module consists of a light detector diode array [14, 15], transimpedance amplifier, hysteresis comparator and filter circuit. When the LED of the transmitter module emits light, the PD receives its photons and converted it into the photocurrent. The current flowing through the transimpedance amplifier and then this current was changed into the voltage V_{Detect}. The subsequent hysteresis comparator compared the V_{Detect} and its own threshold $V_{Threshold}$ when it detected the V_{Detect}. When it is higher than the threshold, the signal passed, otherwise the output is zero.

Schmitt trigger is used for signal shaping and filter is used to filter out high frequency signal. This circuit includes a hysteresis comparator and the filter circuit. It can filter out the common mode noise in the input of the photocoupler and output the control logic for the next circuit.

2.2. TIA Circuit

Considering the factors such as noise, gain and power consumption, this circuit uses the differential structure as the basic structure of TIA. Shown in Figure 2, the TIA has a high gain with the feedback mechanism the DC bias is more stable [16].

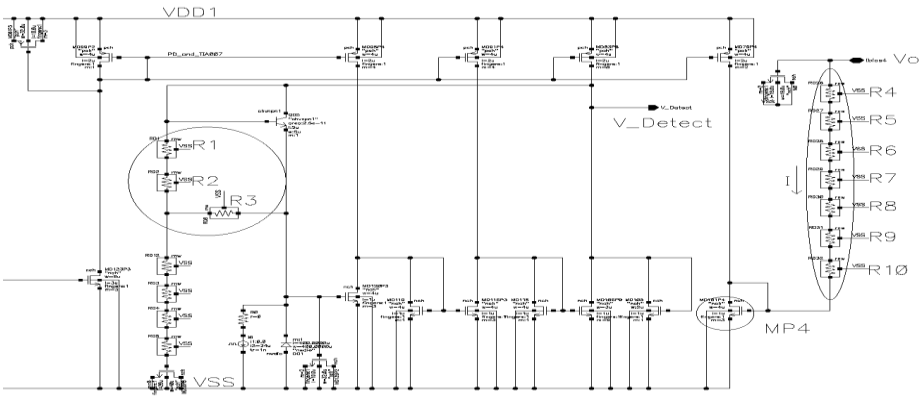

Figure 2. PD_TIA Circuit Diagram

In Figure 2, the resistances in the left circle are composed by three resistors (R1, R2, and R3) in series which length is 72um and width is 3um. Let the three same dimension shorting resistors as the option. When the square resistance is 1kΩ then the value of R1 to R3 is 36kΩ. In the non-adjustment cases, the gain of the transimpedance amplifier is 108kΩ. Through shorting resistors or fusing metal wire, the range of the adjustable gain is 36kΩ ~ 216kΩ and the step is 36kΩ. The ratio of the range is 33.3% to 200% and the step is 33.3%.

In the right circle, the structure of the MOS transistor (MP4) series the resistances (R4~R10) is used to generate the threshold voltage of the light detection module. The seven resistors in series which length is 17um and width are 5um. Also let the shorting resistors to be the Option. For the same square resistance, then the value of R4 to R10 is 4.25kΩ . The all resistances (R_A) are 29.75kΩ . The current (I) through the resistances is 10uA, so the voltage on the resistances (V_o) is 0.3V and the voltage on the MP4 is 1.05V. So in the typical case the V_{Detect} is 1.35V. In the no lighting circumstances the V_{Detect} is 1.10V. Through shorting resistor or fusing metal wire, the threshold voltage can be changed from 1.05V to 1.475V and the step is 42.5mV.

Thus the TIA module can change the gain by the current which came from the PD module. Then the response time will be reduce. At the same time, according to the noise with the photocurrent to adjust the threshold voltage. So as to avoid amplify the noise in the preceding stage [17].

3. PD Model and Response Time Analyze

3.1. PD Model

According with the existing 0.35umBCD process using the N_{well}/P_{sub} structure can build the PD model of the optical receiver chip. Its basic structure is shown in Figure 3:

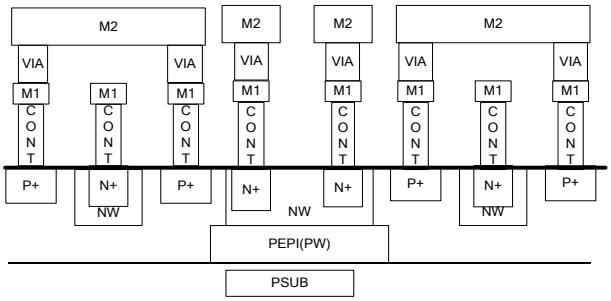

Figure 3. PD Module Structure

In the process of designing the PD [18, 19], using the N_{well}-$P_{epitaxial}$-P_{sub} vertical structure, reduce the substrate on the response speed of movement due to the diffusion of the light-generated carriers [20]. Let the N^+ buried layer as the cathode of the PD and the cathode connected to the high potential. Let the P^+ buried layer as the anode of the PD. The P_{sub} isolated the PD modules and other devices.

According to the maximum size (W = 35um) of the detection diode by the actual process, the design area of the PD is 400um*400um. Select 200 parallel light receiving array which W is 20um and L is 20um. CONT is the connection hole between the first metal layer (M1) and the P^+/N^+. VIA is the connection hole between the MI and M2.

3.2. Photocurrent of the Equivalent PD

In order to analyze the photocurrent and the response time of the PD directly [21], according to the Figure 3, the PD can be equivalent by Figure 4. The current source I_{ph} represents the current generated by the incident radiation. The diode D represents the PN junction. In addition, a junction capacitance C_j and a shunt resistance R_{sh} are in parallel with the other components. Generally the value is so big that can be neglected.

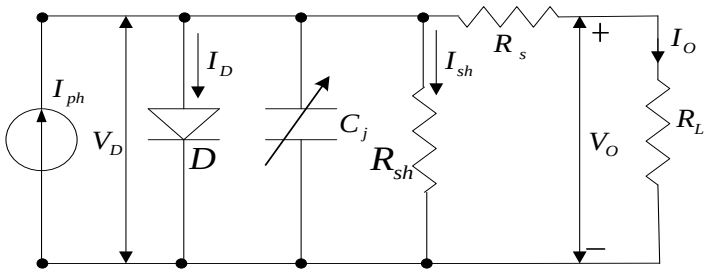

Figure 4. Equivalent Model for the PD

In the above Figure, V_D is the voltage across the diode. I_D is the diode current. I_{sh} is the shunt resistance current. V_O is the output voltage. The open circuit voltage V_O is the output voltage when I_O equals 0. Using the above equivalent circuit, the output current I_O is given as follows:

$$I_o = I_{ph} - I_D - I_{sh} = I_{ph} - I_S(\exp\frac{eV_D}{kT} - 1) - I_{sh} \quad (1)$$

Because the PD has different responsivity for the different wavelengths, when the wavelength is 840nm, the responsivity of the PD gets the maximum value $0.5A \cdot W^{-1}$, as showed in Figure 5.

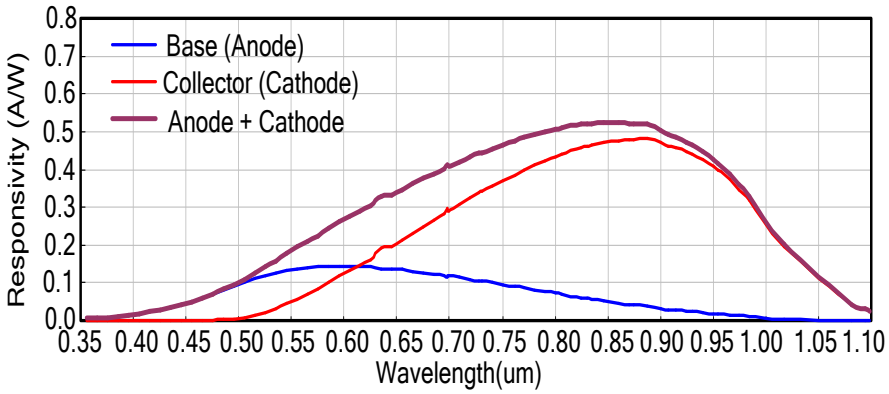

Figure 5. PD Spectral Response

Generally when the incident light current is 20mA, the incident optical power is 1.71mW. The range of the coupling coefficient is 0.05 ~ 1. With the photocurrent formula:

$$I_{ph} = I_{in} \times \frac{P_{in}}{20\ mA} \times R \times S \tag{2}$$

We can calculate the current with different incident light. The specific data as shown in Table 1:

Table 1. Photocurrent with I_{in} and S

	I_{in} (7mA)	I_{in} (16mA)
S = 0.05	11.97	27.36
S = 1	23.94	54.72

3.3. Response Time

The response speed of the PD is a measurement of the time required for the accumulated charge to become an external current and is generally expressed as the rise(fall) time or cut-off frequency. The rise time and fall time of a photodiode is defined as the time for the signal to rise or fall from 10% to 90% or 90% to 10% of the final value respectively [22].

To understand the response speed, the device structure was analyzed. The response speed of the built-in photodiode is controlled by the following three factors:

T_{RC}: T_{RC} is determined by the C and the R, where R is the sum of the series resistance and the load resistance (R_S + R_L). C is the sum of the package capacitance and the photodiode junction capacitance. TRC is given by:

$$T_{RC} = 2.2RC = 2.2 \times C \times (R_s + R_L) \tag{3}$$

$T_{diffusion}$: Carriers may generate outside the depletion layer when incident light misses the PN junction and is absorbed by the surrounding area of the photodiode chip and the substrate section which is below the depletion area [23]. The $T_{diffusion}$ required for these carriers to diffuse may sometimes be greater than several microseconds.

T_{drift}:The transit speed v_d at which the carriers travel in the depletion layer is expressed using the travelling rate μ and the electric field E developed in the depletion layer, as in v_d = μ*E. If the depletion layer width is d and the applied voltage is V_R, the average electric field E = V_R/d, and thus T_{drift} can be approximated as follows:

$$T_{drift} = d / vd = d^2 / (\mu V_R) \tag{4}$$

To achieve a fast response time for T_{drift}, the moving distance of carriers should be short and the reverse voltage should be larger. The rise time of the photodiode is T_r and it is determined by the above three factors. It is approximated by the following equation:

$$T_r = \sqrt{T_{drift}^2 + T_{diffused}^2 + T_{RC}^2} \tag{5}$$

The N_{well}/P_{sub} PD is designed for fewer carriers generated outside the depletion layer, C_t is small and the carrier transit time in the depletion layer is short. Therefore, these types are ideally suited for high-speed light detection. To decrease the response time of the photodiode, each of the factors mentioned above should be as small as possible.

4. Simulation and Test Results

4.1. Simulation Results

In order to simulate the design results, simulation is divided into two cases for the response time. The first case, when the photocurrent is constant, simulates the relationship about the environmental temperature and the response time. The simulation condition is set to V_{DD} = 30V, I_{ph} = 20uA, the temperature T = -25℃~125℃. The frequency of the square wave signal is 10 kHz and the duty cycle is 50%.

From the typical case, the response time can be simulated in two cases. One is from the photon incident to the TIA module (T_{P1}) and the other is from the input port to the output port (T_{P2}). Where the LH indicates the delay time of the signal change from low-to-high and the HL represents the delay time of the signal change from high-to-low. The simulated data is showed in Table 2.

Table 2. Response Time with Temperature Variations

T(°C)	T_{PLH1}	T_{PHL1}	T_{PLH2}	T_{PHL2}
-25	6.5ns	38.4ns	203.1ns	157.2ns
25	7.6ns	41.5ns	205.5ns	155.0ns
75	8.0ns	40.2ns	204.2ns	157.8ns
100	7.5ns	38.7ns	205.9ns	151.1ns
125	8.50ns	33.5ns	208.9ns	156.8ns

In the second case, when the temperature is 25℃, I_{ph} changed from 5uA to 80uA, simulated the influence of the current on T_{PLH1} and T_{PLH2}. The specific data is showed in Table 3.

Table 3. Response Time with Photocurrent Changes

I_{ph}(uA)	T_{PLH1}	T_{PHL1}	T_{PLH2}	T_{PHL2}
5	9.9ns	34.7ns	205.2ns	157.9ns
10	9.54ns	39.9ns	204.4ns	150.1ns
20	9.6ns	41.5ns	205.5ns	153.0ns
40	9.8ns	42.7ns	208.1ns	155.1ns
80	9.2ns	43.5ns	204.1ns	157.2ns

From the simulation data, the response time of the PD model is very short. The PD model has the very good temperature coefficient and the response time could not change with the temperature varied.

4.2. Test Results

To test the performance of the whole chip in the practical applications, the response time of the chip at 840nm wavelength was measured. The typical condition of the measurement is the working voltage VDD = 30V, T = 25℃ and R_L = 50Ω .

According with the formula 2, when the I_{in} = 12.2mA, then the I_{ph} = 20uA. The response time from the input to the output, that is to say, the response speed of the entire chip is showed in Figure 6 and Figure 7.

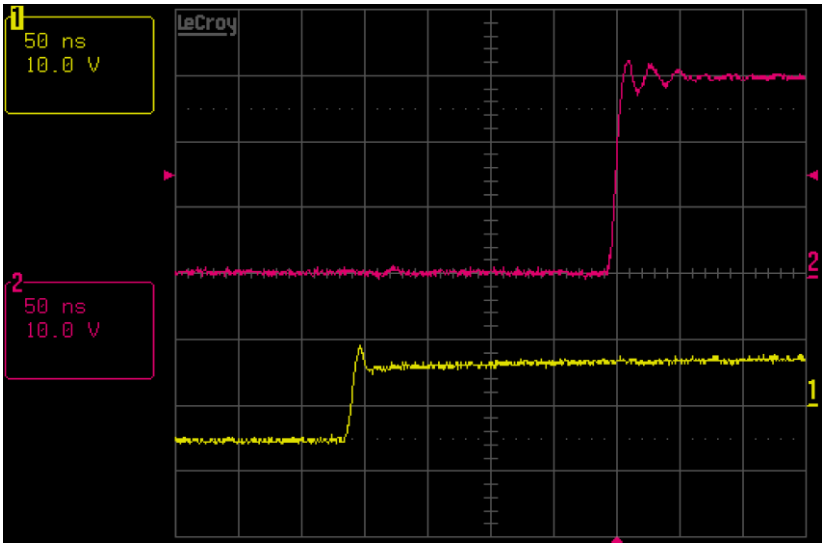

Figure 6. T = 25℃, I_{ph} = 20uA the T_{PLH} of the Whole Chip

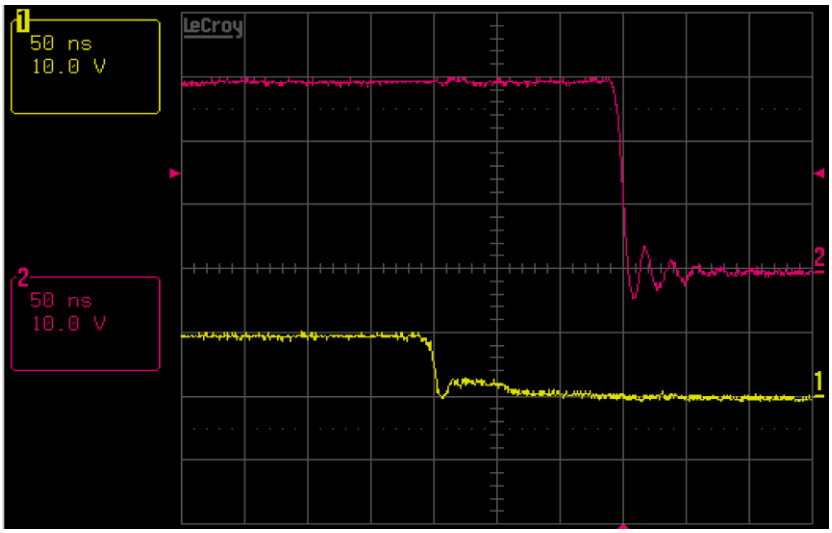

Figure 7. T = 25℃, I_{ph} = 20uA, the T_{PHL} of the Whole Chip

In the above two figures, the yellow line represents to the input photocurrent. The red line indicates the output signal. From the test results, the response speed of the whole chip is so quickly and the T_{PLH} = 205ns, T_{PHL} = 155ns.

When the temperature varied from 25℃ to 125℃ and the I_{ph} kept constant, the response time of the whole chip would not changed dramatically. Choose T=125℃ and I_{ph} kept 20uA, test results of the T_{PLH} and T_{PHL} is in Figure 8 and Figure 9.

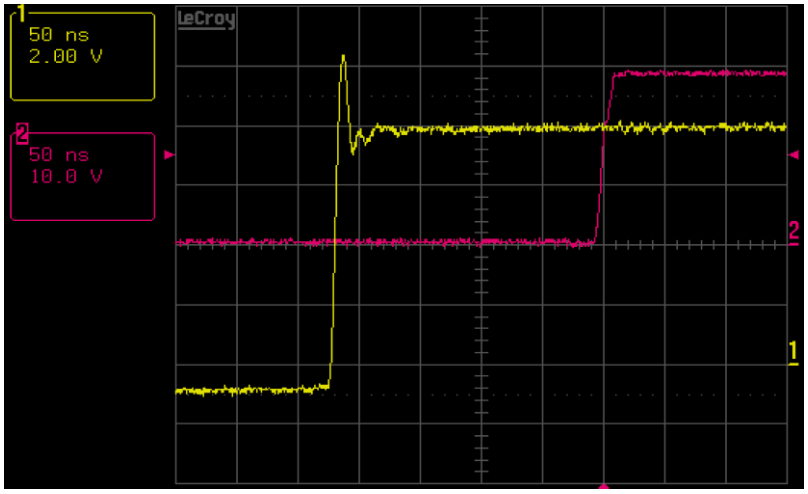

Figure 8. T = 125℃, I_{ph} = 20uA, the T_{PLH} of the Whole Chip

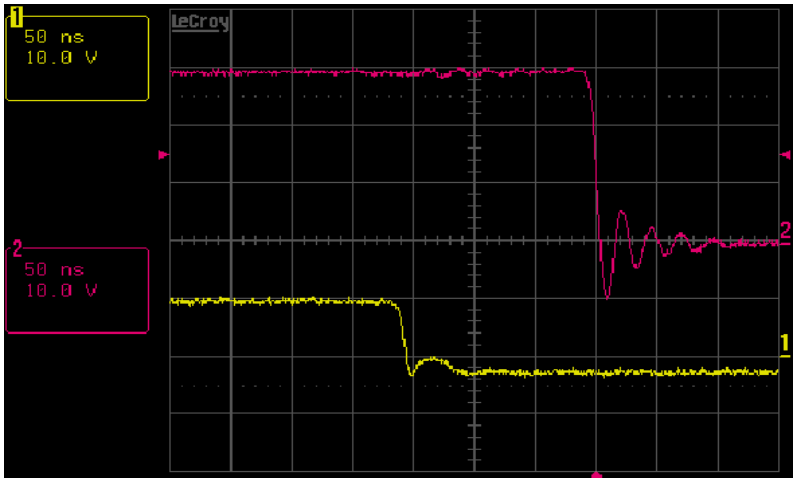

Figure 9. T = 125℃, I_{ph} = 20uA, the T_{PHL} of the Whole Chip

From the comparison of the simulation and the measurements, the response time in the PD is shorter than the designing. The response speed of the whole chip is more quickly than before. Based on the analysis of the PD model and the TIA circuit, the simulation data and test waveform is basically consistent with good test results.

5. Conclusions

This paper fabricates a novel optocoupler in order to solve the problem of the response speed in industry field. Based on 0.35umBCD technology to design and manufacture a monolithic integrated the 840nm optical receiver chip, which contains N_{well}/P_{sub} structure of PD and TIA circuit analysis. It is verified that, the whole chip simulation as well as the measurements indicates the faster response time greatly. The data meets the current equation in the equilibrium matter and the output signal is well. That is to say the entire loop of the whole chip works well.

Acknowledgements

This work was supported by the National Natural Science Foundation (No. 61106026) of China, the Key Lab of High-Speed Circuit Design and EMC Foundation (No. JY0100092702) and the Shaanxi Province Science Foundation (No. 2013JM5002).

References

[1] S. Kaeriyama, S. Uchida, M. Furumiya and M. Okada, IEEE Journal of Solid-State Circuits, vol. 47, no. 2, **(2012)**.
[2] M. Yamamoto, M. Kubo and K. Nakao, "Electron Devices", vol. 42, no. 1, **(1995)**.
[3] H. Zhu, L. Mao, C. Yu and H Chen, "Design and fabrication of a low crosstalk multi-channel CMOS OEIC receiver module", International Society for Optics and Photonics, 68380B-68380B-7; Beijing, China, **(2007)** January.
[4] S. Radovanovic, A. Anuema and B. Nauta, "Microelectronics Reliability", vol. 9, no. 11, **(2004)**.
[5] Yan,Yao, Hsiang-Yu, Chen, Jinsong Huang and Yang Yang, Applied Physics Letters . 90, 5(2007)
[6] C. Caillaud, G. Glastre, F. Lelarge, R. Brenot, S. Bellini, J. F. Paret, O. Drisse, D. Carpentier and M. Achouche, IEEE Photonics Technology Letters, vol. 24, no. 11, **(2012)**.
[7] C. Rooman, D. Coppee and M. Kuijk, IEEE Journal of Solid-State Circuits, vol. 35, no. 7, **(2000)**.
[8] P. Kostov, W. Gaberl and H. Zimmermann, "High-speed PNP PIN Phototransistors in a 0.18 μm CMOS Process", Proceedings of the European Solid-State Device Research Conference,; Helsinki, European, **(2011)** September 187-190.
[9] Z. Haobo, M. Luhong, Y. Changliang and M. Liyuan, "Chinese Journal of Semiconductors", vol. 28, no. 5, **(2007)**.
[10] Y. Changliang, M. Luhong, S. Ruiliang, Z. Haobo, W. Rui and W. Qian, Chinese Journal of Semiconductors, vol. 28, no. 8, **(2007)**.
[11] X. Xindong, Z. Shilin, M. Luhong, X. Sheng and C. Yan, Science China Press, vol. 56, no. 21, **(2011)**.
[12] Q. Chen, D. Chitnis, K. Walls and T. D. Drysdale, IEEE Photonics Technology Letters, vol. 24, no. 3, **(2012)**.
[13] P. Aubert, H. J. Oguey and R. Vuilleumier, "Solid-State Circuits", vol. 23, no. 2, **(1988)**.
[14] H. Cui, Z. Tang, Y. Fang, J. Liu and C. Yang, Journal of Computational Information Systems, vol. 7, no. 1, **(2011)**.
[15] F. Tavernier and M. Steyaert, "A 5.5 Gbit/s Optical Receiver in 130 nm CMOS with Speed-Enhanced Integrated Photodiode", Proceedings of the IEEE, Seville, Spanish, **(2010)** September 542-545.
[16] L. de Abreu Faria, C. Alberto dos Reis Filho, F. Durante Pereira Alves and R. d'Amore, "Analog Integr Circ Sig Process", vol. 73, **(2012)**.
[17] H. Cui, Z. Tang, Y. Fang, J. Liu and C. Yang, Journal of Computational Information Systems, vol. 6, no. 9, **(2010)**.
[18] X. Fan, Y. Huang, X. Duan, Q. Liu, X. Ren, Q. Wang, F. Hu, S. Cai and X. Zhang, "Optics Communications", vol. 2, no. 16, **(2013)**.
[19] C. Zhang, S. Wang, L. Yang, Y. Liu, T. Xu, Z. Ning, A. Zak, Z. Zhang, R. Tenne and Q. Chen, Appl. Phys. Lett., vol. 100, no. 243101, **(2012)**.
[20] S. Hao, Huang and W. Z. Chen, "CMOS Optical Receiver with Integrated Photo Detector for High-Speed Interconnects", 10th IEEE International Conference on Solid-State and Integrated Circuit Technology, Shanghai, China, **(2010)** November 188-191.
[21] X.-W. Fu, Z.-M. Liao, Y.-B. Zhou, H.-C. Wu, Y.-Q. Bie, J. Xu and D.-P. Yu, Appl. Phys. Lett., vol. 100, no. 223114, **(2012)**.
[22] C. S. Liang Pei, L. S. Lai and Y. T. Tseng, IEEE Electron Device Letters, vol. 24, no. 10, **(2003)**.
[23] I. Pei, C. S. Liang, L. S. Lai, Y. T. Tseng, Y. M. Hsu, P. S. Chen, S. C. Lu, M.-J. Tsai and C. W. Liu, IEEE Electron Device Letters, vol. 24, no. 10, **(2003)**.

Author

Lei Tian, received Bachelor of Communication Engineering from Xi'an University of Science and Technology, Xi'an, China in 2001. I received the Master of Mobile Communication degree in Xi'an University of Science and Technology (XUST), in 2006. Then I joined as a lecturer in the Department of Electronic Engineering, Xi'an University of Posts and Telecommunications. In 2010, I joined in Xidian University to get the Ph.D in Optoelectronic Integrated Circuit Design (OEIC). As a member of IEICE, my research interest includes Analog and mixed integrated circuits, Photoelectric signal processing, Optocoupler, SOC Design, Infrared communications.

