

## The Design of a Multi-bit Quantization Sigma-delta Modulator

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### Abstract

*Sigma-delta ACD has two main parts: analog modulator and digital filter, the performance of modulator determines the performance of sigma-delta ADC, so the design of modulator is very important. The paper introduces the principle of sigma-delta AD modulator with high accuracy and the applied over sampling technique, noise shaping technique and multi-bit quantizer technique. Determining the design scheme of modulator—three bits three orders CIFF(Cascade of integrators, feed forward form) structure, and it makes the behavior level verification for this scheme by Simulink tool in MATLAB. The simulation result shows that multi-bit quantizer modulator can get very high SNR, and based on this result it designs every part of the modulator circuit.*

**Keywords:** *Sigma-delta ADC; modulator; over sampling; noise shaping; multi-bit quantization*

### 1. Introduction

ADC (Analog to Digital Converter) is the bridge linking the analog world and the digital world, it can convert the analog signal to the digital signal, and benefits to the storage, processing and transmission of the data [1]. With the development of electronic technique, ADC has much wider application, the requirements of data conversion accuracy is much higher, for example, in high fidelity system, it puts forward the very high requirement to ADC, namely, the resolution of A/D converter must be more than 16-bit. However, when adopting the traditional A/D converter, such as parallel comparison A/D converter, double integral A/D converter and successive approximation A/D converter, they can't gain very high accuracy[2-3].

Oversampling sigma-delta modulation method is one superior way to get the high accuracy converter, this method adopts the over sampling technique and the noise shaping technique of sigma-delta modulator, so it will perform dual suppression for quantization noise in signal frequency band. Finally the down sampling will be performed by the digital decimation filtering. Comparing with other converters with the different structure, sigma-delta ADC has many advantages, such as high accuracy, high linearity and large dynamic range and so on [4].

According to the digit capacity of quantizer in modulator, sigma-delta is classified as 1-bit quantization and multi-bit quantization. The current low order and single-bit ADC is limited by the order of modulator and single-bit quantization, which decreases the possibility to get the higher SNR. With the wider application of sigma-delta ADC, the requirements to it become higher. The SNR is the uppermost parameter to measure performance, and it can be improved largely by changing the modulator order, over sampling rate and quantization bits. Even though increasing the modulator order can

largely improve the SNR, the attendant problems have emerged, such as the stability and complexity of circuit, and so on [5]. These problems are also serious in low voltage and low power circuits at present. Therefore, the multi-bit sigma-delta modulator will be the market mainstream because of the performance advantage and wide application prospect [6].

## 2. The Theoretical Foundation of Sigma-delta Modulator

### 2.1. The Basic Principle of Sigma-delta Modulator

Figure 1 is the function block diagram of sigma-delta modulator.  $V_{in}$  is the analog input voltage.  $V_{ref}$  is the reference voltage of one bit DAC, so  $V_{ref}$  must be equal to or more than the analog input voltage. At  $NT$  moment, in the adder,  $V_{in}$  minus  $R(NT)$  can get error voltage  $V(NT)$ , this error voltage can be performed low-pass filtering by the integrator. By  $T$  moment delay, the output voltage is  $W[(N+1)T]$  at  $(N+1)T$  moment, then  $Y[(N+1)]$  can be got by the comparer. When  $W[(N+1)T] \geq 0$ , the comparer output is "1", then passing the one bit DAC, it can get  $R[(N+1)T] = +V_{ref}$ ; When  $W[(N+1)T] < 0$ , the comparer output is "0", then passing the one bit DAC, it can get  $R[(N+1)T] = -V_{ref}$ . The working process of sigma-delta modulator is as followed, at  $(N-1)Y$  moment,  $W$  is assigned the initial value  $W[(N-1)T]$ , then it can get  $Y[(N-1)T]$ ,  $R[(N-1)T]$  and  $V[(N-1)T]$ . At  $NT$  moment,  $W(NT) = V[(N-1)T] + W[(N-1)T]$ ,  $Y(NT)$  and  $R(NT)$  can be obtained, thus  $V(NT) = V_{in} - R(NT)$ . With the sampling time lasting, it can obtain  $Y(NT), Y[(N+1)T], \dots, Y[(N+K)T]$  series datum flow, this datum flow can get the data output of ADC by the digital filter. It is assumed that the analog input is sine signal, when the sine signal is wave crest, the mass output is "1"; when it is wave hollow, the mass output is "0"; when the change of sine signal is the steepest, the "1" and "0" in output data is equal. The statistic value of  $Y$  datum flow reflects the size of analog input  $V_{in}$  [7].

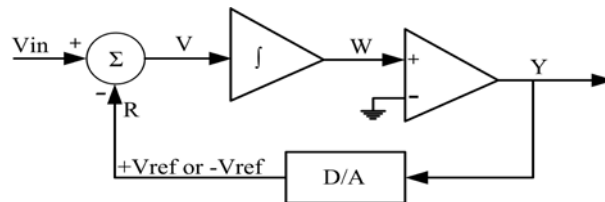


Figure 1. The Schematic of Sigma-delta Modulator

### 2.2. The Key Technique of Sigma-Delta Modulator

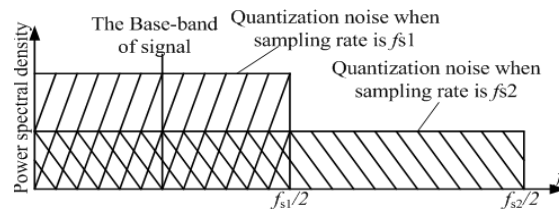
The differences between sigma-delta ADC and general Nyquist converter are that the former adopts the over-sampling and noise shaping technique. Based on these two techniques, the paper designs a high performance sigma-delta ADC modulator. The key techniques are as followed.

**2.2.1. Over-sampling Technique:** The oversampling is sampling the analog signal whose frequency is much higher than Nyquist sampling frequency. To avoiding the aliasing phenomenon, so the over sampling frequency must be much higher Nyquist sampling frequency. The over sampling frequency (usually between 8 to 512) is defined as the ratio of sampling frequency and Nyquist frequency [8]. It is shown in formula (1).

$$OSR = \frac{f_s}{2f_b} \quad (1)$$

In formula (1),  $f_s$ —the system sampling frequency  
 $f_b$ —the signal band

The oversampling technique has two marked characteristic. First, because the signal band  $f_b$  is less than the half of sampling frequency. When compared with Nyquist sampling frequency, the frequency spectrum image produced in sampling process is more dispersed. In the signal band, the frequency of input signal in  $[f_b, f_s - f_b]$  will appear the aliasing phenomenon. Therefore, for the anti-aliasing filter, the change between pass band and forbid band is easier, the design will be simplified largely [9]. Second, over sampling technique can increase signal quantization to noise ratio (SQNR). According to the signal sampling quantization theory, if the smallest amplitude of the input signal is greater than the quantization step  $\Delta$ , and the amplitude distributes randomly, then the total power of quantization noise is a constant, and it has nothing to do with sampling frequency  $f_s$ , in addition, it distributes uniformly in  $0 \sim f_s/2$ . Therefore, the quantization noise level is inversely proportional to the sampling frequency, and increasing the sampling frequency can reduce the quantization noise level, while the base-band is constant. So it reduces the noise function in the base-band to improve the SNR. Figure 1 shows the distribution of quantization noise at different frequency, and it clearly describes the relationship between sampling frequency and noise level. Here,  $f_{s2}$  is far greater than  $f_{s1}$ , so  $f_{s2}$  quantization noise power is much smaller than  $f_{s1}$ 's in the base-band [10].



**Figure 2. Quantization Noise Distribution in Different Sampling Frequency**

**2.2.2. Noise Shaping Technique:** Treating the quantization error can reduce the quantization noise in signal frequency band. The noise shaping technique improves the converting accuracy when analog converting to data. It is assumed that the oversampling input signal has N-bit quantizer, if the oversampling ratio is enough large, then the change of signal is very small in two neighbored sampling process. The quantization noise is alike in the low frequency, the change always appears in the high frequency. So the quantization noise can be decreased in the low frequency band by the method that two successive sampling values subtract. Formula (2) is the principle of one order noise shaping.

$$e_{HP}(n) = e(n) - e(n-1) \quad (2)$$

The quantizer noise in frequency band can be further reduced by more number of times sampling values subtract to achieve the high order noise shaping. For example, formula (3) is the principle of two orders noise shaping. Formula (4) is the principle of three orders noise shaping. According to this principle, it can continue to derive infinitely to get the higher noise shaping [11].

$$e_{HP,2}(n) = e(n) - 2e(n-1) + e(n-2) \quad (3)$$

$$e_{HP,3}(n) = e(n) - 3e(n-1) + 3e(n-2) - e(n-3) \quad (4)$$

In the formula,  $e(n)$ —the quantization noise from the  $n$ -th sampling.

The above processing procedure can be described as formula (5) by the centralized way in  $z$  domain.

$$E_{HP,L}(z) = (1 - z^{-1})^L E(z) \quad (5)$$

This procedure means to make the filtration to the customary noise. So the transfer function of filter, named noise shaping function, can be presented as formula (6).

$$NTF(z) = (1 - z^{-1})^L \quad (6)$$

In the formula,  $L$ —the order of noise shaping.

For the above noise transfer function, its amplitude is shown in formula (7).

$$|NTF_Q(z)| = |1 - e^{-j2\pi f T_s}|^L = (2 \sin \pi f T_s)^L \quad (7)$$

In the signal band ( $f \leq f_b$ ), if the oversampling ratio is very large, so the amplitude of transfer function will be very small in this range, in this band the quantization noise power spectral density is shown in formula (8).

$$P_Q = \int_{-f_b}^{f_b} \frac{\Delta^2}{12 f_s} |NTF(f)|^2 df \approx \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}} \quad (8)$$

Under the ideal conditions, the dynamic range can be got by the AD converter that has been applied to the oversampling technique and noise shaping technique, and it is shown in formula (9).

$$DR \approx \frac{3}{2} 2^{2N} \frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}} \quad (9)$$

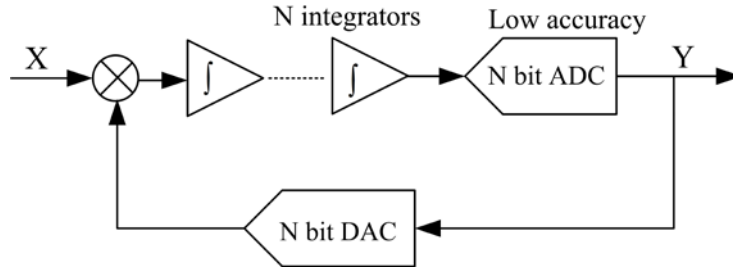
The above formula presented by the decibel will be shown in formula (10).

$$DR \approx 6.02N + 1.76 + 10 \log_{10} \left( \frac{2L+1}{\pi^{2L}} \right) + (2L+1) 10 \log_{10}(OSR) \quad (10)$$

By observing the above formula, when the  $L$  orders noise shaping technique combining with the oversampling technique apply to the converter, its dynamic range increases  $(L+0.5)$  bit. For example, if adopting one order noise shaping, the number of significant digit increases from 0.5 bit to 1.5 bit [12].

**2.2.3. Multi-bit Quantizer Technique:** To improve the single sigma-delta modulator performance largely, the multiple bits quantizer technique is needed. Sigma-delta modulator with multi-bit quantization structure can increase the convert rate and the resolution of ADC, and it consists of an  $N$ -bit parallel ADC and an  $N$ -bit DAC. Compared with the single bit quantization modulator, the multi-bit one has many advantages when the conditions are same: it has a bigger stable region, a larger input dynamic range, a higher resolution [13], in addition, it has a higher linearity. Quantizer is the only nonlinear component in Sigma-delta modulator, but multi-bit quantizer has the good stability and the high linearity, so its

performance is close to the linear system [14]. Figure 3 shows the system chart of multi-bit quantization sigma-delta modulator, the output signal Y returns to input port by N-bit DAC.



**Figure 3. The System Chart of Multi-bit Quantization Sigma-delta Modulator**

In sigma-delta modulator circuit, the structure of single bit quantizer is simple. It just needs one comparator and the DAC in the feedback circuit with the stable linearity. However, single bit quantizer has the large quantization noise, and needs the higher OSR to suppress it. Using the single bit quantizer in high order single circuit modulator will make the system become instable. As for the multi-bit quantization, it has higher conversion accuracy, reduces the quantization noise, eliminates the relativity between modulation process and input signal effectively, and enhances the stability of system. While, multi-bit quantization needs adding a multi-bit DAC to the feedback circuit to produce the feedback signal, which will lead into the nonlinear problem and affect the system's performance, so the calibration is necessary. The quantization SNR of an L-order and M-bit sigma-delta modulator is as followed [15].

$$\begin{aligned}
 SQNR &= 10\log_{10}\left(\frac{P_s}{P_q}\right) = 10\log_{10}\left(\frac{3}{2}2^{2N}\right) \\
 &+ 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}OSR^{2L+1}\right) \\
 &+ 10\log\left[2^M - 1\right]^2
 \end{aligned} \tag{11}$$

Here, M presents the digit of quantizer. The relationship between the digit and SNR is shown in Table 1.

**Table 1. Relationship between the Bit of Quantizer and SNR**

The Bit of Quantizer	The SNR Increment	The Increment of SNR When Quantizer Increases One Bit
2	9.5	9.5
3	17	7.5
4	23.5	6.5
5	29.8	6.3
6	35.9	6.2

From Table I, we can see that increasing the digit of quantizer can increase SNR quickly. When the digit of quantizer is more than 5, the quantization accuracy in feedback circuit becomes double, and the increment of SNR is about 6 dB [9].

### 3. Design of Multi-bit Quantization Sigma-delta Modulator

Sigma-delta modulator is the core part of sigma-delta ADC, and it is composed of the difference summation unit, integrator, quantizer and a DAC. The paper designs a sigma-delta modulator with 24 significant digits, uses Simulink toolbox fully in MATLAB to model the

multi-bit quantization sigma-delta modulator, gets its topological structure, and finally designs each module circuit of modulator by using simple components.

### 3.1. Sigma-delta Modulator Modeling

To improve design efficiency and reduce design period, it must adopt one fast and flexible circuit simulation scheme with high accuracy to design the high accuracy Sigma-delta modulator. Meanwhile, it must make the circuit structure adjustment and parameters optimization to get the high resolution and large dynamic range. The design adopts single circuit three orders CIFF circuit, and the ideal model of multi-bit quantization sigma-delta modulator is established by Simulink in MATLAB. It is shown in Figure 4.

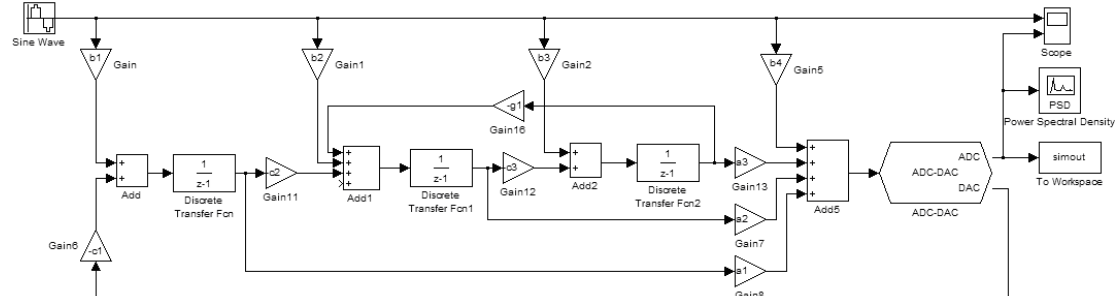


Figure 4. Multi-bit quantization Sigma-delta Modulator's Ideal Model

### 3.2. Sigma-delta Modulator Circuit Design

Sigma-delta modulator includes integrator, quantizer and DAC. The paper designs a low cost and high performance sigma-delta modulator through simple discrete device. It adopts 3-bit quantizer and feedback DAC. Compared with others, they can be achieved easily and their cost is low. The each part circuit is as followed.

**3.2.1. Integrator Design:** The integrator is the core circuit module of sigma-delta modulator. Here we adopt the switched capacitor integrator, which consists of the switch, sampling integrating capacitor and operational amplifier. Figure 5 describes the three stages integrator with switched capacitor. A voltage follower between input port and first stage integrator is designed to lead into the negative feedback with voltage series. The input impedance of voltage follower is high, while the output impedance is low, so it can achieve the impedance match and isolation between former and latter stages.

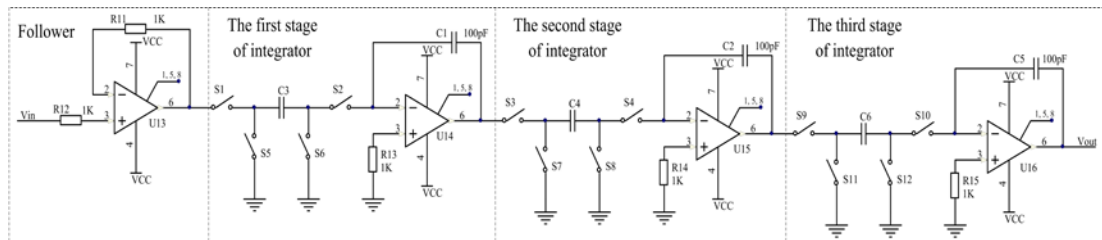
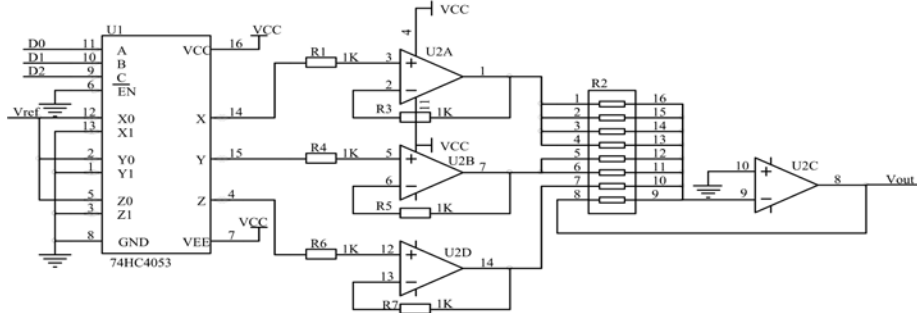


Figure 5. Three Orders Paralleled Integrator

**3.2.2. DAC Design:** The output of quantizer gets to the first integrator through the feedback of DAC. The feedback loop can make the input port of the first integrator tend to zero, namely, the input value of modulator is equal to the average value of DAC's output. In this

paper, we use 3-bit feedback ADC, which is composed of multiple switch 74HC4053, operational amplifier, and exclusions. Due to the low cost and fast speed of multiple switch, and similar performance in exclusion, they are appropriate to used as feedback ADC whose accuracy is very high. Its structure is shown in Figure 6.



**Figure 6. Feedback ADC**

**3.2.3. Quantizer Design:** The quantizer is a 3-bit successive approximation ADC, and is composed of a comparator, D/A converters, buffer registers and control logic circuits. The structure of D/A converter is shown in Figure 6, and the control logic of it is realized in FPGA. The basic principle is that, comparing levels from high bit to low bit, as if using balance to weigh objects, we should increase or decrease weights step by step from heavy to light. The process of successive approximation conversion is as follows: clear every bit in the register when initializing, and the supreme bit will be set “1” and be sent into D/A convert at the beginning of conversion. The output of D/A convert is analog, *i.e.*,  $V_o$ . Then compare it with  $V_i$ , which is also an analog signal waiting to be converted. If  $V_o < V_i$ , the 1 in this bit is kept, otherwise it will be cleared. Then the second high bit will be set “1” and be sent into D/A convert,  $V_o$  compares with  $V_i$ , If  $V_o < V_i$ , the 1 in this bit is kept, otherwise it will be cleared. Repeat this process until the lowest bit of the successive approximation register. After the transformation, send every digital quantity into the buffer register, and get the digital output. All these processes are controlled by a circuit. Because the 3-bit successive approximation ADC can be achieved by sample discrete components, and doesn’t need photolithographic process, thus it has low cost and high convert rate.

#### 4. Simulation Experiment Result

At different over-sampling rates, we simulate the proposed modulator which has a monocyclic third-order CIFF structure with 3-bit quantization, and the simulation results are shown in Table 2.

**Table 2. Relationship between Over-sample Rate and Module Performance**

Over Sampling Rate	SNR	Number of Significant Bit
16	82.0	13.32
32	102.5	16.74
64	123.7	20.25
128	144.9	23.70
256	169.1	27.79
512	189.9	31.26

From the Table 2, we can see that, when the number of order and bits of quantization in the modulator are determined, increasing the sampling rate can obviously improve the modulator performance.

Thus, making full use of the high speed and data processing ability of FPGA, it is easy to realize high over-sampling rate and sigma delta ADC with high performance.

The paper simulates the 3-bit quantization sigma-delta modulator under the conditions that the over-sampling rate is 256. Here we use the Simulink toolbox in MATLAB. Figure 7 shows the input wave and output wave of modulator, the red line presents the input wave, and the blue line is output wave. Figure 8 shows the performance of multi-bit quantization modulator model while Figure 9 shows the performance of modulator model with 1-bit quantization.

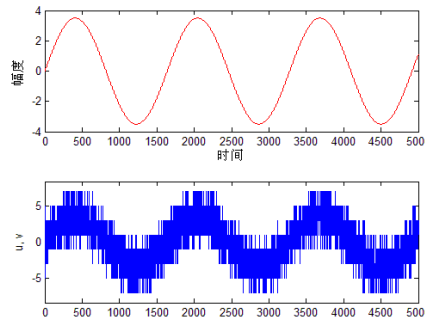


Figure 7. The Input and Output Wave of Modulator

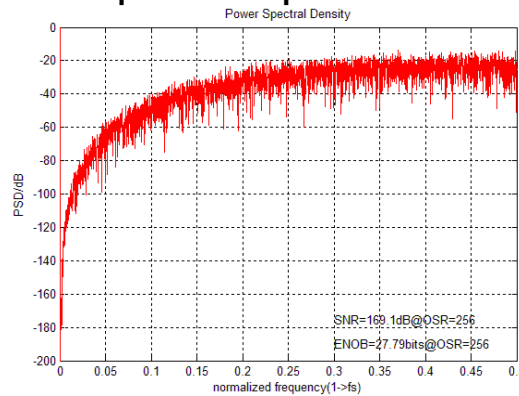


Figure 8. The Performance of Multi-bit Quantization Modulator Model

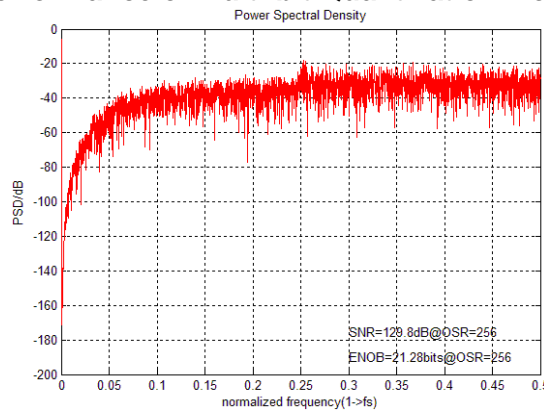


Figure 9. The Performance of Multi-bit Quantization Modulator Model



The simulation results show that, the wave groove in Figure 7 is wider than it in Figure 8, and the SNR is evidently higher than it by one bit quantization. When sampling rate is 256, the resolution of 3-order 3-bit quantization sigma delta modulator is 27.79 bits when the SNR is 169.1dB, while the resolution of 1-bit quantization sigma-delta modulator is 21.28 bits when SNR is 129.8 dB.

## 5. Conclusion

The paper studies the sigma-delta modulator and analyzes the modulator principle. It introduces the key technology, the modeling and simulation for sigma-delta modulator will be made by Simulink tool in MATLAB. The simulation result shows that multi-bit quantizer can get the high SNR (signal to noise ratio). Meanwhile, it designs every part circuit of modulator by the discrete components, so it gets the smart multi-bit sigma-delta modulator with the simple circuit. This modulator uniting the digital decimation filter by FPGA can achieve the sigma-delta ADC with high accuracy

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