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Impact of Various Parameters on Power Consumption of CMOS Logic Circuits

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Abstract

System level issues such as battery life, size and weight are directly affected by power dissipation. To improve the performance and capability of systems, reduction of power dissipation is necessary. Power Dissipation in conventional Complementary Metal Oxide Semiconductor (CMOS) circuits can be minimized using adiabatic technique because power dissipation is the primary concern in commercial applications. Using adiabatic technique, minimization of power dissipation is achieved and some of energy stored in load capacitance can be recycled instead of heat dissipation. Adiabatic technique is highly dependent on parameter variations. Various digital circuits have been designed & simulated in TANNER TOOLS using 180nm technology. In this paper, comparison of Efficient charge recovery logic (ECRL) and Positive feedback adiabatic logic (PFAL)are done with conventional CMOS technique and it has been analyzed that circuit designed with PFAL adiabatic technique consumes less power. Circuits designed with adiabatic technique are used in signal processing & biomedical applications due to its reduced dynamic power.

Keywords*: Adiabatic Switching, ECRL, PFAL, Equivalent model*

1. Introduction

In VLSI technology, the term Adiabatic is the thermodynamic process in which no heat is exchange with environment, and there is no dissipated energy loss. To increase the functionality of portable devices, lot of power is required for longer batteries. The size of the battery increases with the increasing the demand of portable devices. Nowadays, various techniques have been developed and adiabatic technique is one of them which are also called reversible logic technique [1]. In conventional CMOS circuits, with the help of reducing supply voltage, node capacitance and switching frequency, power consumption can be minimized but recently adiabatic technique has been implemented very successfully in low power systems [2].

Adiabatic switching is also called energy recovery technique which is used for implementing the Low Power Array Architecture. Its large hardware complexity does not allow efficient implementation. The hardware complexity can be reduced by using reversible pipelining system. Due to the inherent property of this pipelining system, the reverse logic blocks are used at different time instances. The reversible operation can be achieved with small hardware cost by using multiplexer and clocking strategy [3]. In this paper, a CMOS inverter and CMOS 2:1 MUX with conventional CMOS and Adiabatic technique has been designed, simulated in Tanner Tools and compared with each other. In conventional CMOS logic circuit the transition from 0 to VDD of output node, the output energy CL. VDD2is drawn from power supply. At the end of transition only

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1/2C_L.VDD2energy is stored at load capacitance. The half of drawn energy from power supply is dissipated in PMOS network (M2). From VDD to 0 transition of output, energy stored in NMOS network is dissipated by NMOS network(M1). Adiabatic logic circuit reduces the power consumption during switching and reuses some of energy by recycling from output load Capacitance [4]

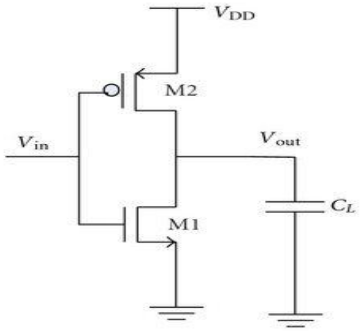

Figure 1. Schematic of CMOS Inverter

When input is low, PMOS is on and NMOS is off, hence direct path exist between power supply voltage and load capacitance. This is called charging phase[2].

$$E_{Charge} = \frac{1}{2} C_L VDD^2 \quad (1)$$

When input is high, PMOS is off and NMOS is on, hence there is no direct path exists between power supply voltage and load capacitance. This is called discharging phase [4].

$$E_{disCharge} = \frac{1}{2} C_L VDD^2 \quad (2)$$

The total amount of energy dissipated during charging & discharging phase is given by:

$$E_{TOTAL} = E_{Charge} + E_{disCharge} = C_L VDD^2 \quad (3)$$

2. Power Dissipation Mechanism in Adiabatic Logic Circuits

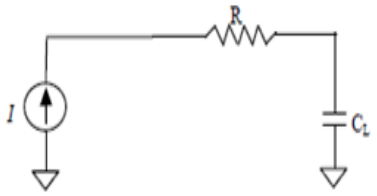

Figure 2. Equivalent Circuit Model

In the charging process, capacitor C_L is connected in series with resistor R and using constant current source for charging the load capacitance [5]. R is the resistance of PMOS and C_L is the load capacitor and T is the charging Time. The relation $Q=C_L V_{DD}$ is taken from the voltage source as energy source.

$$Ev_{DD} = Qv_{DD} = C_L v_{DD}^2 \quad (4)$$

Energy stored on capacitor at the voltage V_{DD} is equal to

$$E_C = {}^1/_{2C_L V_{DD}^2} \quad (5)$$

Energy dissipation of a switching event in static CMOS is given by:

$$E_{CMOS} = \alpha^{1}/_{2C_L V_{DD}^2} \quad (6)$$

Current into the circuit is given by:

$$i(t) = \frac{C_L dv(t)}{dt} = \frac{C_L vdd}{T} \quad (7)$$

Energy for a charging event is calculated by integrating the power p(t) during the transition time T:

$$E = \int_0^T p(t)\ dt = \int_0^T v(t).i(t)\ dt = \int_0^T (vR(t) + vc(t)).i(t)dt \quad (8)$$

Integral of vc(t).i(t) over one clock cycle will be zero as no energy is dissipated in the capacitance. Replacing the voltage source vR(t) in equation (5). With i(t).R and inserting eq. (7) in eq. (8).

$$E = \int_0^T R\frac{C^2 V_{DD}^2}{T^2}\ dt = \frac{RC}{T} Cv_{DD}^2 \quad (9)$$

Whole cycle consist of charging and recovering. As the same amount of energy dissipated in recover process. The overall dissipation in adiabatic logic (AL) is

$$E_{Al} = 2\frac{RC}{T}\ Cv_{DD}^2 \quad (10)$$

Since EDISS depend on R, so reducing the R of PMOS network energy dissipation can be minimized.

$$R = \left[\mu COX\frac{W}{L}(Vgs - Vth)\right]^{-1} \quad (11)$$

Where μ is the mobility, C_{OX} is the oxide capacitance, V_{GS} is the source voltage, V_{th} is the threshold voltage, W is the width and L is the channel Length. Adiabatic switching technique offers less energy dissipation in PMOS network and reuses the stored energy in load capacitance by reversing the current source direction.

3. Various Adiabatic Techniques

There are many adiabatic logic design techniques. But two of them are most widely used which are ECRL and PFAL which shows good improvement in energy dissipation and are mostly used as reference in new logic families for less energy dissipation.

3.1. Efficient Charge Recovery Logic (ECRL)

ECRL has two cross coupled PMOS and two NMOS transistors. The schematic and simulated waveform of ECRL inverter gate is shown in Figure 3 and Figure 4 respectively. Initially input in is high and inbar is low. When power clock (pclk) rises from 0 to VDD since P is on so output out remains at ground level. Output outbar follows the clock. When reaches at VDD, output out and outbar hold the logic zero and VDD respectively. This output value can be used for next stage as an input. Now power clock (pclk) falls from VDD to zero, outbar returns its energy to pclk hence delivered charge is recovered. The logic functions which are to be implemented both in true and complemented form.ECRL use the four phase clock rule to efficiently recover the charge to power clock.

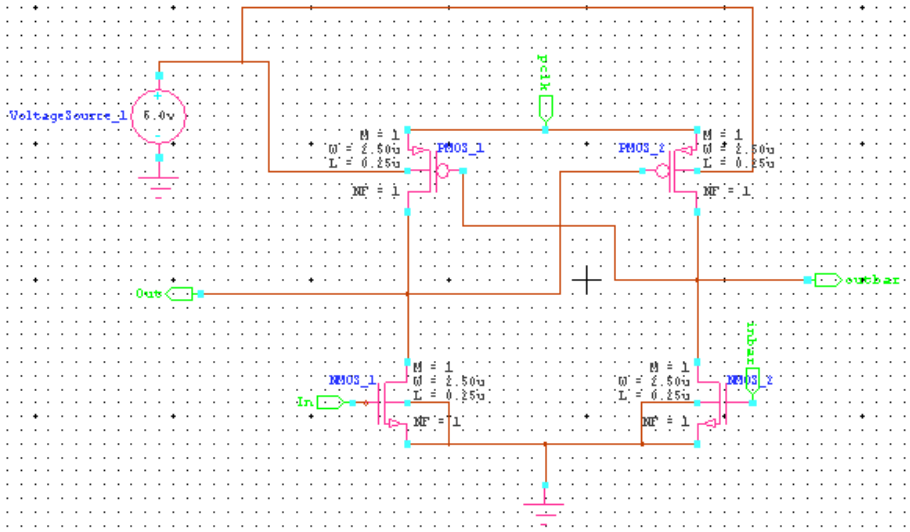

Figure 3. Schematic of ECRL Inverter

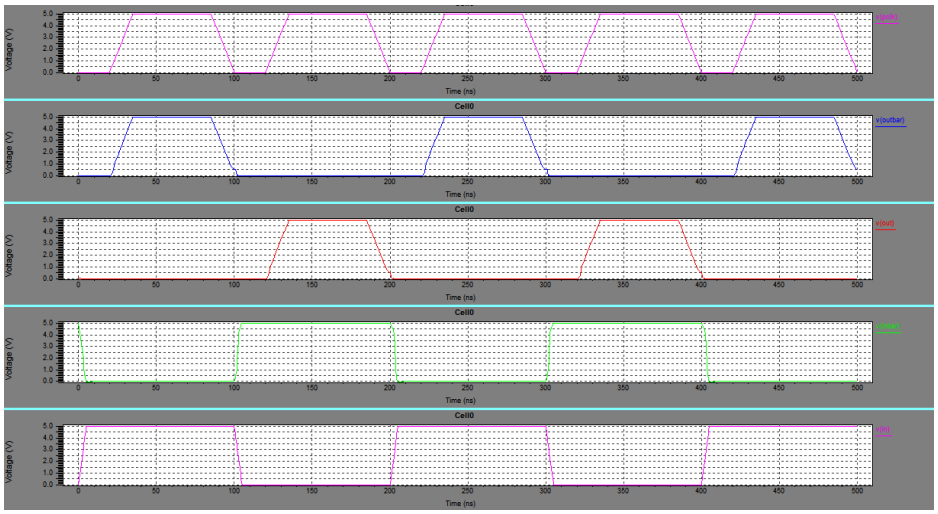

Figure 4. Simulated Waveform of ECRL Inverter

3.2. Positive Feedback Adiabatic Logic(PFAL)

PFAL has two cross coupled inverters connected as LATCH also called sense amplifier, which has two complimentary outputs and logic function. It has good lustiness against technological parameter variations. Latch is ignoring logic level degradation on the output nodes [3][6]. Initially input a is high and abar is low. When power clock p(clk) rises from 0 to VDDand since P and NMOS 4 are on, the outputout remains at ground level. Output 'outb' follow the clock. When reaches at V_{DD}, output 'out' and 'outb' hold logic zero and V_{DD} respectively. This output value can be used for next stage as an input. Now power clock (clk) falls from VDD to 0, 'outb' returns its energy to 'clk' hence delivered charge is recovered. PFAL use four phase clock technique to recover charge.

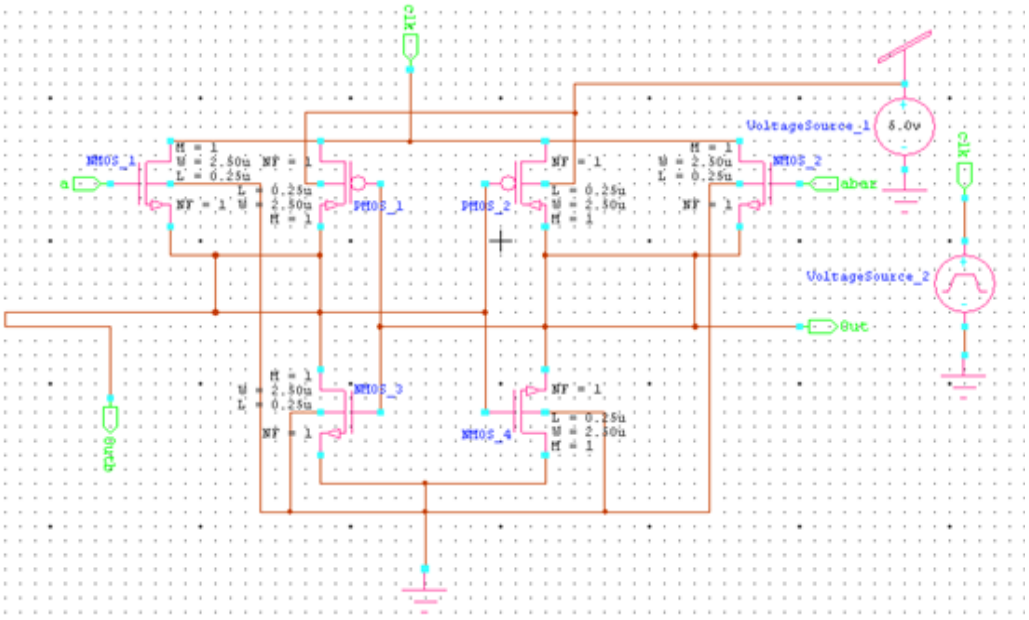

Figure 5. Schematic of PFAL Inverter

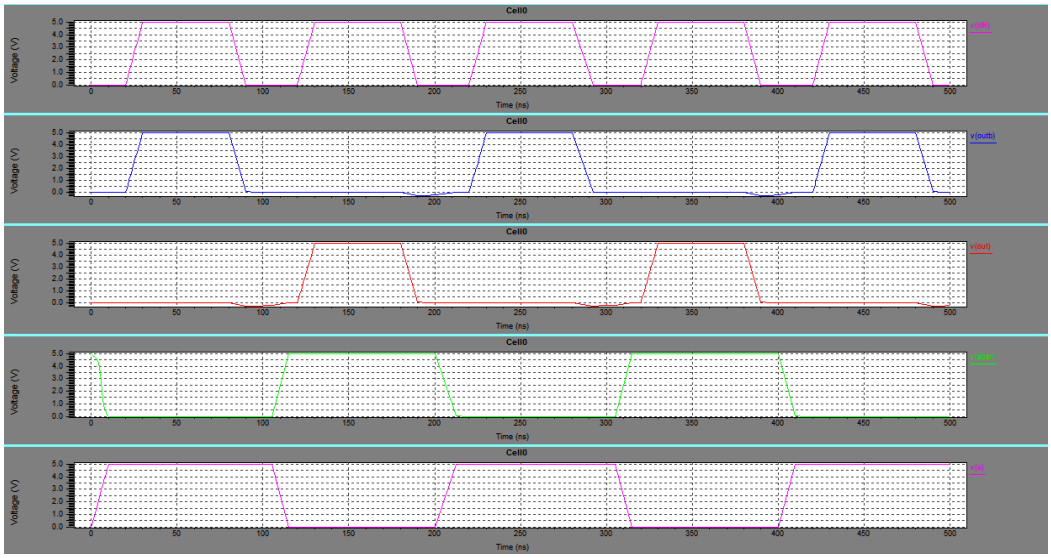

Figure 6. Simulated Waveform of PFAL Inverter

3.3. Multiplexer Using CMOS

A 2:1 multiplexer is a combination circuit that select one of the data input and transmits it to output depending on the control signal. It implement the function Z = I0Sbar+ I1S. When select line S is low, output selects the signal I0 and when select line S is high, output selects the signal I1[8].

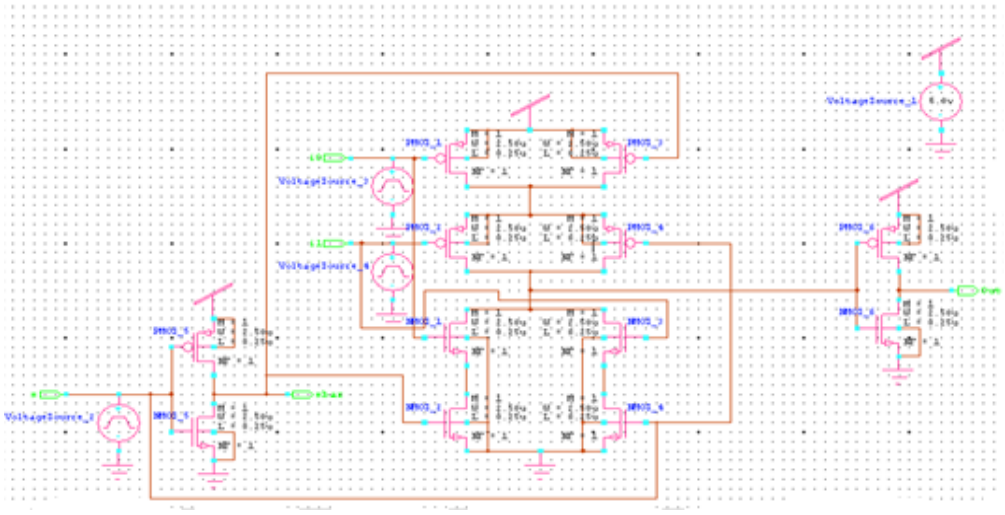

Figure 7. Schematic of Conventional CMOS 2:1 MUX

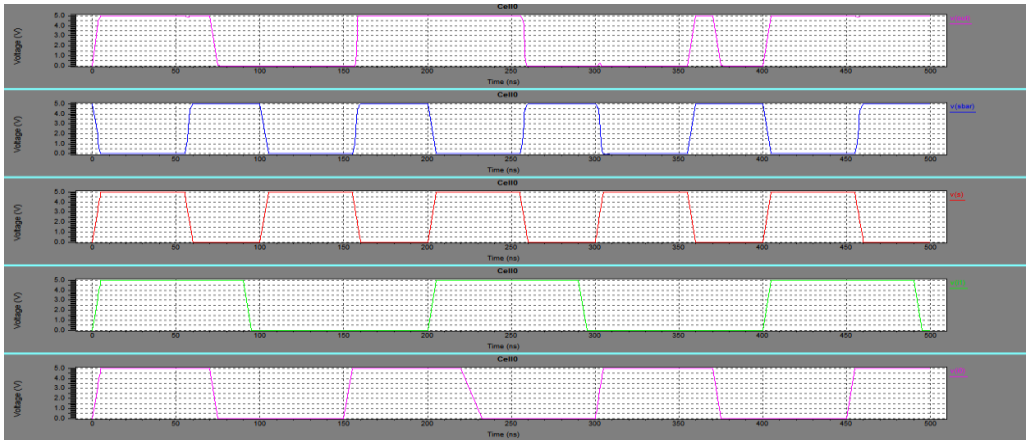

Figure 8. Simulated Waveform of 2:1 CMOS MUX

3.4. Multiplexer Using ECRL

The logic density of ECRL MUX is more as compared to CMOS that is achieved by elimination of PMOS from each logic function. The schematic and simulated waveform of 2:1 MUX using ECRL is shown in Figure 9 and Figure 10 respectively. When the select input S is high, power clock rises from 0 to VDD, output out will select the input I1. When select input S is low, power clock rises from 0 to VDD, output out will select the input I0. All the functions are implemented using NMOS. The ECRL latch is realized using cross coupled PMOS & cascade logic array with NMOS logic tree. PMOS is used as pull up logic.

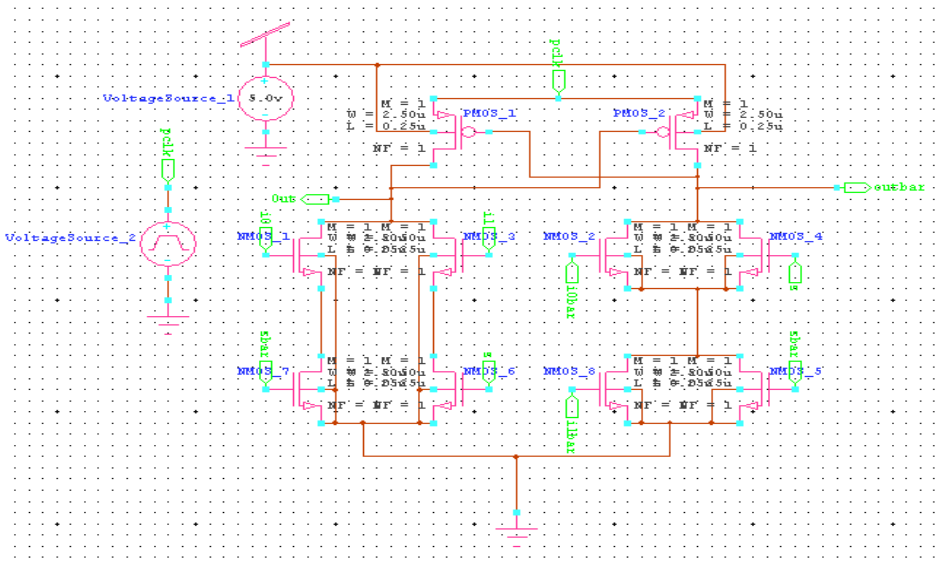

Figure 9. Schematic of 2:1 MUX Using ECRL

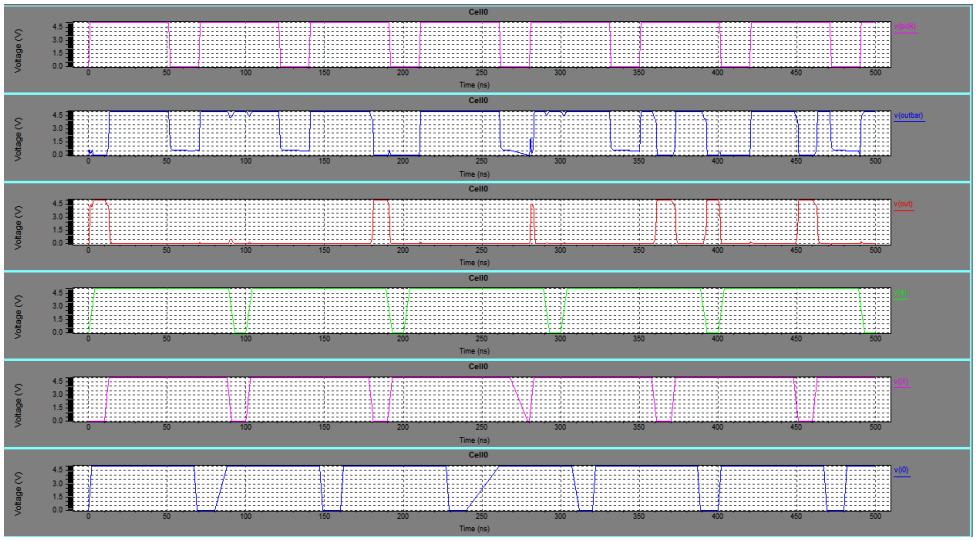

Figure 10. Simulated Waveform of 2:1 MUX Using ECRL

3.5. Multiplexer Using PFAL

The schematic and simulated waveform of 2:1 MUX using PFAL are shown in Figure 11 and Figure 12 respectively. The inverters connected cross coupled drives the two complementary outputs of the PFAL circuit. The logic function Z = I0Sbar+I1S is realized using NMOS network which is connected parallel to PMOS transistor & result in reduction of equivalent resistance of the logic network thereby reducing the power dissipation.

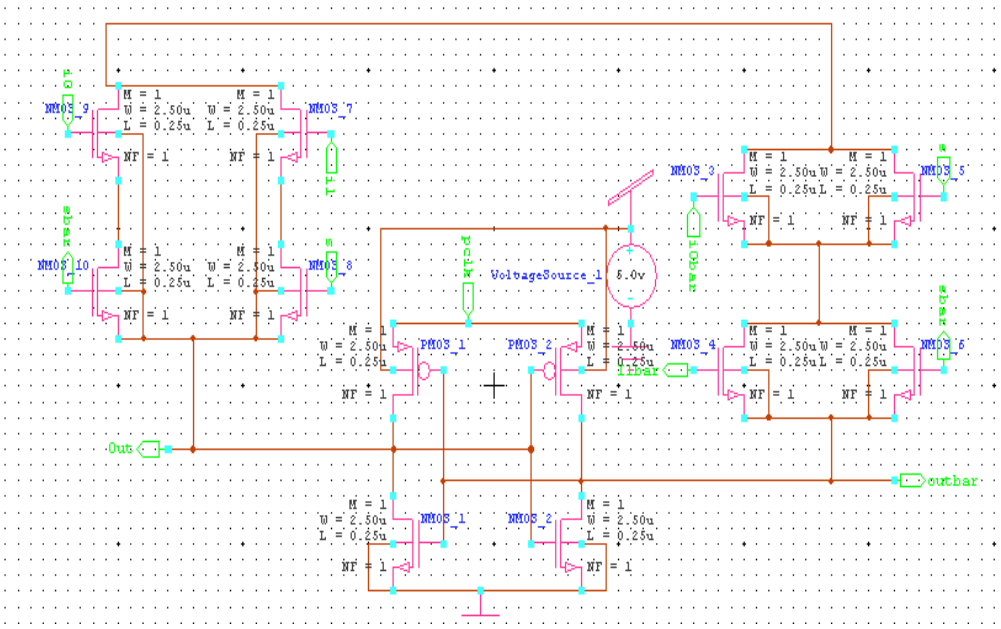

Figure 11. Schematic of 2:1 MUX Using PFAL

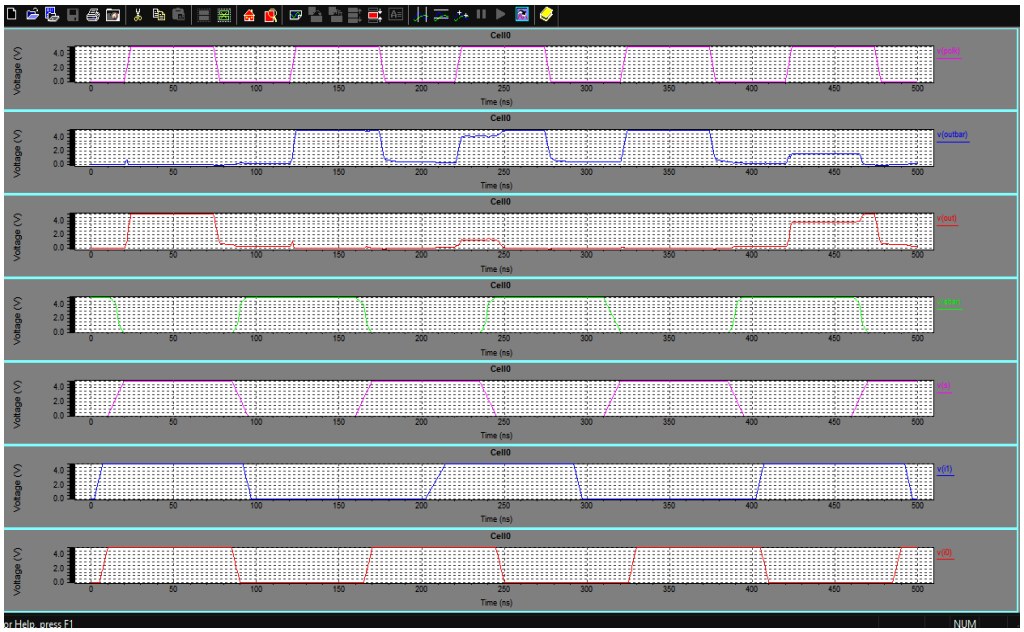

Figure 12. Simulated Waveform of 2:1 MUX Using PFAL

4. Supply Voltage and Frequency Variation

Power consumption in adiabatic circuits largely depends on parameter variations [7]. The impact of parameter variations on power consumption for the two logic families is investigated with CMOS logic circuits, by using TSPICE. Simulation is carried out at 180nm technology node. The W/L ratio for PMOS and NMOS are taken as 9λ/2λ and 3λ/2λ respectively where λ is 90nm.

4.1. Transition Frequency Variation

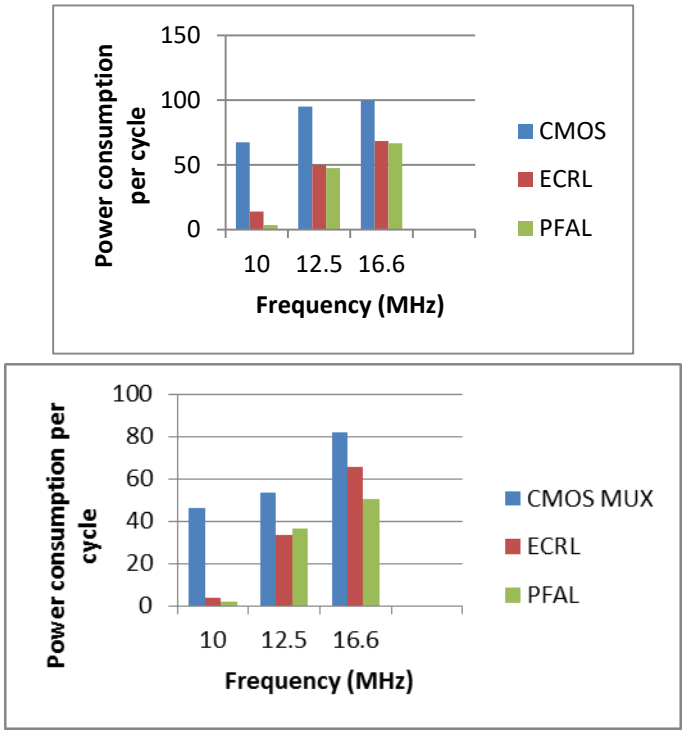

Figure 13. Power Consumption for Inverter and 2:1 Multiplexer

Figure 13 shows the power dissipation per cycle versus switching frequency of two adiabatic logic families and CMOS inverter and CMOS multiplexer. It is seen that at very high frequency, behavior is no more adiabatic and power dissipation increases for both CMOS and adiabatic logic. As we increase the frequency, power dissipation also increases. Thus, the simulation is carried out at useful range of frequency to show the better result with respect to CMOS [8].

Table 1. Shows the Average Power Consumption at Fixed Supply Voltage

Technology	Supply Voltage	Power Consumption
CMOS inverter	5V	444.42(nW)
ECRL inverter	5V	116.82(nW)
PFAL inverter	5V	115.70(nW)
CMOS 2:1 MUX	5V	406.53(nW)
ECRL2:1 MUX	5V	271.11(nW)
PFAL 2:1 MUX	5V	84.28(nW)

Table 1 shows the power consumption at fixed supply voltage equals to 5V. It shows the variation of power consumption of conventional logic circuits and adiabatic logic circuits. PFAL gives less power consumption among all circuits.

4.2. Supply Voltage Variation

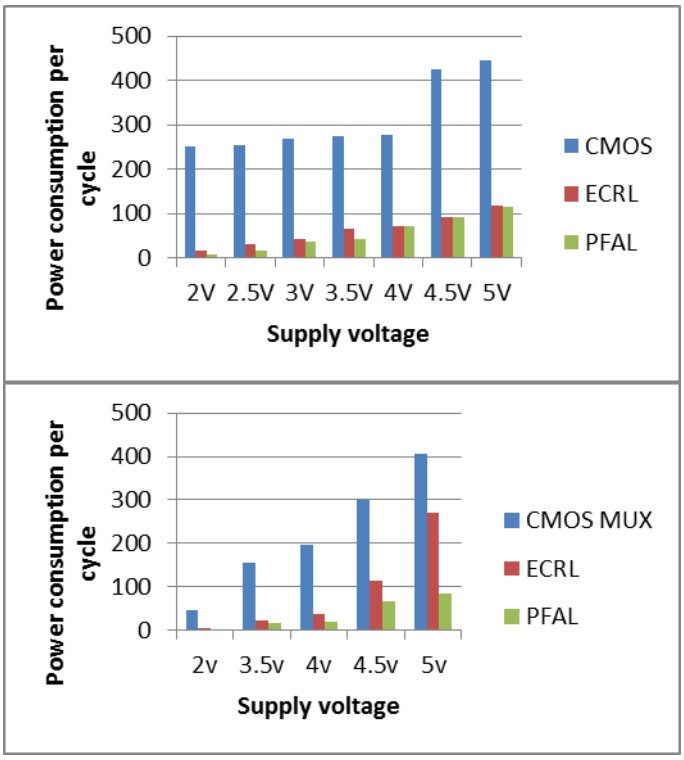

Figure 14. Power Consumption for Inverter and 2:1 Multiplexer

Figure 14 show the power dissipation per cycle versus supply voltage for both adiabatic logic families, for CMOS inverter and 2:1 MUX. It is seen that as the supply voltage decreases, gap between CMOS and adiabatic logic for CMOS inverter and MUX has been reduced. This shows the large energy saving over wide range of supply voltage[9]. printed material

5. Conclusion

A 2:1 MUX and CMOS inverter has been implemented using various adiabatic techniques and compared with conventional CMOS logic. The average power consumption of ECRL, PFAL & CMOS based MUX and inverter at different frequency and supply voltage has been observed. It was observed that power dissipation in ECRL and PFAL is less as compared to conventional CMOS logic. This Adiabatic technique can be used for low power application over wide range of parameter variations. Tanner EDA tool is used for the simulation of circuit at 180nm CMOS technology. A 2:1 Mux designed using adiabatic technique can be further used in applications such as barrel shifters, memory designing & other low power applications. This approach is suitable for implementing the array architecture, which realizes a certain class of DSP (Digital Signal Processing) applications. It can also be used in biomedical applications which require less power.

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