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Novel Adder Design Using Quantum Cellular Automata Implementation

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Abstract

Quantum Cellular Automata (QCA) has been widely used to digital circuits and systems in recent years. QCA technology is a promising alternative to CMOS technology, which offers a novel electronics paradigm for information processing and communication. It has the attractive features such as faster speed, higher scale integration, smaller size and lower power consumption than transistor technology. Previously, adder designs based on conventional designs were examined for implementation by QCA technology. A briefness cell is used as the basic element, which is a building block to construct gates and wires. In this paper, we propose two kinds of new adder designs based on QCA. One is full-adder, and the other is carry look-ahead half adder. The simulation results show that the adder designs we proposed are more robust and reliable compared with previous works in the aspects of complexity, area, crossing and delay.

Keywords*: QCA; QCA Logic Gate; Full-Adder; Carry Look-Ahead Half Adder; QCA Designer*

1. Introduction

It is well known that the famous Moore's law will reach its limitation because the present CMOS technology of VLSI design is approaching its scaling limit very fast. There has been extensive research on the nanoscale to replace conventional CMOS technology in recent years. Nanotechnology, especially Quantum-dot Cellular Automata provides new possibilities for computing owing to its unique properties [1]. It owns the attractive features such as faster speed, higher scale integration, smaller size and lower power consumption compared to transistor technology. QCA relies on afresh physical phenomena (Coulombic interaction), the logic states of which are not stored as voltage levels but the position of individual electrons. In the QCA structure, each independent QCA cell has two electrons, which have two polarization states meaning information "0" and "1", respectively. They are located at the diagonal positions of the QCA cells. The interaction between two adjacent QCA cells, due to Coulomb force, allows them to be used to communicate information with each other, and this method of transmission does not require any wire connections, and this method can also simulate complex circuit functions, which shows that QCA can make VLSI circuits better. As QCA has nonlinear and bistable saturation characteristics, the application of QCA in digital circuits has become a research hotspot. The applications of QCA in classical logic circuits include full adder, multiplier, selector, memory and so on [2-12]. This paper presents two kinds of new adder designs based on QCA. The flow of information through the circuits is controlled by four clock signals, each of which shifts by 90 degrees in phase. The design and simulation are carried out in the QCA Designer environment.

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The remainder of this paper is organized as follows. The fundamental of QCA is presented in Section 2. The logic designs of adders and comparison are given in Section 3. The simulation results are given in Section 4. The conclusions are given in Section 5.

2. Preliminaries

QCA is an array structure known as quantum-dots. Computing with QCA is achieved by the tunneling of individual electrons among the quantum-dots inside a cell and the classical coulombic interaction among them [2]. A QCA cell consists of two electrons, positioning at opposite corners according to coulombic repulsion. So the polarization states of P= -1 and P = +1 can be represented by two stable configurations of a pair of electrons. The corresponding logic values of "0" and "1" are represented in Figure 1.

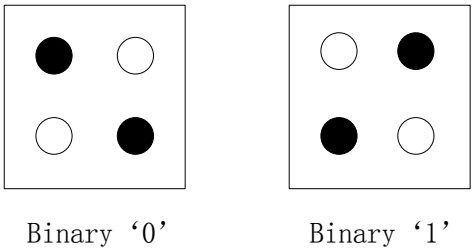

Figure 1. QCA Cells

The electrostatic repulsion between electrons leads to the synchronization of neighboring cells. Thus, one cell’s polarization is determined by the effect of its neighboring cell’s polarization. Therefore, the array of QCA cells will be able to propagate information as a wire [13]. The QCA cells can form the primitive logic gates such as inverter gate shown in Figure 2 and majority gate shown in Figure 3. A majority gate with the logic function of MV(A, B, C) = AB+AC+BC is composed of five cells. By setting one of the inputs of this gate permanently to 0 or 1, AND and OR functions will be formed in QCA. Some other combinational logic designs with plus-shaped quantum-dot cellular automata using minority gate as the fundamental building block have been presented in [2].The 5-input AOI (And-Or-Inverter) gate [4] has also been proposed to realize universal gate function.

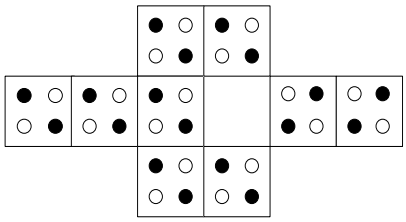

Figure 2. Inverter Gate

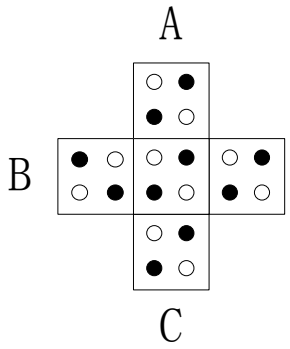

Figure 3. Majority Gate

The CMVMIN gate shown in Figure 4 is a new improved majority gate we proposed, which simultaneously realizes 3-input minority logic (MIN) and majority voter (MV) in its two outputs *OUT1* and *OUT2* in [5]. The *OUT1* = A′B′+B′C′+C′A′ is the complement of the *OUT2* = AB + BC + CA.

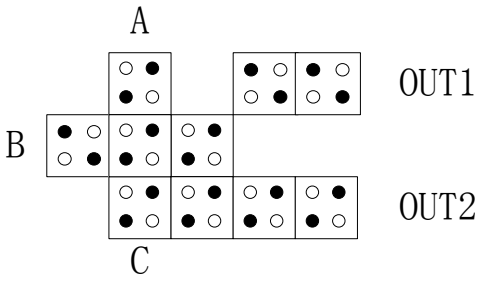

Figure 4. CMVMIN Gate

The basic QCA cell has no inherent directionality for information flow, so timing in QCA is accomplished by a cascaded clocking of four distinct and periodic phases [14]. In each phase, the clock signal has four states: high-to-low, low, low-to-high, and high. The cell begins to compute during the high-to-low state, holds the value during the low state, releases during the low-to-high state and stays inactive during the high state [7].

Coplanar wire-crossing is one of the very elegant features of this new low power computing paradigm In QCA. However, two types of cells are needed, and it is neither easy to fabricate nor very robust. In QCA based on logic designs, the utmost necessity is to ensure least number of wire crossings due to its single layer restriction [8].

3. Proposed Adder Designs and Presentation

3.1. One-bit Full-Adder Design

According the earlier adder design rules, the equations used for a full adder are given as follows:

$$s_i = a_i b_i c_i + a_i \overline{b_i}\,\overline{c_i} + \overline{a_i} b_i \overline{c_i} + \overline{a_i}\,\overline{b_i} c_i = M(\overline{c_{i+1}}, M(a_i, b_i, \overline{c_i}), c_i) \quad (1)$$

$$c_{i+1} = a_i b_i + b_i c_i + c_i a_i = M(a_i, b_i, c_i) \quad (2)$$

Using above equations, one of the previous logic structure designs of full adder is implemented as shown in Figure 5.

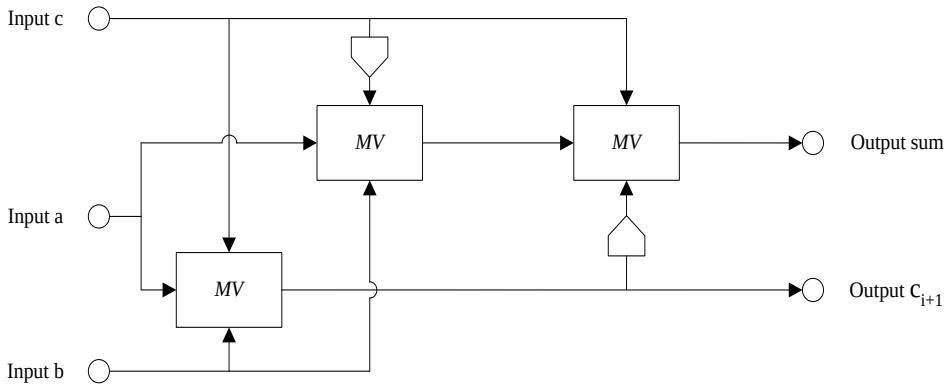

Figure 5. Previous Full Adder Schematic

In this paper, we proposed a whole new design of a full adder, the logic structure of which is presented in Figure 6. The proposed adder design shows a less spend on cell area and the number of QCA logic gates, which is in contrast to the conventional full adder. In the other hand, this structure makes a masterly method to avoid the wire crossing.

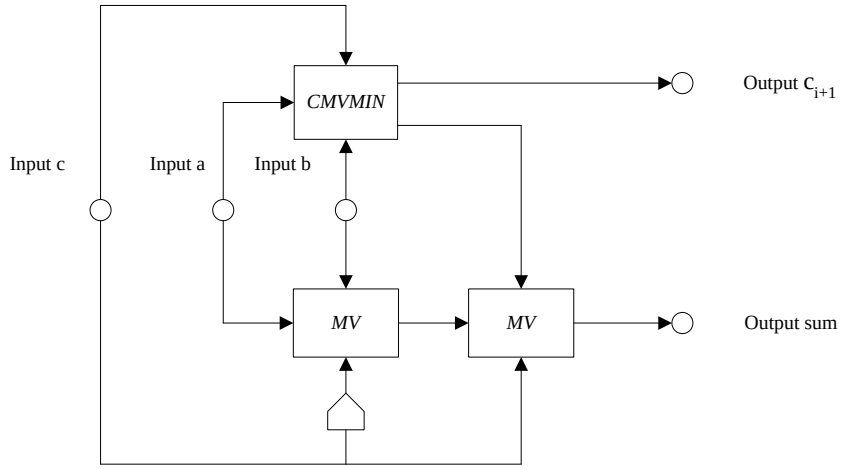

Figure 6. Proposed Full Adder Schematic

The QCA layout of this structure was described in Figure 7 using one inverter gate, two majority voter gates and one CMVMIN gate. This structure utilizes four-phases clocking zones in QCA. We compare this QCA layout structure with the latest and best full adder designs in [15, 18].

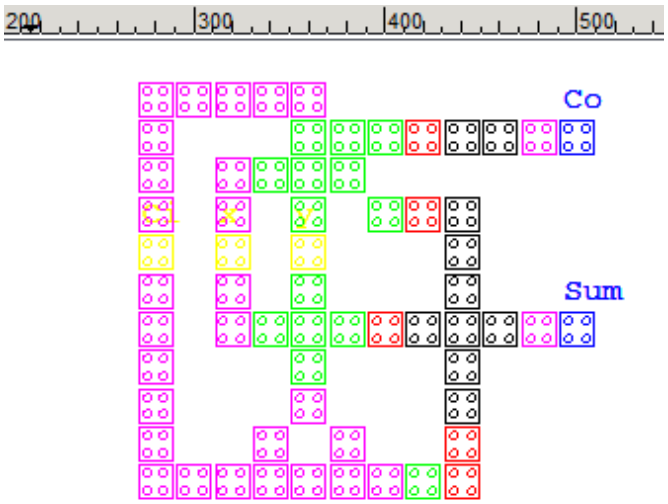

Figure 7. QCA Layout Structure of the Proposed One-bit Full Adder

The comparison results are presented in Table 1. These results indicate the proposed design consumes smaller area and has lesser complexity. Table 2 describes the improvement of the proposed design.

Table 1. Comparative Study of Two Designs

Full adders	Cell count	Gate count	Crossing count
Previous	102	5	3
Proposed	63	4	0

Table 2. The Improvements of Proposed Full Adder Compared with Previous Design

Type	Based on previous design
Cell count	38%
Gate count	20%
Wire-crossing count	$+\infty$

3.2. 2-bit Full-Adder Design

The one-bit full adder designed in the previous section performs one-bit addition, and in many cases two-bit or multi-bit addition operations are required in the digital logic circuit. The 2-bit Full-Adder layout shown in Figure 8 is based on the dense and robust full adder design introduced above. Comparison of Figure 7 and Figure 8 can be directly seen that the design of two-bit full adder is the superposition of two one-bit full adders.

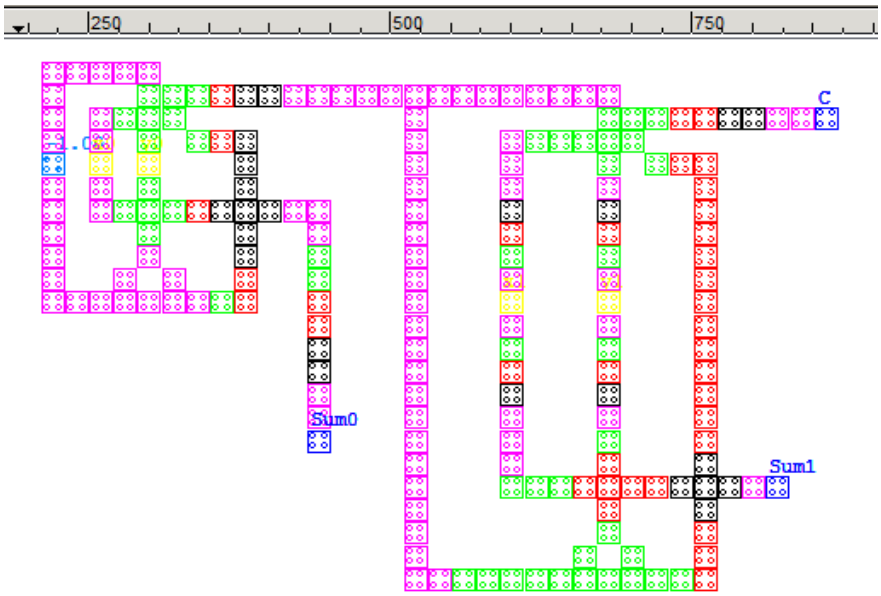

Figure 8. QCA Layout Structure of the Proposed 2-bit Full Adder

We also can construct the *n*-bit full adder through this method. However, we must be careful to construct the adjacent blocks to avoid inter-block disturbance. This is relatively easily achieved by keeping the distances larger than two cells, or the adjacent wires on different clock zones. In this design, most important of all is no wire-crossing in the whole adder layout. It reduces the possibility of something going wrong.

3.3. Carry Look-ahead Half Adder Design

The carry look-ahead adder, as its name suggests, carries the carry output signal first and outputs the output signal. Because the clock signal is used to control the flow of information in the design of QCA, the design of carry look-ahead adder using QCA has some advantages over the classical logic circuit design method. The design of carry look-ahead adder based on QCA was first proposed in [10], the design method of which was also based on the common full adder design by Equation (1) and Equation (2). Carry look-ahead adder's carry output went through the less clock delay than the sum output.

In this paper, we adopt the different design concept from the previous carry look-ahead half adder. For the half adder, we can get the equations as follows:

$$s_i = a_i \overline{b_i} + \overline{a_i} b_i = a_i \oplus b_i \quad (3)$$

$$c_{i+1} = a_i b_i = M(a_i, b_i, 0) \quad (4)$$

Equation (3) shows that the sum output of a_i and b_i is equal to their exclusive or (XOR). XOR gate module has been provided in QCA Designer. The carry outputs of a_i and b_i can be designed with a majority logic gate. Figure 9 presents the QCA layout of this carry look-ahead half adder. The clocking of the cells within this circuit is designed such that the carry will propagate before the sum is computed.

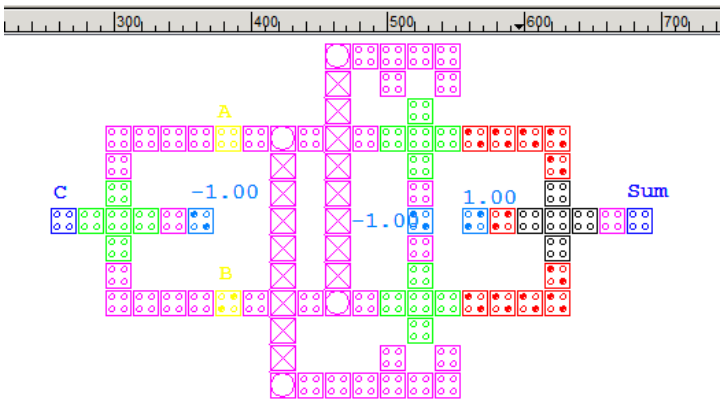

Figure 9. QCA Layout Structure of the Proposed Carry Look-ahead Half Adder

As can be seen from Figure 9, this method is very simple to design carry look-ahead half adder, the number of cells is very small, cell crossing number is only two, and it is a more optimized design.

There are two cells crossing in Figure 9 using a different plane crossing. Put the crossing cells onto a new layer so as to separate them from the main cell layer. In Figure 9, the cell with "○" is a sign meaning that the crossing layer intersects the main layer, and the "×" cells between two cells with "○" are cells on the crossing layer.

4. Simulation Results

The circuits are functionally simulated using the QCA Designer tool. In order to facilitate the analysis of the results, let the simulation is not a waveform output but the binary value display. Thus, we can see the simulation results more intuitively.

Figure 10 shows the simulation results of the proposed One-bit full adder circuit. Simulation results verify the correctness of this module. In the module shown in Figure 10, it goes through four clock zones from the input signals of X_i , Y_i , C_i to the output signals of C_0, Sum, which means that the delay is a full clock cycle. Therefore, the output C_0 and Sum are available one clock cycle delay after X_i, Y_i, C_i having been applied.

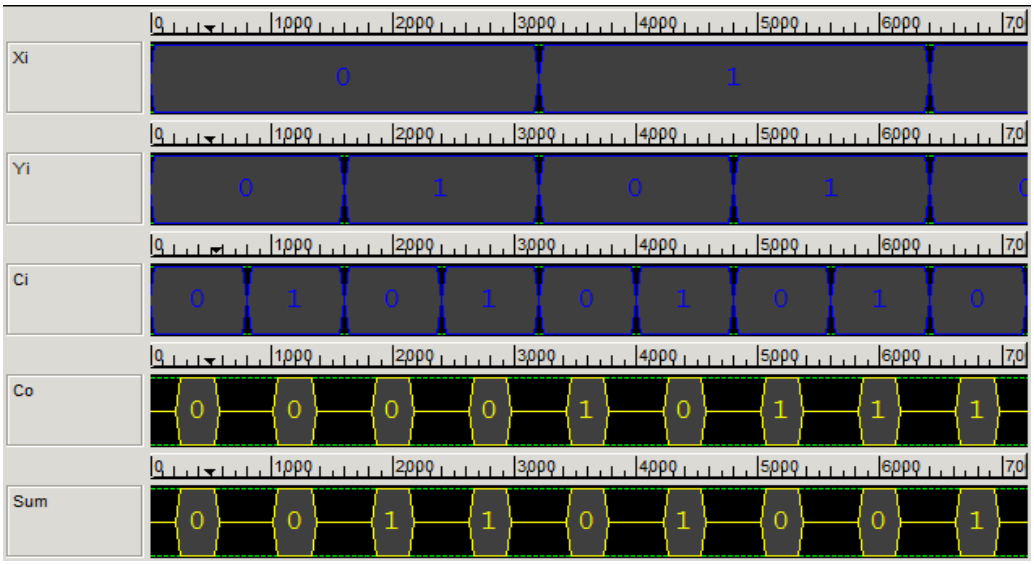

Figure 10. Simulation Result of the Proposed One-bit Full Adder

Figure 11 shows the simulation results of the proposed 2-bit full adder circuit. The input signal X_0 and X_1 form a two-bit input x[1: 0], and the input signal Y_0 and Y_1 form a two-bit input y[1: 0]. The output signals Sum_0 and Sum_1 form a two-bit output Sum [1: 0], and the output signal C_0 as a separate output. The difference from the one-bit full adder is that the clock delay of 2-bit full adder is two clock cycle. Simulation results verify the correctness of this module.

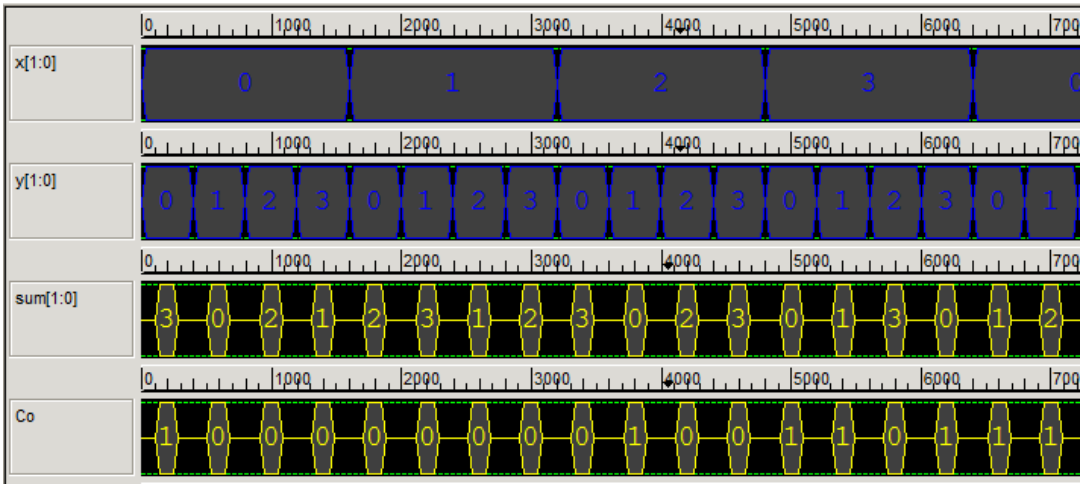

Figure 11. Simulation Result of the Proposed 2-bit Full Adder

Figure 12 shows the simulation results of the proposed carry look-ahead half adder circuit. However, the clock delay is divided into two parts (sum output and carry output). The delay of the sum output is one clock cycle, and the delay of the carry output is a quarter clock cycle. Simulation results also verify the correctness of this module.

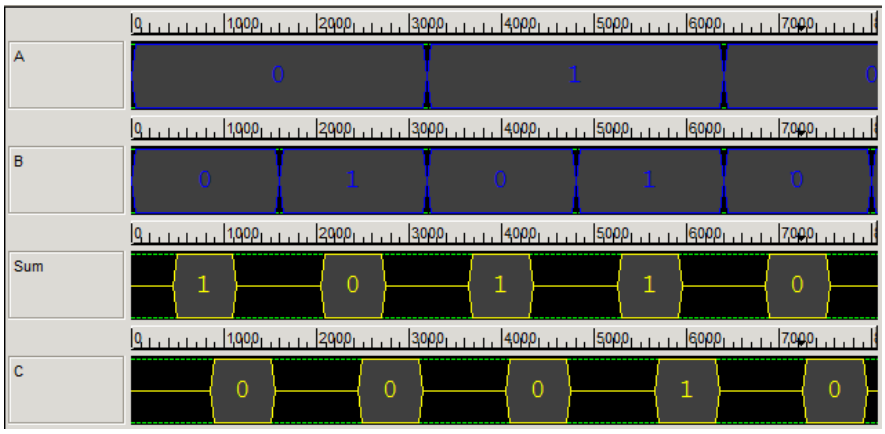

Figure 12. Simulation Result of the Proposed Carry Look-ahead Half Adder

5. Conclusions

One of the main goals of our design is to construct a robust and reliable full adder structure. We check the robustness and reliability of mentioned designs. The simulation results demonstrate that the proposed circuits are reliable. We also simulate the QCA layout based on previous circuit design. It is inferable that the proposed design is more robust and reliable than previous circuit design through the simulation results, because we use less QCA gate, less number of cells and wire-crossing. The reliability is very important when the component is used for the realization of larger designs.

The proposed method is an efficient way, which notably decreases the number of cells and the delay in signal propagation. We can easily construct complex *n*-bit full adder by this method. In addition, QCA logic functions and the relevant to new nanotechnology will provide high-speed computing and high-density adhibition. It is believed that QCA will become a more actual way to create faster and denser circuits.

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References

[1] C. Lent, and P. Tougaw. “A device architecture for computing with quantum dots”. Proceedings of the IEEE, vol.85, **(1997)**, pp. 541-557.
[2] Samir Roy, Biswajit Saha. “Minority gate oriented logic design with quantum-dot cellular automata”. Lecture Notes in Computer Science, vol. 4173, **(2006)**, pp. 646-656.
[3] S. Frost, A. F. Rodrigues, A. W. Janiszewski, R. T. Raush, and P. M.Kogge, “Memory in motion: A study of storage structures in QCA”, in Proc. First Workshop Non-Silicon Computing, **(2002)**.
[4] Momenzadeh, Mariam, Jing Huang, Mehdi B. Tahoori, and Fabrizio Lombardi. “Characterization, test, and logic synthesis of and-or-inverter (AOI) gate design for QCA implementation”. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on 24, no. 12, **(2005)**, pp. 1881-1893.
[5] S. Ditti, P. K. Bhattacharya, P. Mitra and B. K. Sikdar. “Logic Realization with Coupled QCA Majority-Minority Gate”. Proceedings of 12th IEEE VLSI Design and Test Symposium, **(2008)**.
[6] Mohammad Amin Amiri, Mojdeh Mahdavi and Sattar Mirzakuchaki, “LUT-Based QCA Implementation of a 4×4 S-Box”. TIC-STH, **(2009)**.
[7] Cho, Heumpil, and Earl E. Swartzlander. “Adder Designs and Analyses for Quantum-Dot Cellular Automata. Nanotechnology”, IEEE Transactions on, vol.6, **(2007)**, pp.374-383.

[8] Yinshui Xia, Keming Qiu. "Design and application of universal logic gate based on quantum-dot cellular automata". Communication Technology, ICCT 2008, 11th IEEE International Conference, **(2008)**, pp. 335-338.
[9] Mohammad Amin Amiri, Mojdeh Mahdavi and Sattar Mirzakuchaki, 2009 Second International Conference on Advances in Circuits. Electronics and Micro-Electronics, **(2009)**.
[10] Heumpil Cho and Earl E.Swartzlander, "Adder and Multiplier Design in Quantum-Dot Cellular Automata". IEEE TRANSACTIONS ON COMPUTERS, Vol.58 (6), **(2009)**.
[11] Hashemi, S, Azghadi, M.R, Zakerolhosseini, "A novel QCA multiplexer design". Telecommunications. IST 2008. International Symposium on. **(2008)**, pp. 692-696.
[12] Debarka Mukhopadhyay, Sourav Dinda, Paramartha Dutta, "Designing and Implementation of Quantum Cellular Automata 2:1 Multiplexer Circuit". International Journal of computer Applications, vol. 25(1), **(2011)**, pp. 21-24.
[13] Lent, Craig S., Tougaw, P. Douglas. "Lines of interacting quantum dot cells: A binary wire". Journal of Applied Physics, vol. 74, **(1993)**, pp. 6227-6233.
[14] Lent, Craig S., and Beth Isaksen. "Clocked molecular quantum-dot cellular automata". Electron Devices, IEEE Transactions on 50, no. 9, **(2003)**, pp. 1890-1896.
[15] Hanninen, Ismo and Jarmo Takala. "Binary Adders on Quantum-Dot Cellular Automata". Journal of Signal Processing Systems, 58(1), **(2010)**, pp. 87-103.
[16] V. S. Dimitrov, G. A. Jullien, K. Walus. "Quantum-dot cellular automata carry-look-ahead adder and barrel shifter". IEEE Emerging Telecommunications Technologies Conference,**(2002)**, pp. 2-4.
[17] Rigui Zhou, Xiaozhou Xia, Fengmei Wang, Yang Shi, Huichuan Liao. "A Logic circuit design of 2-4 decoder using quantum cellular automata". Journal of Computational Information Systems, 8(8), **(2012)**, pp. 3463-3469.
[18] Rigui Zhou,Tianru Xiao. "A Research on Simulation Engines of Quantum-dot Cellular Automata". Journal of Computational Information Systems, 9(3), **(2013)**, pp. 977-985.

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