International Journal of Signal Processing, Image Processing and Pattern Recognition
Vol. 10, No. 11 (2017), pp.1-12
http//dx.doi.org/10.14257/ijsip.2017.10.11.01

Design and Analysis of Various Gates using Efficient Charge Recovery Logic (ECRL)

Prerna Chauhan[1] and Bal Krishan[2*]

[1]Scholar, YMCA University of Science & Tech., Faridabad, (Haryana)- 121006, India
[2]A.P., YMCA University of Science & Tech., Faridabad, (Haryana)- 121006, India
[1]prernac20@gmail.com, [2]kadiyan26@yahoo.com

Abstract

In the past CMOS technique were used for low power consumption in the electronic devices but there is power consumption due to switching activity, leakage current and short circuit current. One of the major sources of power dissipation is the charging and discharging of load capacitor. To avoid this drawback ADIABATIC technique is used. In this paper gates are design with these technique and different parameters are compared. Tanner tool is used for the simulation of the circuits. From the compared result it is found that ADIABATIC technique is advantageous in low power devices.

Keywords: *CMOS, Adiabatic logic, ECRL, low power*

1. Introduction

As power dissipation now end up an outstanding concern in design of low electricity VLSI circuits for transportable and no portable packages. Circuit designers largely targeted on voltage scaling as in conventional circuits device switching is the cause of power dissipation. To lessen the power dissipation, the discount in supply voltage is the opportunity additionally circuit fashion designer can reduce the switching activities, lower the node capacitance or observe a mixture of all those strategies together. Yet in all above condition, the power is used most effective as soon as after drawn from the supply.

A novel magnificence of logic circuits referred to as Adiabatic logic good judgment uses consistent current source and gives the possibility of decreasing power dissipation at some stage in the switching activities, and recycling, reusing, a number of the power drawn from the deliver. In this method the fed on power is recycled returned to the power supply thereby lowering common power consumption. Efficient charge recovery logic (ECRL) is one of the standard logic style investigated from adiabatic common sense, that's strength efficient as compared with conventional CMOS circuits and additionally been carried out in many sequential circuits.

In this paper gates are carried out using ECRL logic fashion. Circuit performance has been analyzed and comparative power analysis has been finished.

2. Adiabatic Logic

The phrase adiabatic is derived from the Greek phrase “adiabatic”, which means there's no trade of strength with the environment and hence no strength loss in heat dissipation. Adiabatic good judgment is normally used to lessen the energy loss in the course of the charging and discharging system of circuit operation. Adiabatic logic is likewise referred to as “energy recovery” or “charge recovery”. [8]

Received (May 25, 2017), Review Result (August 28, 2017), Accepted (August 30, 2017)

ISSN: 2005-4254 IJSIP

Sensible adiabatic households can be labeled as both Partially Adiabatic andCompletely Adiabatic.

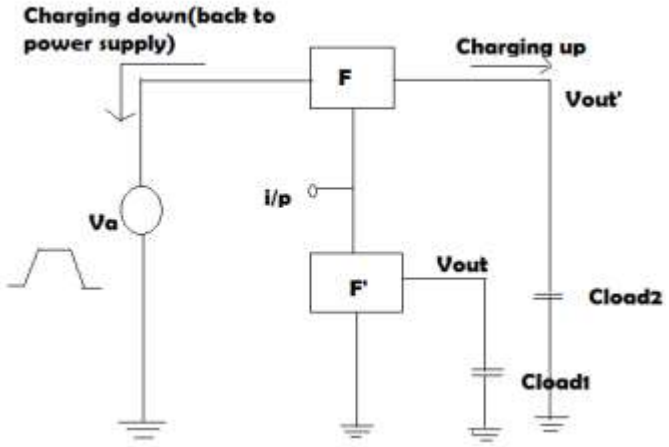

Figure 1. Circuit for Energy Recovery Charging and Discharging [7]

In a Partially Adiabatic circuit, some charge is authorized to be transferred to the ground, at the same time as in a Completely Adiabatic circuit, all the price at the load capacitance is recovered by way of the power deliver. Completely adiabatic circuits face lots of troubles with recognize to the operating velocity and the inputs power clock synchronization.

Partially Adiabatic

Maximum of the partly adiabatic circuits use crossed coupled gadgets; meaning, a flip-flop like crossed coupled, connecting two nodes that shape the true and complementary outputs, when a voltage romp is ramp is carried out the outputs settled to one of the states based totally on the outputs; which means, in this example we do no longer genuinely use transmission gates in preference to, we use traditional NMOS and PMOS transistors; however, there's a non-adiabatic dissipation of about (½)CL V_{th}^2 for transition from one kingdom to every other.

Completely Adiabatic

Implementations of completely adiabatic circuits are very highly-priced. You may require huge quantity of transistors, it's been discovered that, a completely reversible bit-stage pipelined 3-bit adder calls for. [13]

2.1. ECRL Technology

ECRL stands for Efficient Charge – Recovery Logic proposed by Moon and Jeong.

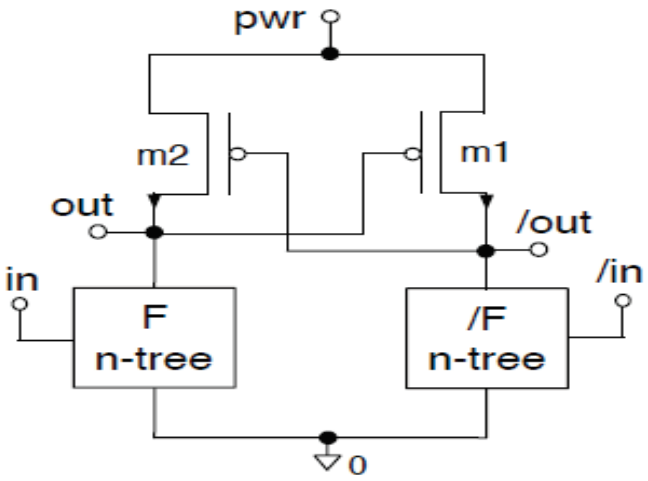

Figure 2. Basic Adiabatic Circuit

It has a cross-coupled PMOSFET .The fundamental production of ECRL is matched with cascade voltage switch logic (CVSL). It has two PMOSFET which can be linkedback to back like out/ is gives the input to m2 and out gives theenter to m1. For common sense operation, F n-tree and F/ n-tree blocks are used. A ramp or pulse voltage is implemented to the circuit, it'll be recycled returned to the essential supply. Outputs out and out/ are used to explain the condition of ECRL operation.[9]

2.1.1. Clocking Scheme (Trapezoidal Waveform)

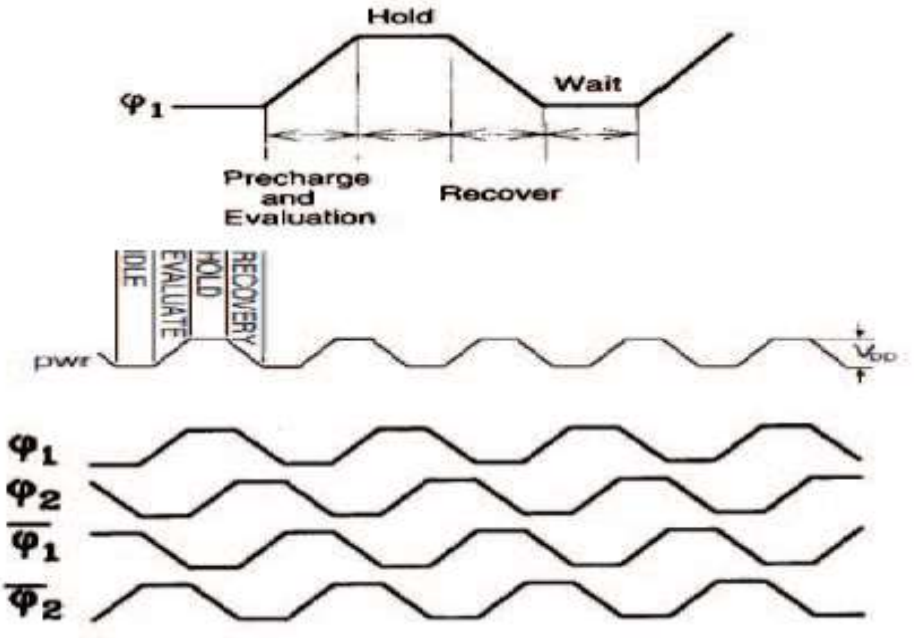

Figure 4. Four Phase Clock Cycle

The trapezoidal waveform plays an important role in charge recovery.

It has 4 phase named: **Pre-charge and Evaluation, hold, recover, wait**.

- In **Evaluation phase**: the junction capacitance is charged and logic is evaluated.
- In **hold phase**: the logic is kept at hold and used as input for next stage.

- In **recover phase:** the drawn power is fed back to the source.
- In **wait phase**: the circuit waits for the logic to be calculated in the previous stage. [11]

3. Implementation and Circuit Simulation

The simple gates are normally used in digital circuits. Some of the generally used gates are NOT, NAND, NOR, XOR .These gates are implemented the usage of adiabatic strategies ECRL with the aid of analyzing the fact table, forming Boolean equation after which designing the circuit in keeping with these equation.

3.1. NOT Gate

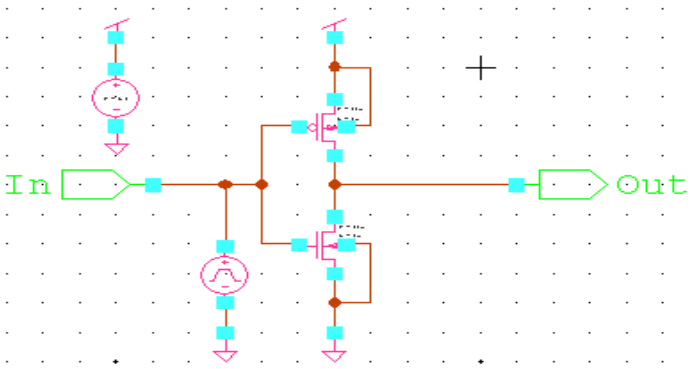

Figure 3. Circuit of CMOS NOT Gate

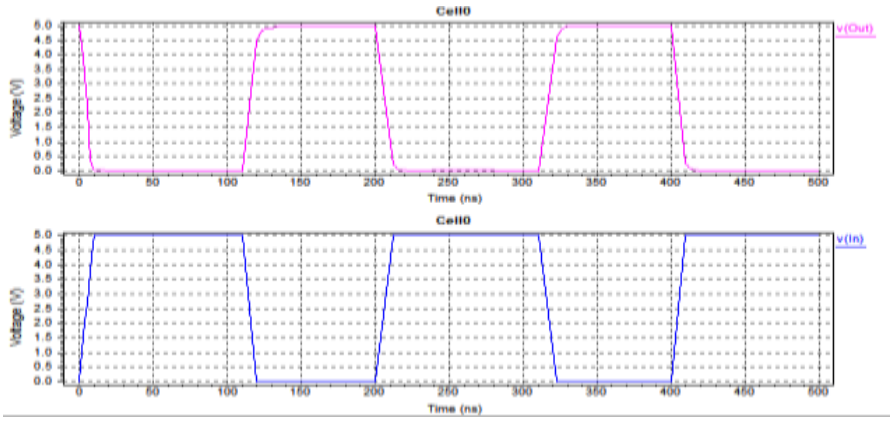

Figure 4. Output Waveform of CMOS NOT Gate

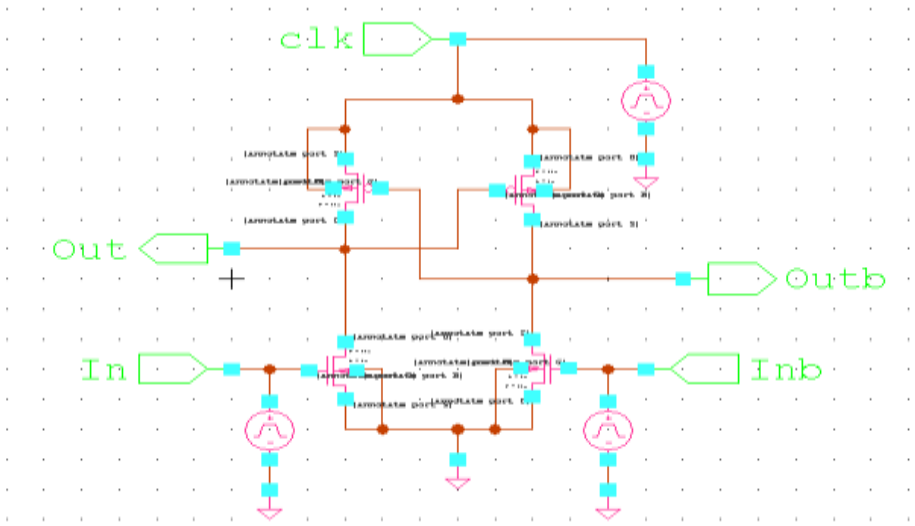

Figure 5. Circuit of ECRL NOT Gate

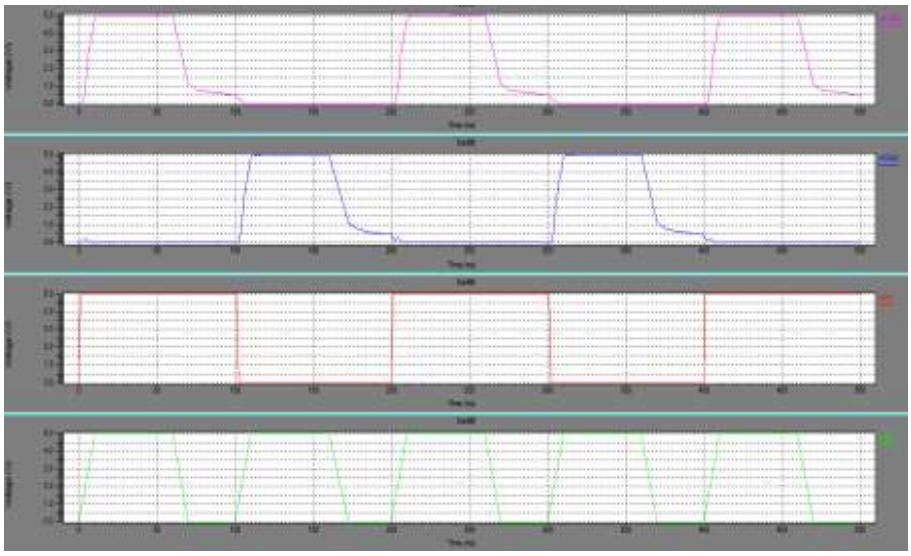

Figure 6. Output Waveform of ECRL NOT Gate

3.2. NAND Gate

Table 1. Truth Table for NAND Gate

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Boolean equation for logic 0: AB
Boolean equation for logic 1: A'+B'

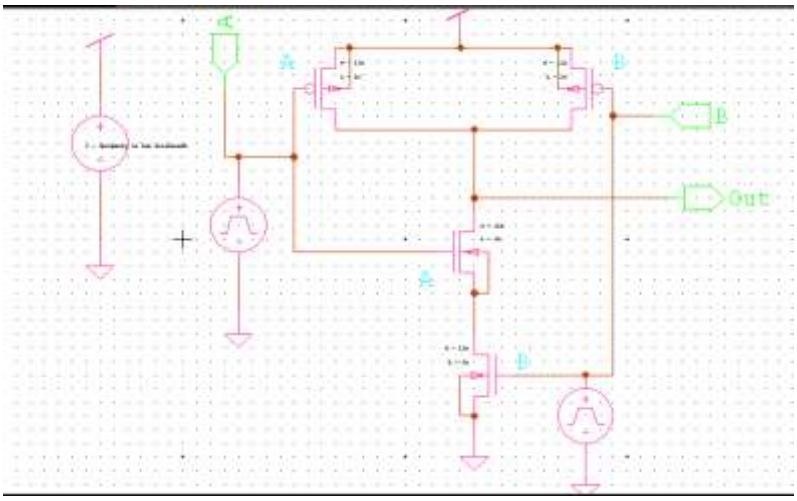

Figure 7. Circuit of CMOS NOT Gate

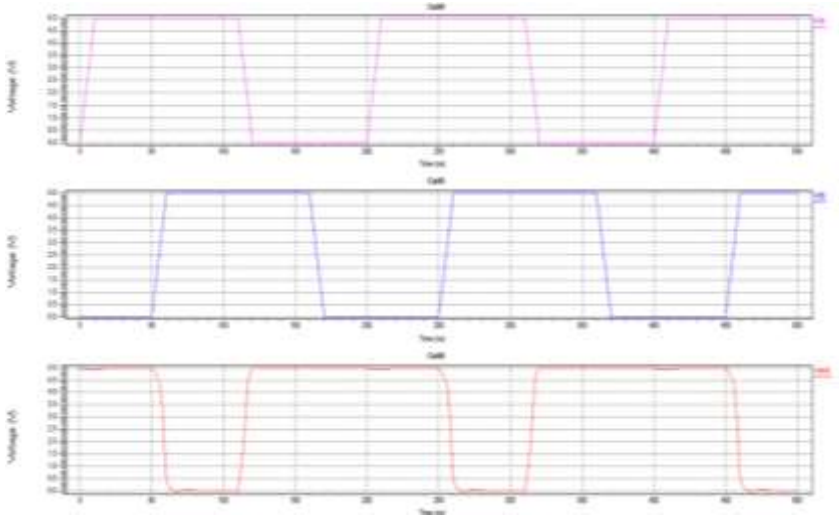

Figure 8. Output waveform of CMOS NAND Gate

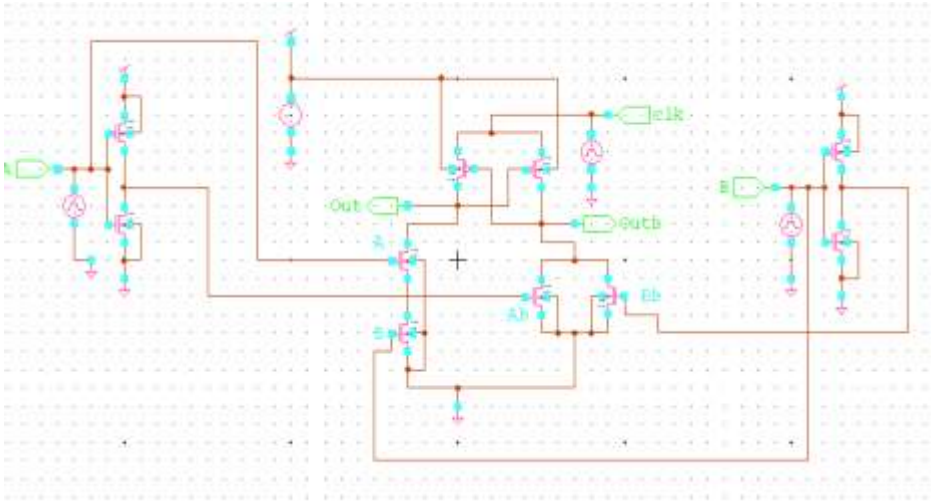

Figure 9. Circuit of ECRL NAND Gate

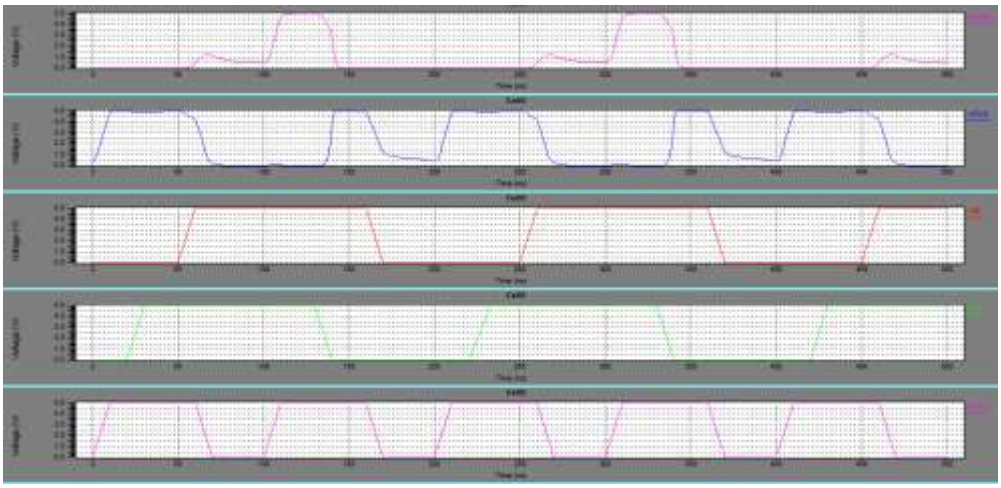

Figure10. Output Waveform of ECRL NAND Gate

3.3. NOR Gate

Table 2. Truth Table for NOR Gate

A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Boolean equation for logic 0: A+ B
Boolean equation for logic 1: A'B'

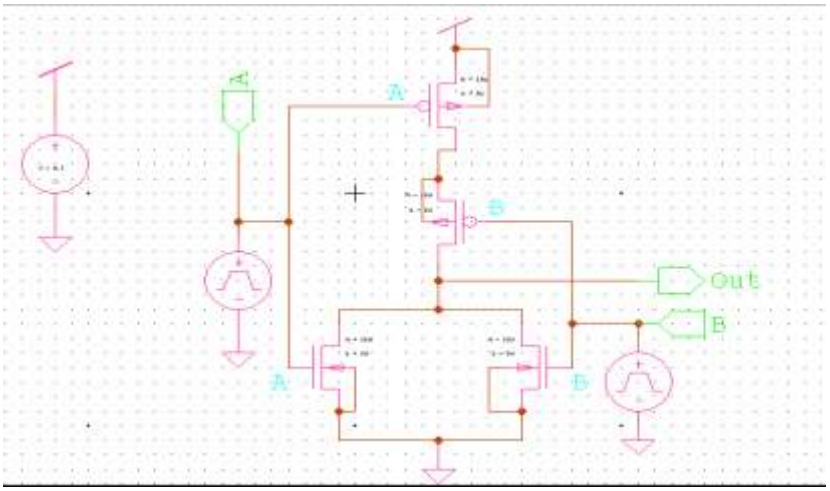

Figure 11. Circuit of CMOS NOR Gate

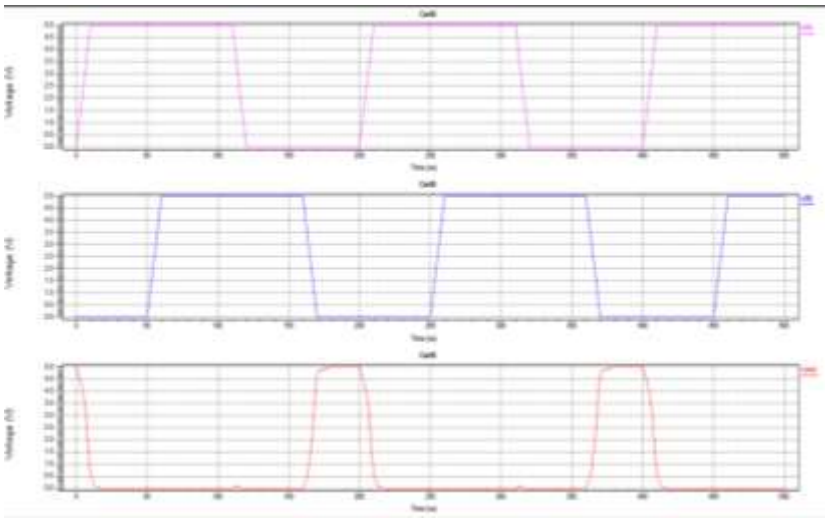

Figure 12. Output Waveform of CMOS NOR Gate

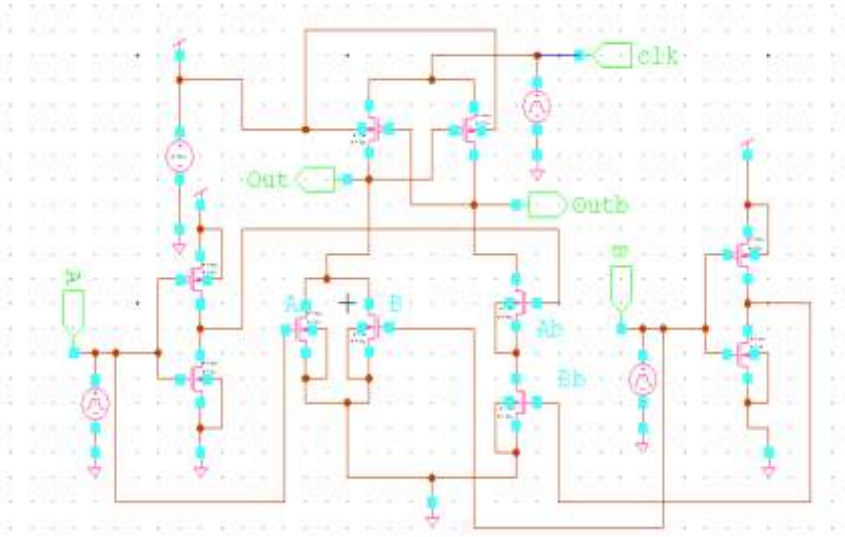

Figure 13. Circuit of ECRL NOR Gate

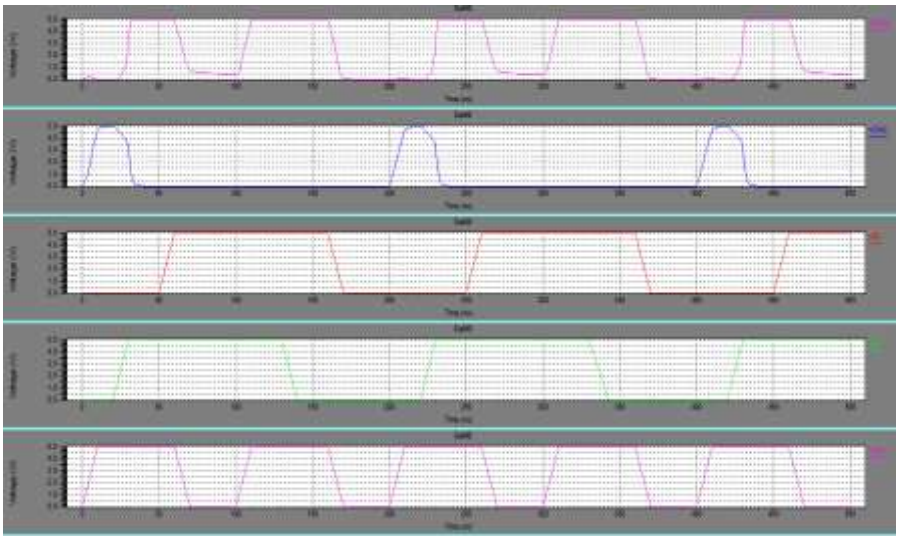

Figure 14. Output Waveform of ECRL NOR Gate

3.4. XORGate

Table 3. Truth Table for NOR Gate

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Boolean equation for logic 0: A'B' + AB
Boolean equation for logic 1: A'B + AB'

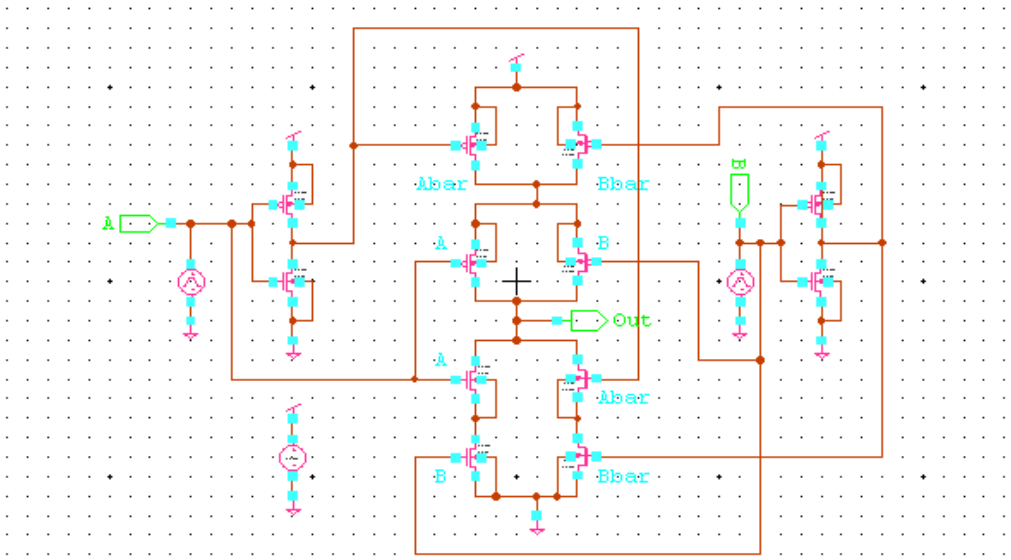

Figure 15. Circuit of CMOS XOR Gate

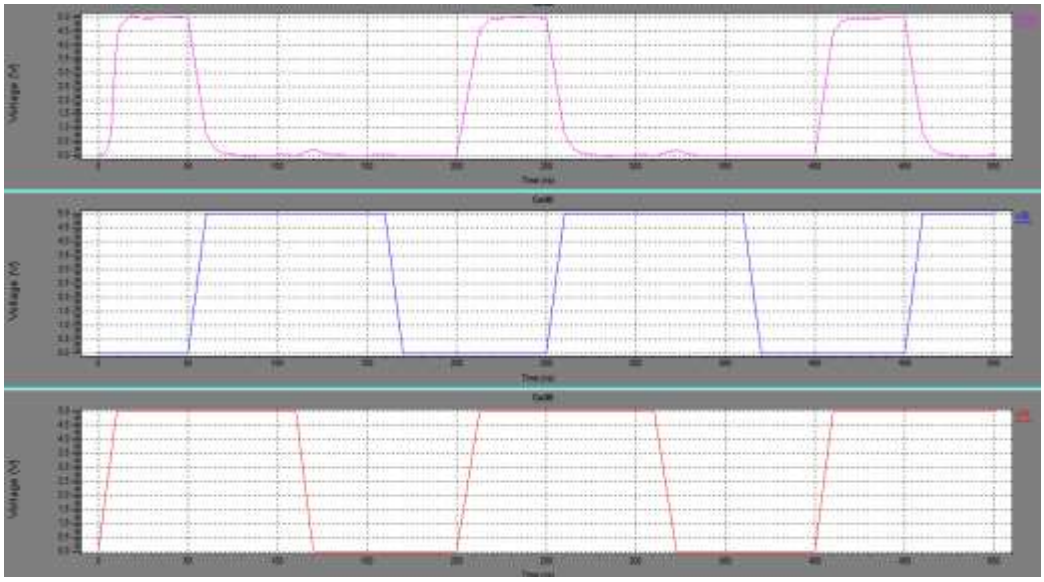

Figure 16. Output Waveform of CMOS XOR Gate

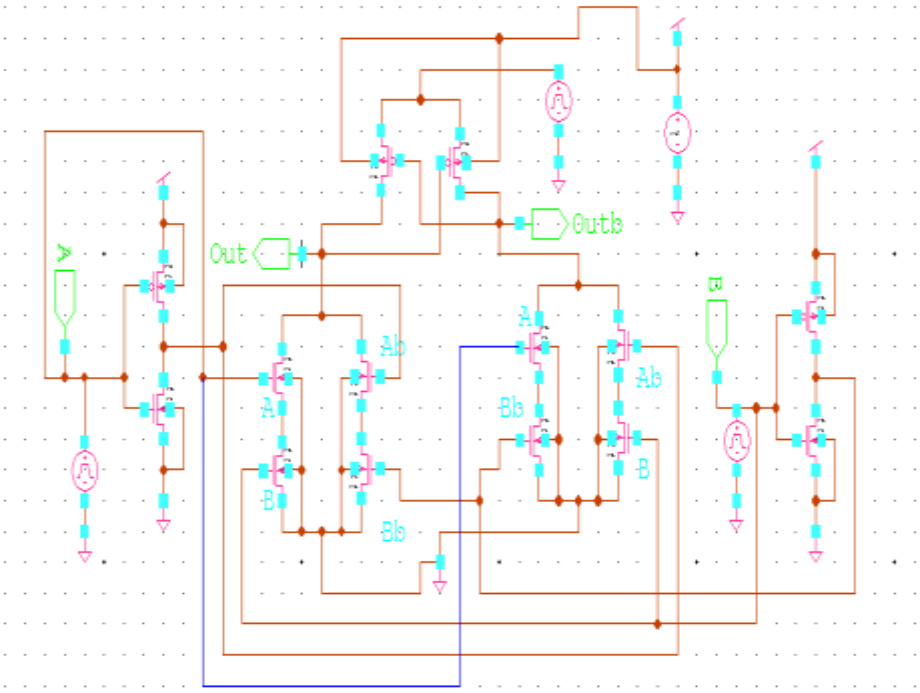

Figure 17. Circuit of ECRL XOR Gate

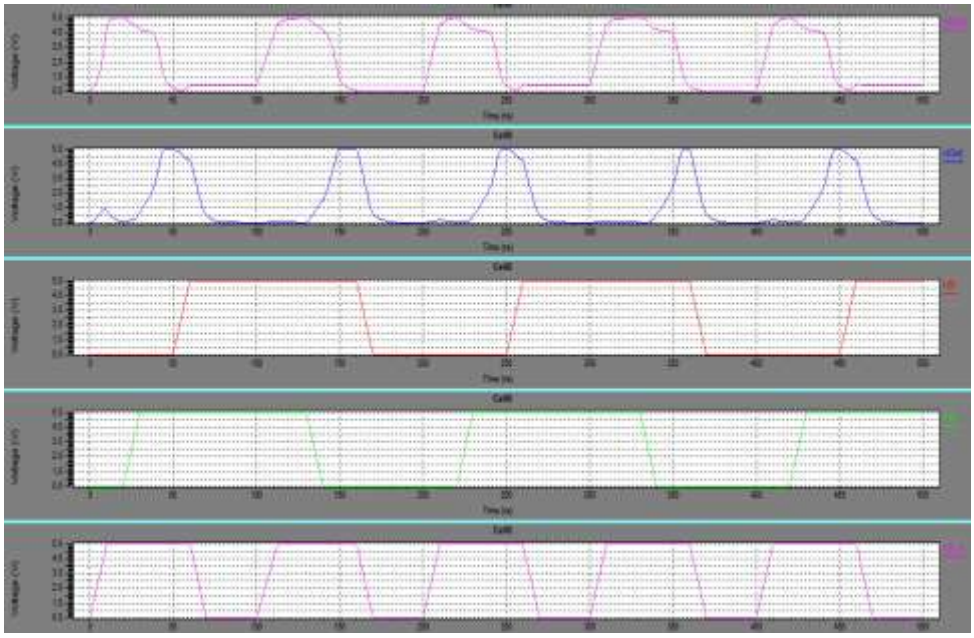

Figure 18. Output Waveform of ECRL XOR Gate

4. Result and Discussion

This section deals with the comparison of the CMOS logic style with the Adiabatic ECRL in terms of average Power consumed and No. of transistors. The results were simulated using TSPICE tanner tool in 180nm technology.

Table 4. Inverter Gateresult

Power Reduction Techniques	No. of Transistor	Average Power Consumed (In Watts)
Conventional	2	3.33278e-005
ECRL	4	6.493241e-006

Table 5. NAND Gate Result

Power Reduction Techniques	No. of Transistor	Average Power Consumed (In Watts)
Conventional	4	4.133877e-005
ECRL	10	3.367439e-006

Table 6. NOR Gate Result

Power Reduction Techniques	No. of Transistor	Average Power Consumed (In Watts)
Conventional	4	4.931314e-005
ECRL	10	1.892458e-006

Table 7. XOR Gate Result

Power Reduction Techniques	No. of Transistor	Average Power Consumed (In Watts)
Conventional	12	2.3528e-005
ECRL	14	4.819652e-006

The results show that the proposed adiabatic logic has less power dissipation compared to conventional CMOS design. These advantages made this logic more convenient for energy efficient digital applications.

6. Conclusion

This assignment proposes power efficient adiabatic logic for digital circuits. The consequences had been simulated using TSPICE and comparison has been executed for extraordinary widely wide-spread gates in adiabatic logic style and CMOS design. The results display that the proposed adiabatic logic has much less strength dissipation in comparison to standard CMOS layout. Those blessings made this common logic greater handy for power efficient digital applications.

ECRL is a low-power, adiabatic logic. Simulation shows electricity saving over static and other adiabatic logic households. The ECRL inverter chain shows 10-20 instances energy benefit over a conventional inverter chain. ECRL indicates large power saving and

shows the promising usage of ECRL in a low electricity device. With the adiabatic switching method, circuit energies are conserved as opposed to dissipated as heat. Depending on the application and the device requirements, this technique can once in a while be used to lessen the power dissipation of virtual structures

References

[1] Pal, "Low-Power VLSI Circuits and Systems", **(2014)**.
[2] K. Roy and S. C. Prasad, "Low Power CMOS VLSI Circuit Design", Wiley India Edition, **(2009)**.
[3] N. Goyal, R. Singla and P. Goyal, "Study & analysis of universal gates using stacking low power technique", International journal of computer science & Information technologies, vol. 6, no. 3, **(2014)**, pp. 4200- 4204.
[4] A.P. Chandrakasan and R.W. Brodersen, "Lowpower CMOS digital design", Kluwer Academic, Norwell, May 1995
[5] W.C. Athas, J.G.Koller, L. Svensson, "An Energy Efficient CMOS Line Driver using Adiabatic Switching", Fourth Great Lakes symposium on VLSI, California, **(2005)**.
[6] Dilip, P. S. Prasad and R. S. G. Bhavani, "Leakage power reduction in CMOS circuits using Leakage control transistor technique in nanoscale Technology", in International Journal of Electronics Signals and Systems (IJESS) ISSN: 2231- 5969, vol. 2, Iss-1, **(2012)**.
[7] http://research.ijcaonline.org/ic3s/number6/ic3s1357.pdf.
[8] https://en.wikipedia.org/wiki/Adiabatic_circuit.
[9] http://www.ijetae.com/files/Volume6Issue5/IJETAE_0516_36.pdf.
[10] http://www.ijctjournal.org/Volume1/Issue2/IJCT-V1I2P3.pdf.
[11] http://nanocad.ee.ucla.edu/pub/Main/SnippetTutorial/AdiabaticLogic.pdf.
[12] http://scialert.net/fulltext/?doi=itj.2007.325.331.
[13] http://ieeexplore.ieee.org/document/6637237/.

Authors

PrernaChauhan, she is a M. Tech. Scholar (VLSI Design: YMCA University of Science and Technology, Faridabad, Haryana-121006, India); B. Tech (Electronics and Communication Engineering: RKGITW, Ghaziabad-201017, India). Her Area of research: VLSI Design.

Bal krishan, he is an Assistant Professor, Electronics Engineering Department, YMCA University of Science and Technology, Faridabad, Haryana-121006, India; B.E. (Electronics & Communication Engineering: DCRUST Murthal, Sonepat, Haryana, India), M. Tech. (Nanotechnology : Jamia Milia Islamia Central University, Delhi, India), Ph. D. (pursuing in Nanoelectonics). He has published 35 numbers of papers in various International & National Journals &conferences.His Areas of research: Nanoelectronics & Devices, VLSI Design, Electronics Engineering.

