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Design of Energy Efficient Sinusoidal PWM Waveform Generator on FPGA

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Abstract

In this investigation, we are designing an energy efficient sinusoidal PWM Waveform Generator on a FPGA which obviously consumes less amount of power. The used power is obtained by varying ambient temperature level and then checking corresponding amount of energy consumed. There is a reduction of Leakage power in the percentage of 60.86 %, 52.17 %, 39.13 % and 21.73 % when we scaled down ambient temperature from 50 (C) to 0, 12.5, 25, 37.5 (C) respectively. SPARTAN-6 family FPGA is being used to implement sinusoidal PWM waveform generator.

Keywords*: Energy Efficient, Sinusoidal PWM Waveform Generator, FPGA, VHDL*

1. Introduction

The basic idea *here* is to generate or synthesize a sinusoidal PWM waveform by passing a digitally generated PWM through a low pass filter that is technically, known as Direct Digital Synthesis (DDS). We have analyzed the varying power with different levels of temperature in order to develop the energy efficient sinusoidal PWM waveform generator.. In this paper, we have used four different clock frequencies 50 MHz, 71.42 MHz, 125 MHz and 500MHz and four wave pulse frequencies 33.33 MHz , 47.61MHz , 83.33MHz and 333.33MHz respectively for the different level of ambient temperature level varying from 0 (C) to 50 (C) with a step value of 12.5 (C). Spartan-6 family FPGA is used for simulation and monitoring of total power consumed. SPARTAN-6 family has greatest system integration abilities and some points about SPARTAN-6 are highlighted Figure 1.

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Has lowest total cost.

Three Spartan-6 which are SLICEL, SLICEM and SLICEX.

Every CLB has two slices which are arranged side by side as a part of two vertical columns.

The power consumed is almost half the power consumed by previous families.

It offers more effective and efficient look up table i.e. LUT logic.

Figure 1. Some Important Feature about Spartan6

1.1. RTL Schematic

RTL is acronym for Register Transfer Level. RTL of our designed sinusoidal waveform generator is shown in Figure 2.

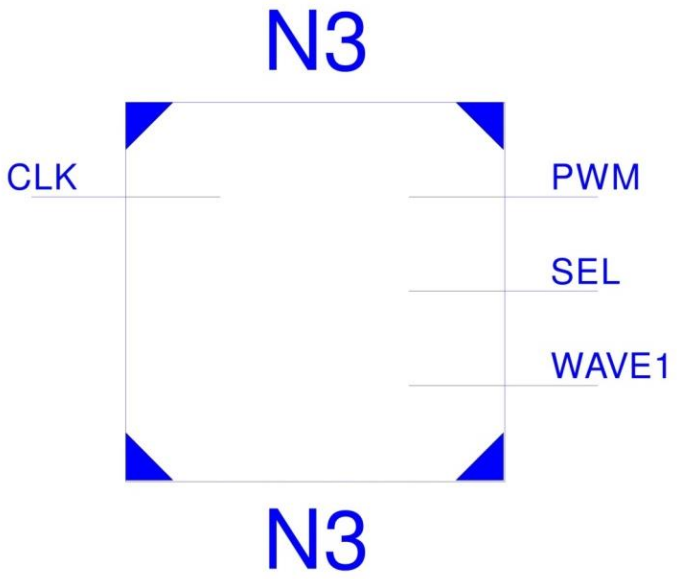

Figure 2. Basic Architecture of the RTL Schematic

As seen in the Figure 2, the RTL has one input clock port and three output ports such as PWM, SEL, and WAVE1. RTL schematics of sinusoidal PWM Waveform Generator. This block diagram define the external architecture of the N3 model which has total four port one is clock input port and others three are output ports which provides the PWM waveform.

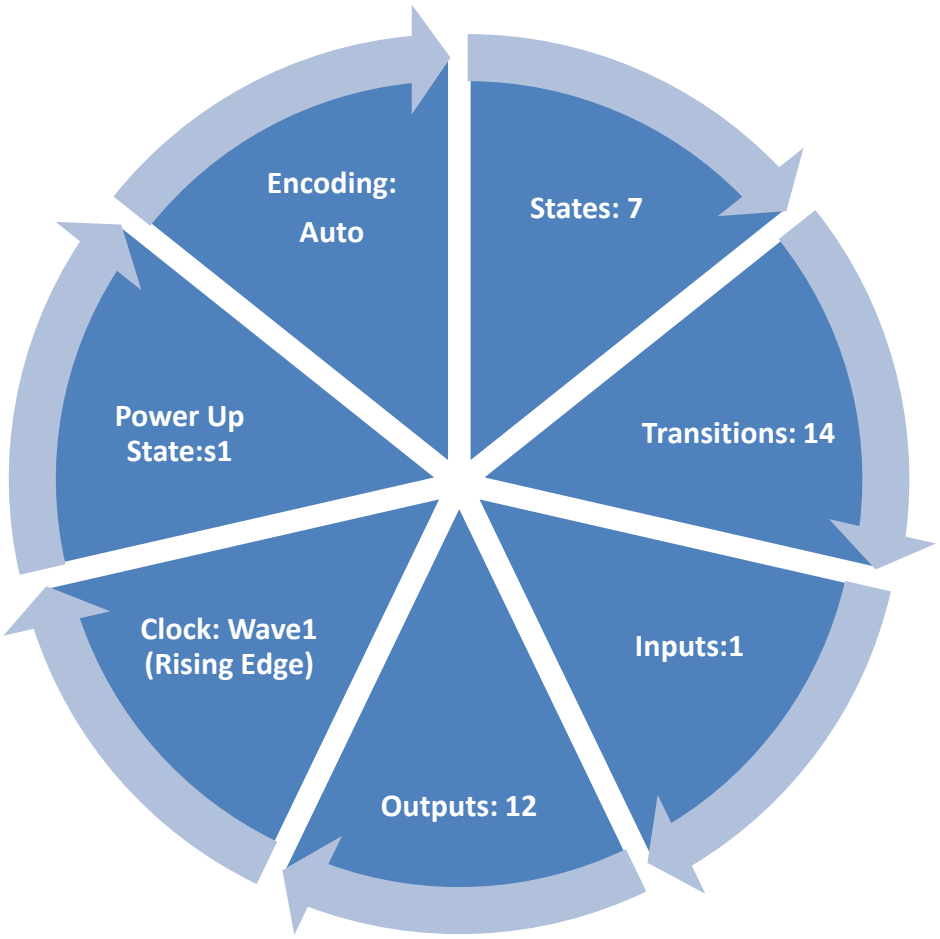

Figure 3. Initial Feature of the Synthesizing Modal N3 Design

As shown in Figure 3, N3 model has eight HDL synthesizing units for example number of States, Transitions, Inputs, Outputs are 7, 14, 1, and 12 respectively. Clocks pulse is rising edge WAVE1, power Up State is connected to state s1. Figure 4 illustrates internal architecture of RTL schematics of sinusoidal PWM waveform generator. In this type of model, we can take HDL synthesis report that contains Macro Statistics of components, which are being used in the model. This design is using 3 adders, 5 registers, 1 comparator and 1 finite state machine (FSM).

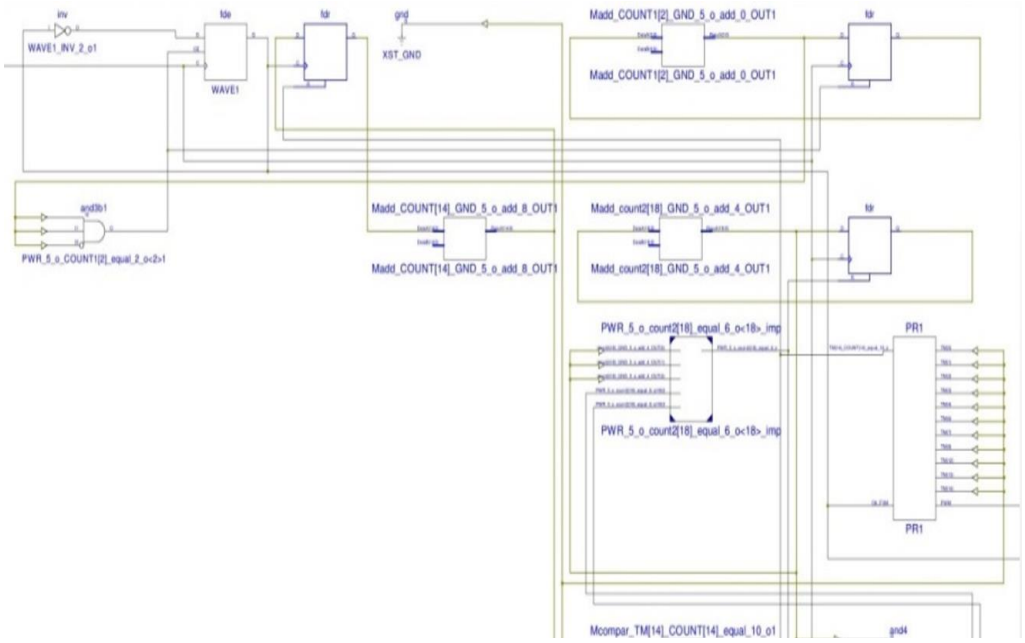

Figure 4. Internal Architecture of RTL Schematics of Sinusoidal PWM Waveform Generator (Part 1)

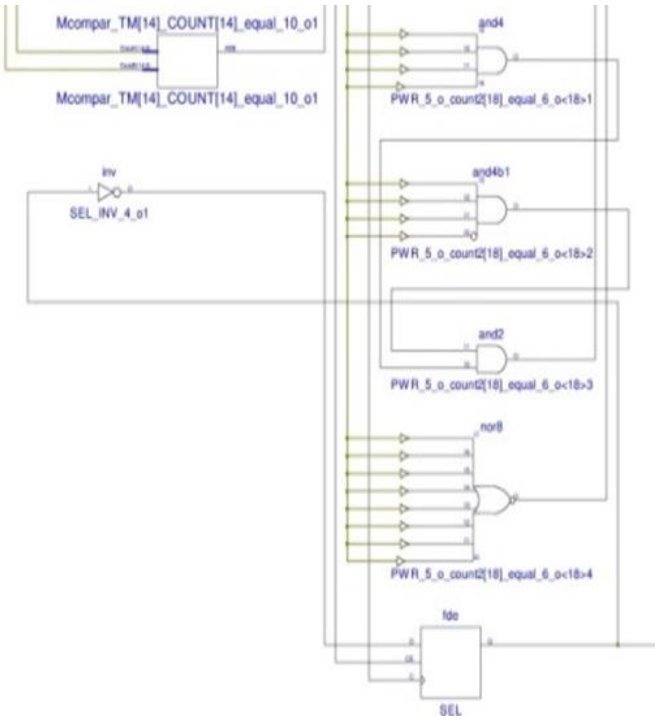

Figure 5. Internal Architecture of RTL Schematics of Sinusoidal PWM Waveform Generator (Part 2)

1.2. Technology Schematic

The RTL Schematic describe the technical architecture of the behavior of the model design. It has seven states and corresponding encoding bits are shown in the Figure 4 and Table 1. Technology schematic illustrates its actual implementation on FPGA.

Table 1. State and its Corresponding Encoding Bits of Finite State Machine

State	Encoding
S1	000
S2	001
S3	010
S4	011
S5	100
S6	101
S7	110

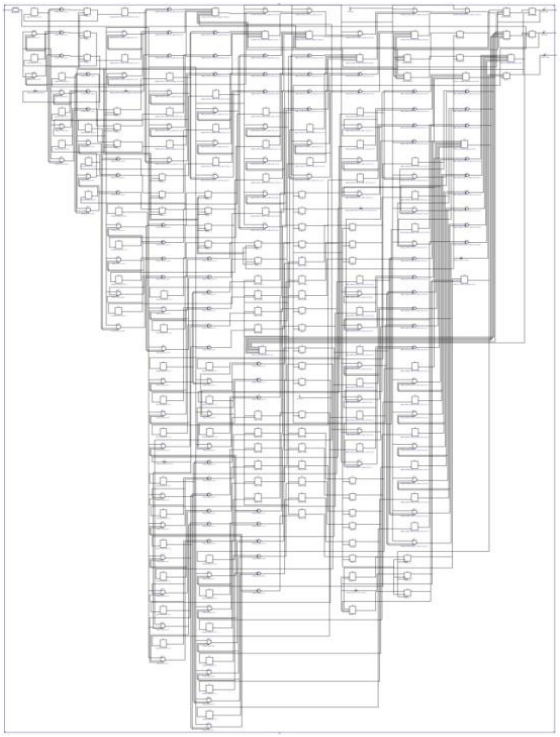

Figure 5. Technology Schematic of Sinusoidal PWM Waveform Generator

2. Related Works

In this reference research [1], work have been investigated and an energy efficient ALU using Mobile DDR IO standards has been designed. In our work, we are making Energy efficient PWM in place of ALU. We are using thermal scaling and frequency scaling in place of Mobile DDR IO standards. In this reference [2] researcher have designed an energy efficient Multiplier using Nikhilam Navatashcaramam Dashatah Vedic technique. Another researcher have performed power dissipation analysis of DES algorithm, implemented on a 28nm FPGA [3]. Some researcher have used thermal aware approach in an encoder design and also testing thermal stability by working on different ambient temperatures [4]. In our investigation, we are also using thermal and frequency scaling for making the design energy efficient. In this, reference [5] researchers have made energy efficient thermal aware image ALU Design on a FPGA. In this work researcher has tried to analyze the energy optimization possibility in counter design by the selection of energy efficient IO standards [6]. We are using different levels of thermal and frequency scaling in place of IO standards. In this research investigation researcher is using 11 different IO standards from HSTL and LVCMOS family to explore the

feasibility of Vedic Multiplier in Data Encryption Algorithm, DSP, Reliable System, Multimedia and Fault Tolerant Systems [7]. In this reference work [8] researcher have made thermal efficient ALU Design by using six different members of SSTL IOs standards. Researcher in this investigation have performed power analysis of DES algorithm, which is being implemented on a 28nm FPGA using HTML (H-HSUL, T-TTL, M-MOBILE_DDR, L-LVCMOS) technology [9].

3. Results

Table 2. Power Dissipation when Clock Period is 20ns and Period of Wave Pulse is 30 ns

Ambient Temperature (in C)	Clocks Power (W)	Logic Power (W)	Signals Power (W)	IOs Power (W)	Leakage Power (W)	Total Power (W)
0	0.002	0.000	0.000	0.008	0.009	0.019
12.5	0.002	0.000	0.000	0.008	0.011	0.021
25	0.002	0.000	0.000	0.008	0.014	0.024
37.5	0.002	0.000	0.000	0.008	0.018	0.028
50	0.002	0.000	0.000	0.008	0.023	0.033

We can see from Table 2 that there is a fall of 60.86%, 52.17%, 39.13% and 21.73% in the Leakage Power as the ambient temperature is scaled down from 50 (C) to 0, 12.5 , 25, 37.5 (C) Degree Celsius Respectively. The total power goes low by a percentage of 46.66%, 40%, 30%, and 16.66% as the temperature level is scaled down from 50(C) to 0, 12.5, 25, 37.5 (C) respectively. Figure 6. is displaying leakage and total power for the range of ambient temperature. There is no change in Clock Power (W) which has a constant value 0.001W and IOs Power(W) with a constant value 0.006W when ambient temperature is increasing from 0(C) to 50(C). Also note that there was no Logic Power (W) and Signal Power (W) consumed by the circuit within the range of our ambient temperature scale.

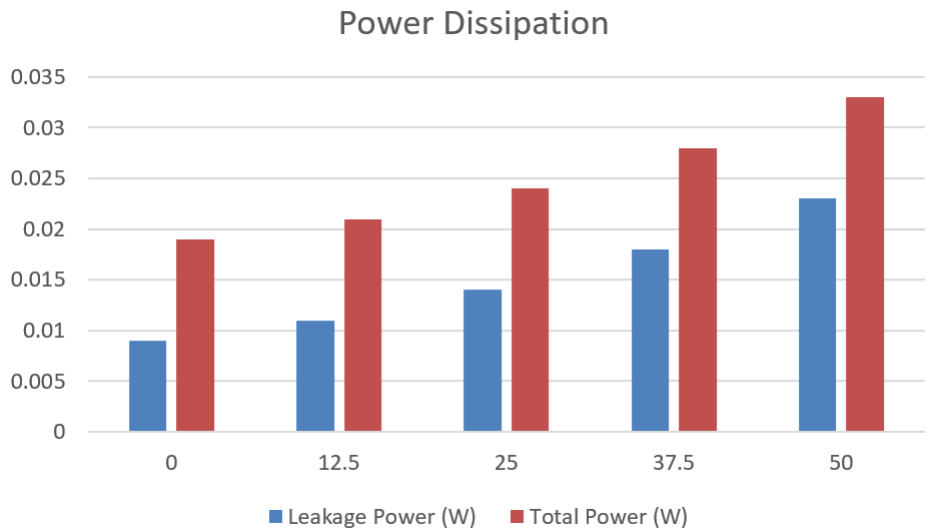

Figure 6. Power Dissipation by Sinusoidal PWM Waveform Generator

Table. 3 Power Dissipation when Period of Clock is 14 ns and Wave Pulse is 21 ns

Ambient Temperature (in C)	Clocks Power (W)	Logic Power (W)	Signals Power (W)	IOs Power (W)	Leakage Power (W)	Total Power (W)
0	0.001	0.000	0.000	0.006	0.009	0.016
12.5	0.001	0.000	0.000	0.006	0.011	0.018
25	0.001	0.000	0.000	0.006	0.014	0.021
37.5	0.001	0.000	0.000	0.006	0.018	0.025
50	0.001	0.000	0.000	0.006	0.023	0.030

For this case we can see from Table 3 and Figure 7 that there is a fall of 60.86%, 52.17%, 39.13% and 21.73% in the Leakage Power as the ambient temperature is scaled down from 50 (C) to 0, 12.5, 25, 37.5 (C) degree Celsius Respectively. The total power goes low by a percentage of 42.22%, 36.36%, 27.27%, and 15.15% as the temperature level is scaled down from 50(C) to 0 , 12.5 , 25 , 37.5 (C) respectively. There is no change in Clock Power (W) and IOs Power (W) both remains constant value with a value 0.002W and 0.008W respectively when ambient temperature is increased from 0 (C) to 50 (C). Also see no Logic Power (W) and Signal Power (W) was consumed by the circuit when the ambient temperature is varied from 0 (C) to 50 (C). Figure 7 is displaying leakage and total power for the range of ambient temperature when the clock period is 14 ns and pulse width is 21 ns.

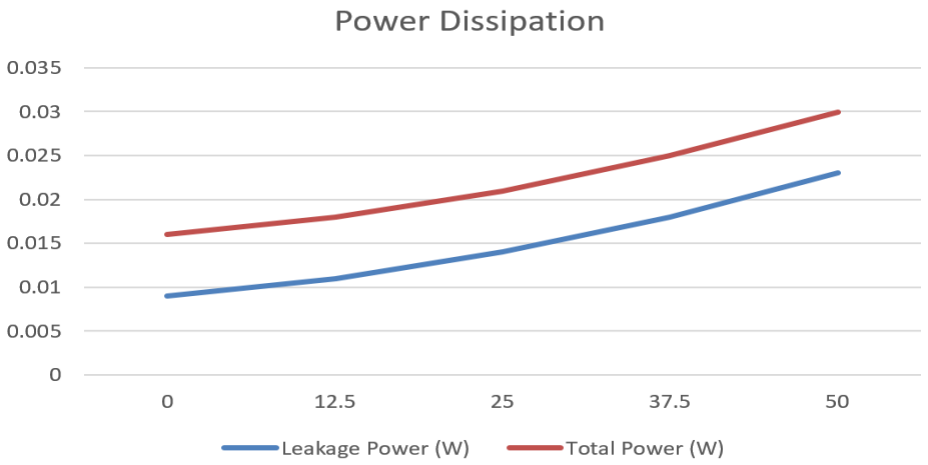

Figure 7. Power Dissipation when Clock Period is 14 ns and Period of Wave Pulse is 21 ns

Table 4. Power Dissipation when Period of Clock is 08 ns and Wave Pulse is 12 ns

Ambient Temperature (in C)	Clocks Power (W)	Logic Power (W)	Signals Power (W)	IOs Power (W)	Leakage Power (W)	Total Power (W)
0	0.003	0.000	0.000	0.014	0.009	0.026
12.5	0.003	0.000	0.000	0.014	0.011	0.028
25	0.003	0.000	0.000	0.014	0.014	0.031
37.5	0.003	0.000	0.000	0.014	0.018	0.035
50	0.003	0.000	0.000	0.014	0.023	0.040

Total power decreases by a percentage of 35%, 30%, 22.5%, and 12.5% as the temperature level is scaled down from 50 (C) to 0, 12.5, 25, 37.5 (C) respectively as shown in Table 4. There is no change in Clock Power (W) that stays at a constant value 0.003W and it is the case with IOs Power (W) with a constant value 0.014W during the scaling range. It should also be noted that no Logic Power (W) and Signal Power (W) was consumed by circuits when increasing in Ambient temperature from 0 (C) to 50 (C). Figure 8 is displaying leakage and total power for the range of ambient temperature when the clock period is 08 ns and pulse width is 12 ns.

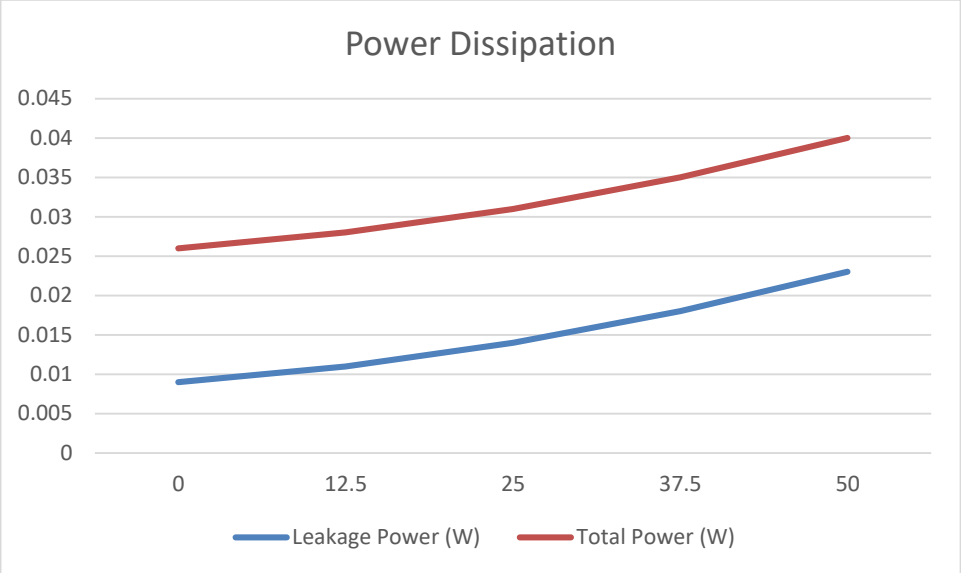

Figure 8. Power Dissipation by Sinusoidal PWM Waveform Generator

Table 5. Power Dissipation when Clock Period is 02 ns and Period of Wave Pulse is 03 ns

Ambient Temperature (in C)	Clocks Power (W)	Logic Power (W)	Signals Power (W)	IOs Power (W)	Leakage Power (W)	Total Power (W)
0	0.009	0.001	0.000	0.057	0.009	0.077
12.5	0.009	0.001	0.000	0.057	0.011	0.079
25	0.009	0.001	0.000	0.057	0.014	0.082
37.5	0.009	0.001	0.000	0.057	0.018	0.086
50	0.009	0.001	0.000	0.057	0.024	0.092

We can see from Table 5 and Figure 9 there is a fall of 62.5%, 54.16%, 41.66% and 25% in the Leakage Power as the ambient temperature is scaled down from 50 (C) to 0, 12.5, 25, 37.5 (C) degree Celsius Respectively. The total power goes low by a percentage of 16.3%, 14.13%, 10.86%, and 6.52% as the temperature level is scaled down from 50 (C) to 0, 12.5, 25, 37.5 (C) respectively. There is no change in Clock Power (W) and IOs Power(W) both stays at a value of 0.009W and 0.057W during ambient temperature scaling from 0 (C) to 50 (C). It should also be noted that there is no change in Logic Power (W) which has constant value 0.001W and no Signal Power (W) is consumed by the circuit when ambient temperature is scaled from 0(C) to 50 (C).

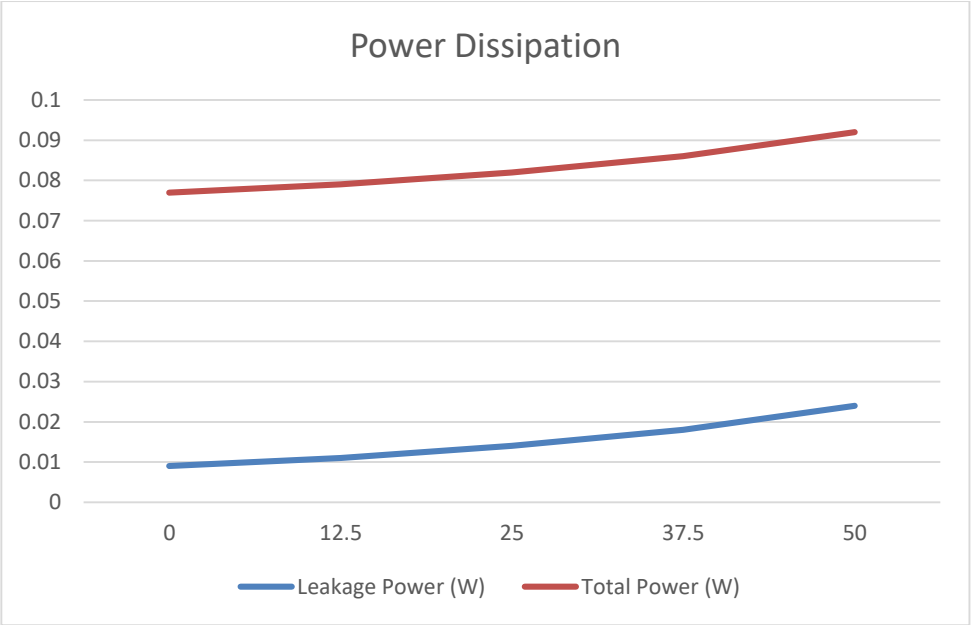

Figure 9. Power Dissipation Clock Period is 02 ns and Period of Wave Pulse is 03 ns

4. Conclusion

Reductions in clock, logic, IOs, leakage and total power values are obtained in our simulation. It is obvious from these tables that at higher value of ambient temperature more power is consumed and vice versa. Through this investigation we are able to design a low power sinusoidal PWM waveform generator with an efficient output. Spartan-6 gives low power readings and so is efficient for designing of not only sinusoidal PWM waveform generator but various other electronic designs. The frequency range used from 50M Hz to 500MHz for clock pulse and 33.33 MHz to 333.33MHz for wave pulse. For this frequency range the value of clock and IOs power remains the same and logic and signal power is negligible for different levels of ambient temperature scaling however due to leakage there is noticeable difference in total power consumed.

5. Future Scope

These results can be used in future for making efficient sinusoidal PWM waveform generator on FPGA. In this investigation work has been done on various frequencies at different levels of ambient temperature. It is important to make this useful device efficient and a lot of work can be extended in this field further. We can also use different FPGA families like automotive Artix-7, automotive coolrunner-2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan-3A, automotive Spartan-3E, automotive Spartan-6, Spartan-3, Spartan-3E. It is important to make this useful device efficient and a lot of work can be done in this field further.

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