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A Universal Reversible Gate Architecture for Designing N-Bit Comparator Structure in Quantum-dot Cellular Automata

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Abstract

Logic computing around quantum-dot cellular automata (QCA) has emerging area of high-speed nanoelectronics. We implemented the synthesis of the reversible comparator circuit in QCA regime that employs minimum primitives results. This paper presents a universal reversible quantum-dot cellular automata gate (URQG) and its implementation in QCA technology. The efficiency of the proposed gate in designing reversible circuits is validated by implementing the QCA standard benchmark Boolean functions. We also synthesize n-bit comparator, where proposed URQG and existing Feynman gates are cascaded together. Finally, in a QCA paradigm, we designed layout for the 1-bit and 2-bit comparators, and prove the better primitives results over existing layouts. Synthesis results indicate that the proposed 1-bit reversible comparator has achieved 75% improvement in delay and 95% improvement in quantum cost compared to existing design. The proposed gate currently aims the testability world such as cell deposition and HDLQ that test suite. The authors also show the energy dissipation results for existing benchmark reversible gates introduced in state-of-art technology and URQG gate that proposed herewith. QCADesigner tool is used to design and verify the functionality of the proposed designs. QCAPro tool is used for energy dissipation analysis of the proposed gate.

Keywords*: Logic gate; Reversible logic; Quantum-dot cellular automata; Fault-tolerant; HDLQ*

1. Introduction

In VLSI circuits we do feel the challenge to further scale down the transistor size and to decrease the power consumption [1]. The increases in the number of transistor in a chip are often driven by increased density and degrade the performance. Computation is involved by quantum gates in which no information loss. Reversible logic finds many applications in the era of quantum computing [2]. Bennett demonstrates that no energy dissipation is possible only if a circuit involved reversible gates [3].

The existing CMOS has been under constraints by the growing QCA technology as consider to high-speed operating frequency and low power are involved [4]. The cost and complexity of a QCA design are particularly affected by the cell count, area, and latency. Thus a great deal of forced the layout consideration has been developed for optimizing the complexity and better computation speed [5].

In the work, the synthesis of a reversible comparator using QCA technique is proposed. It would be important if the primitive's results used for layout design would be optimal. Existing comparator based on conventional logic based can still provide the design

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engineer with enough freedom to synthesize reversible logic design to best meet the energy free requirements of a specific application [6]. The reasons are, once there is designed by reversible gates in a circuit there must be quantum gates to compute the quantum information [7]. The circuit cost is determined by the figure of merits rather than by size order of gates considerations. The figure of merits is deal with the quantum cost, garbage output, ancilla inputs and gate count [8,9]. There is few number of research works on reversible comparator layout in QCA with provable better primitive's results. Although the reversible comparator in QCA concept is presented in [10,11] to used coplanar approach to checking the workability. This paper targets the QCA comparator circuit which can be implemented without crossover.

The major contributions of this work are summarized as follows:

1. A new gate named as universal reversible QCA gate (URQG) is proposed. It is a 3×3 gate that realizes 13 standard functions with optimal gate count.
2. The URQG gate is compared with the existing reversible gates using standard Boolean equations. The proposed gate outperforms the existing gates in terms of design cost and testing overhead.
3. Using the QCAPro tool, energy dissipation analysis is performed for the proposed gate.
4. Hardware description language for QCA (HDLQ) Verilog library is used to measure the fault tolerance attribute of the proposed gate.
5. A novel architecture of the n-bit reversible comparator structure is designed.

This paper is organized as follows. Section 2 describes the background of the QCA technology. Section 3 introduces the proposed model, and evaluates the performance of the proposed reversible gate. New efficient reversible comparator architecture is detailed in Section 4. Comparison results are illustrated in Section 5. Section 6 concludes the paper.

2. Background Study

The QCA is an emerging technology in which the logic states are not stored as voltage levels, but rather as the position of the individual electrons [12,13]. A QCA cell can be viewed as a set of four "dots" that are placed at the corner of a square. A quantum dot is the location of the cell in which a charge can be localized. The cell contains two extra mobile electrons, which can quantum mechanically tunnel between the dots. Owing to Coulomb repulsion, in the absence of external electrostatic, the electrons are forced to the corner positions to maximize their separation. As shown in Figure 1*a*, the QCA cell represents binary 1 and binary 0 configurations for the P = +1 and P = −1 polarization values, respectively.

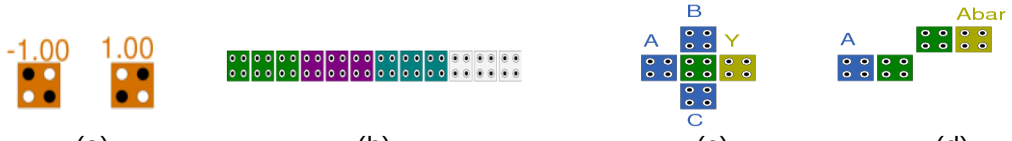


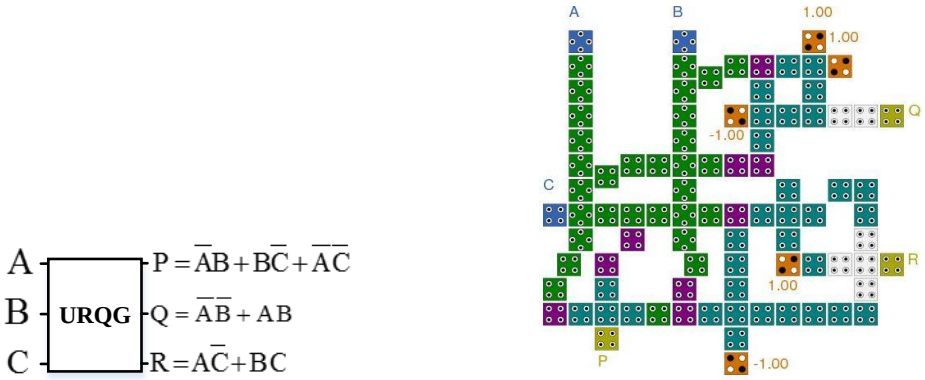
Figure 1. QCA Basics (a) QCA Cell (b) Binary Wire (c) Majority Voter (d) Inverter

The QCA operates by the Columbic interaction that connects the state of one cell to that of its neighbors, unlike the conventional logic circuits in which the information is transferred by electrical current. Figure 1*b* shows a binary wire with four-phase clock zones. In the binary wire, a signal propagates from the input to the output owing to the Columbic interactions between the cells. In a CMOS-based

system, timing is controlled by a reference signal (*i.e.*, a clock) and is mostly required for sequential circuits. However, timing in the QCA is necessary for both combinational and sequential circuits and is accomplished by clocking in four distinct periodic phases. The clocking provides power gains in the QCA as well as the control of information flow between the cells. Various types of QCA devices can be constructed using different physical cell arrangements. The two basic logic gates in the QCA are the majority voter and the inverter. The logic function of the majority voter is M (A, B, C) =AB + AC + BC, where A, B, and C are the three inputs. The majority voter can be realized using 5 QCA cells, as shown in Figure 1*c*. Further, AND, OR logic functions can be implemented by the majority voter by setting an input (control input) permanently to a "0" or "1" value. The inverter is shown in Figure 1*d*, where displacements of 45˚ in the two lines of the merging cells produce a complementary action of the input signals.

3. New Reversible URQG Gate

A 3x3 reversible gate named as URQG is designed in this section and is drawn in Figure 2a. The reversible truth table is listed in Table 1. Here it is proved that bijective mapping between inputs and outputs, hence it reversible. In focus to reversibility given the outputs logic P, Q, R the inputs A, B, C can be computed. The reversible URQG gate is a universal and implements 13 standard functions which are presented in Table 2. The QCA layout of the proposed URQG gate is illustrated in Figure 2b. It requires a total of six majority voters and four inverters. The present work is based on a four-phase clocking scheme, which is utilized in all the QCA circuits. All four clock zones are employed in this QCA layout.



(a) (b)

Figure 2. The Proposed URQG (a) Block Diagram (b) Cell Layout

Table 1. Truth Table of URQG Gate

A	B	C	P	Q	R
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	0	0	1
1	0	1	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1

The URQG gate is simulated using the QCADesigner tool. The simulation waveform of the proposed URQG gate is shown in Figure 3. It confirms that the proposed QCA

layout has achieved the desired functionality with a latency of one. The proposed gate is compared with all the existing QCA reversible gates. The analysis of the results reported in Table 3 indicates that the proposed URQG gate QCA implementation is efficient in terms of the QCA design metrics. It requires eighty-nine QCA cells and a delay of one clock, which is effective for designing larger circuits. It also covers a minimum area of 0.09 μm^2. Comparison graph for this implementation is shown in Figure 4.

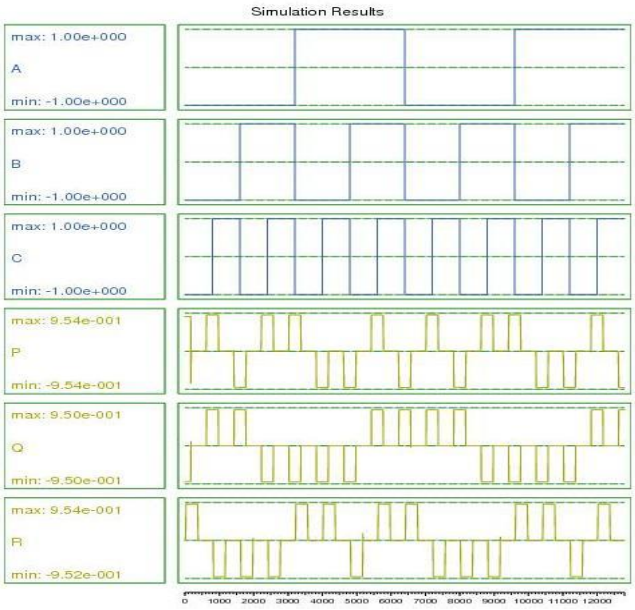


Figure 3. Simulation Results of the URQG Gate

Table 2. Comparison between the New URQG and the Existing Gates

Thirteen standard functions	**FRG [14]**	**PG [15]**	**RUG [16]**	**PPRG [17]**	**Proposed URQG**
Reversible/Nonreversible	Y/Y	Y/N	Y/N	Y/Y	Y/Y
ABC	2	2	2	2	2
AB	1	1	1	1	1
$ABC + \bar{A}\bar{B}\bar{C}$	3	3	2	2	3
$ABC + A\bar{B}\bar{C}$	4	4	3	3	2
AB+BC	2	2	2	2	2
$ABC + \bar{A}\bar{B}C$	5	3	3	2	2
$\bar{A}BC + \bar{A}\bar{B}\bar{C} + AB\bar{C}$	6	4	3	3	2
A	1	1	1	1	1
AB+BC+AC	5	4	1	2	2
$AB + \bar{B}C$	1	3	1	1	1
$AB + BC + \bar{A}\bar{B}\bar{C}$	6	1	2	2	2
$AB + \bar{A}\bar{B}$	2	1	1	2	1
$ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{A}B\bar{C}$	3	3	2	2	3

Table 3. Comparison between Proposed Gate Layout and the Existing Gate Layout

Reversible gates	Cell Count	Area (μm^2)	Latency	Total no. of gates For 13 standard Functions (G)
TR [9]	122	0.09	1	52
Fredkin [14]	246	0.37	1	41
RUG [16]	297	0.46	2	30
PPRG [17]	171	0.19	1	25
QCA1 [18]	147	0.16	0.5	29
RM [19]	224	0.25	1	28
Reversible gate [20]	90	0.09	1	26
URQG (proposed)	88	0.09	1	24

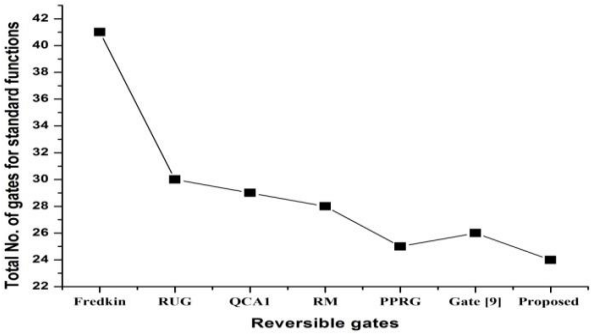


Figure 4. Comparison Graph for Implementing QCA Standard Functions

4.1. Power Dissipation

The total power dissipation of a QCA circuit is composed of two components: leakage and switching. The power losses during the clock alternations period and switching are termed as the leakage power and switching power, respectively [10]. In this section, a comprehensive power analysis and comparison of the proposed layout of the URQG with existing Fredkin gate [14], RM [21], PPRG [17] reversible gates are performed. The QCAPro tool is utilized as an adequate tool for estimating the power consumption of the structures at a 2K temperature under three different tunneling energy levels (0.5 E_k, 1.0 E_k, and 1.5 E_k). The power dissipation map for the URQG gate implementation is shown in Figure 5. The cells with higher power dissipation are distinguished using thermal hotspots with darker colors. The average leakage and switching energy dissipation of the proposed URQG implementations and the previously proposed reversible gates are listed in Table 4. The power analysis results indicate a significant efficiency obtained by our URQG design for both the switching and leakage energy dissipation criteria.

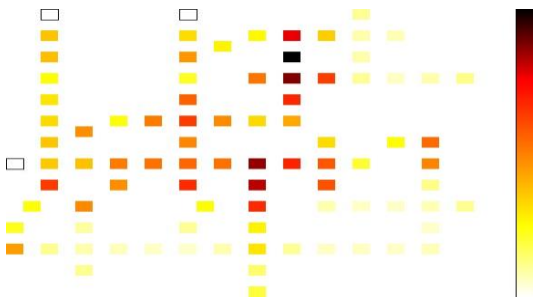


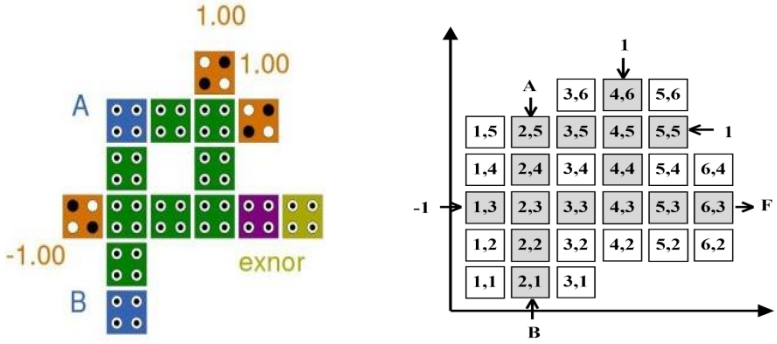
Figure 5. Power Dissipation Map of URQG Gate

Table 4. Energy Dissipation Results

Design	Leakage energy dissipation (eV)	Switching energy dissipation (eV)	Total energy dissipation (eV)
	$0.5E_k$ $1.0E_k$ $1.5E_k$	$0.5E_k$ $1.0E_k$ $1.5E_k$	$0.5E_k$ $1.0E_k$ $1.5E_k$
Fredkin [14]	0.101 0.283 0.482	0.213 0.175 0.143	0.314 0.458 0.625
PPRG [17]	0.058 0.168 0.294	0.193 0.166 0.141	0.251 0.334 0.435
RM [19]	0.117 0.318 0.534	0.309 0.251 0.205	0.426 0.569 0.739
New (URQG)	0.043 0.125 0.219	0.099 0.085 0.072	0.142 0.210 0.291

4.2. Fault Tolerance Analysis of URQG

In this section, the fault tolerant analysis of the URQG gate is performed. During the manufacturing of QCA circuits, defects are likely to occur. These defects are mainly due to missing and additional QCA cells [14]. Faults have been injected into the gate to validate the fault tolerance of the proposed URQG gate. Any QCA layout can be easily converted to the equivalent hardware description language notations by using the HDLQ Verilog library [15]. The library consists of majority voter (MV), inverter (INV), crosswire (CW), fan out (FO) and L-shaped wire (LS) with fault injection capability. The fault set and defect impact of these standard QCA devices are defined in [14, 15]. In the QCA layout of XNOR gate which is used in the proposed URQG gate layout Q output, as shown in Figure 6a, two number of majority voters are used. In this structure, the two outputs of majority voters are connected to a single line to produce the desired output. If multiple inputs are connected to a single line, it is called Fan-in at the inputs. The fault set and HDLQ model of this Fan-in structured QCA devices are not defined previously. In this Section, the fault set of XNOR gate QCA device shown in Figure 6a is established, through extensive simulation and the impact of the defects is evaluated. Input and output cells are located outside the layout of the device and a single missing or additional cell deposition defect is injected either in the original device or along the adjacency boundary, *i.e.*, no defect is injected for input/output cells. Figure 6b shows the cell layout of the XNOR gate and the locations of the possible cell deposition defects.



(a) (b)

Figure 6. Ex-Nor Gate (a)QCA Layout (b) Cell Positions

The two coordinates are used to identify the position of cells in the cartesian layout. Simulation results are reported in Table 5. C_M shows the coordinates of the missing cell deposition defect; C_A shows the coordinates of the extra cell deposition defect; Pmax denotes the highest magnitude polarization of F. This depicts the strength of the signal

between the highest polarization (1) and an extremely low polarization (0). All input values are applied with maximum polarization.

Table 5. Functionality of XNOR Gate under Cell Deposition Defects

C_M	F	Polarization		C_A	F	Polarization	
		P_{max}	P_{min}			P_{max}	P_{min}
1,3	1	+0.95	-0.81	1,1	$\overline{A \oplus B}$	+0.95	-0.95
2,1	$\overline{A}$	+0.95	-0.95	1,2	$\overline{A}$+B	+0.95	-0.95
2,2	-	-	-	1,4	$\overline{A \oplus B}$	+0.95	-0.95
2,3	1	+0.98	+0.38	1,5	$\overline{A \oplus B}$	+0.95	-0.95
2,4	0	+0.36	-0.95	2,6	$\overline{A \oplus B}$	+0.95	-0.95
2,5	0	+0.30	-0.95	3,1	$\overline{A \oplus B}$	+0.95	-0.95
3,3	1	+0.95	-0.89	3,2	A+B	+0.95	-0.95
3,5	$\overline{A \oplus B}$	+0.95	-0.95	3,4	A	+0.95	-0.98
4,3	0	+0.37	-0.95	3,6	$\overline{A \oplus B}$	+0.95	-0.95
4,4	0	+0.24	-0.95	4,2	$\overline{A}$+B	+0.95	-0.95
4,5	0	+0.25	-0.95	4,7	$\overline{A \oplus B}$	+0.95	-0.95
4,6	AB	+0.95	-0.95	5,2	$\overline{A \oplus B}$	+0.94	-0.94
5,3	-	-	-	5,4	1	+0.95	-0.53
5,5	$\overline{A \oplus B}$	+0.95	-0.95	5,6	$\overline{A \oplus B}$	+0.95	-0.95
6,3	$\overline{A \oplus B}$	+0.95	-0.95	6,2	$\overline{A \oplus B}$	+0.98	-0.98
				6,4	$\overline{A \oplus B}$	+0.98	-0.98

From Table 5 it is found that total six number of faults are possible by both single missing cell and additional cell deposition defects These six fault sets are {1, A', 0, AB, (A'+B), A}. In this work, we proposed a new HDLQ model of XNOR logic having this fault set. The HDLQ model design of the proposed URQG gate is shown in Figure 7. The model contains 21 elements (MV=4, INV=4, CW=3, FO=6, LS=3, proposed XNOR HDLQ model=1). An exhaustive testing is conducted for this model using eight input test vectors in the presence of all the possible missing or additional cell defects in MV, INV, CW, FO, LS, and proposed XNOR block. The number of fault patterns for MV, INV, CW, FO, LS, proposed XNOR block are 2,1,2,1,1,6 respectively [14, 15]. The design is simulated using Verilog HDL simulator which generates a total of 33 fault patterns, of which 26 fault patterns are unique for all the blocks, as shown in Table 6. In Table 6, a_i is a three-bit number with an equivalent decimal value of *i*. For example, a_6 represents 110 (*i.e.*, decimal 6). It is evident from Table 6 that for test vector a_3, the proposed gate exhibits the highest fault tolerance capability of 61 %. It also exhibits an overall fault tolerance capability of 51.12 % for all the test vectors, which indicates there is an average of 51.12% successful patterns that produce the correct output, even when there is a fault.

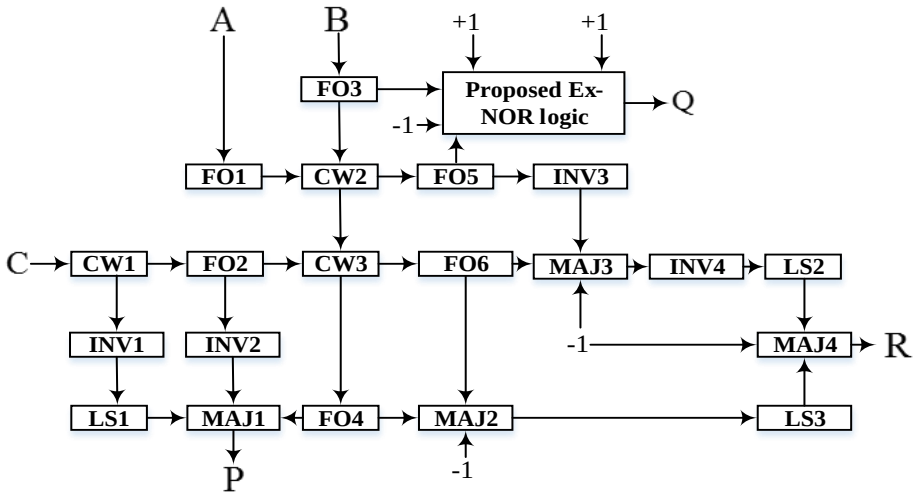


Figure 7. HDLQ Model of URQG Gate

Table 6. Fault Patterns in URQG

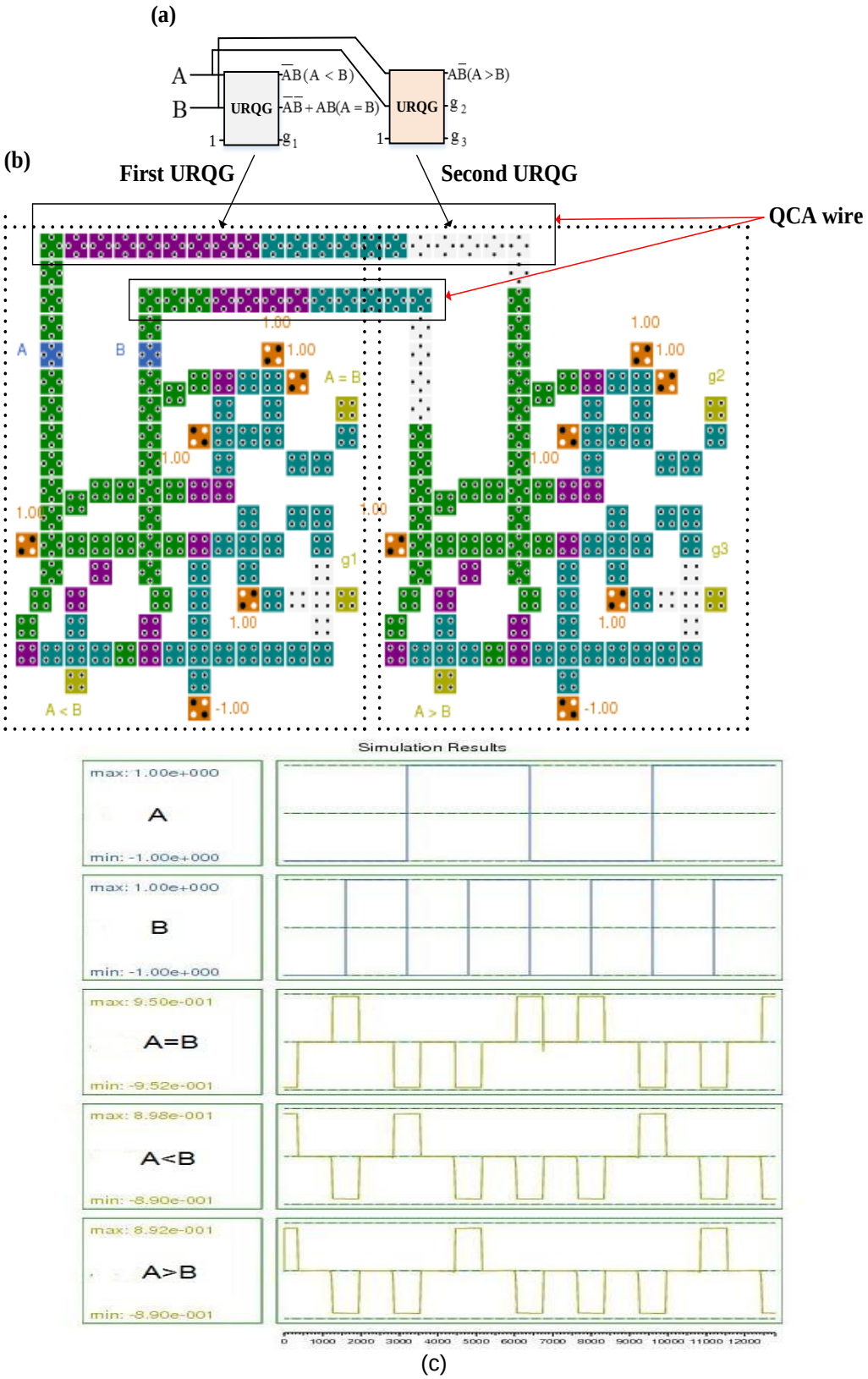
IV	EV	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
a_0	a_6	a_2	a_2	a_6	a_5	a_6	a_5	a_6	a_4	a_6	a_7	a_6	a_2	a_7	a_7	a_6	a_6
a_1	a_2	a_2	a_2	a_7	a_0	a_2	a_0	a_2	a_0	a_3	a_2	a_2	a_6	a_3	a_3	a_6	a_6
a_2	a_4	a_4	a_5	a_4	a_4	a_4	a_7	a_5	a_6	a_4	a_5	a_4	a_4	a_5	a_5	a_0	a_4
a_3	a_5	a_1	a_5	a_0	a_5	a_4	a_7	a_4	a_7	a_4	a_5	a_5	a_5	a_5	a_4	a_5	a_5
a_4	a_1	a_5	a_1	a_5	a_1	a_0	a_2	a_0	a_3	a_1	a_0	a_0	a_1	a_0	a_1	a_1	a_1
a_5	a_0	a_0	a_1	a_1	a_0	a_0	a_2	a_1	a_2	a_1	a_0	a_1	a_0	a_1	a_1	a_4	a_0
a_6	a_7	a_7	a_7	a_3	a_4	a_7	a_4	a_7	a_5	a_7	a_6	a_6	a_3	a_6	a_7	a_3	a_3
a_7	a_3	a_7	a_7	a_2	a_1	a_3	a_1	a_3	a_1	a_2	a_3	a_3	a_7	a_3	a_2	a_3	a_3

17	18	19	20	21	22	23	24	25	26	FT
a_7	a_6	a_7	a_7	a_4	a_6	a_4	a_4	a_6	a_6	42%
a_2	a_2	a_3	a_3	a_0	a_2	a_0	a_0	a_2	a_2	42%
a_5	a_5	a_5	a_5	a_6	a_4	a_4	a_4	a_4	a_6	46%
a_5	a_5	a_5	a_5	a_7	a_5	a_5	a_5	a_5	a_7	61%
a_1	a_1	a_1	a_1	a_1	a_1	a_1	a_1	a_3	a_3	57%
a_0	a_0	a_0	a_1	a_0	a_0	a_0	a_0	a_2	a_2	50%
a_7	a_7	a_7	a_7	a_7	a_7	a_7	a_5	a_5	a_7	54%
a_3	a_3	a_3	a_3	a_3	a_3	a_3	a_1	a_1	a_3	57%

IV= input vectors, EV= expected vectors, FT= fault tolerance in % , Average fault tolerance = 51.12 %

5. The Proposed Architecture of Reversible Comparator

By combining two URQG gates, a reversible one-bit comparator can be efficiently designed as shown in Figure 8a. In this circuit has two constant inputs and three garbage outputs. The QCA layout and simulation results of the proposed one-bit reversible comparator are shown in Figure 8*b* and Figure 8*c*, respectively. From the simulation results, it is evident that the delay is 0.75 clocks. This reduced delay is possible because of both the proposed gates in the comparator function independently and the output R is not used in the comparator structure.



(c)

Figure 8. One-bit Reversible Comparator (a) Block Diagram (b) QCA Layout (c) Simulation Result

Table 7 compares the existing one-bit reversible QCA comparator [6] with the proposed one-bit comparator. The proposed comparator structure can be extended to any number of bits (*i.e.*, n). Accordingly, a proposed one-bit comparator cell is designed. This cell compares the outputs of the previous stage with the current inputs and produces three outputs. In a one-bit comparator cell, five URQG gates and two Feynman gates are used, wherein the latter is employed for the addition of two input numbers. The structure of a two-bit reversible comparator using a one-bit comparator and a one-bit comparator cell is shown in Figure 9a. Further, the first stage produces the output of the comparison of the two most significant bits (MSB) of the inputs A and B. The second stage is a one-bit comparator cell, which compares the outputs of the first stage with A_0 and B_0 and presents the final results. The Boolean expressions for the two-bit comparator are shown by equation (1) to (3).

$$(A<B) = (A_{n-1} < B_{n-1}) + (A_{n-1} = B_{n-1})\times(A_{n-2} < B_{n-2}), \quad (1)$$

$$(A>B) = (A_{n-1} > B_{n-1}) + (A_{n-1} = B_{n-1})\times(A_{n-2} > B_{n-2}), \quad (2)$$

$$(A=B) = (A<B) \text{ xnor } (A>B). \quad (3)$$

The general structure of the n-bit comparator structure is shown in Figure 9b. It is shown that for a comparator structure of size n bits, a one-bit comparator and (n-1) number of one-bit comparator cells is needed. In Figure 10, QCA layout of 2-bit comparator is illustrated. It requires 1302 cells with an area of $2\mu m^2$. The QCA design analysis of n-bit comparator structure is detailed in Table 8.

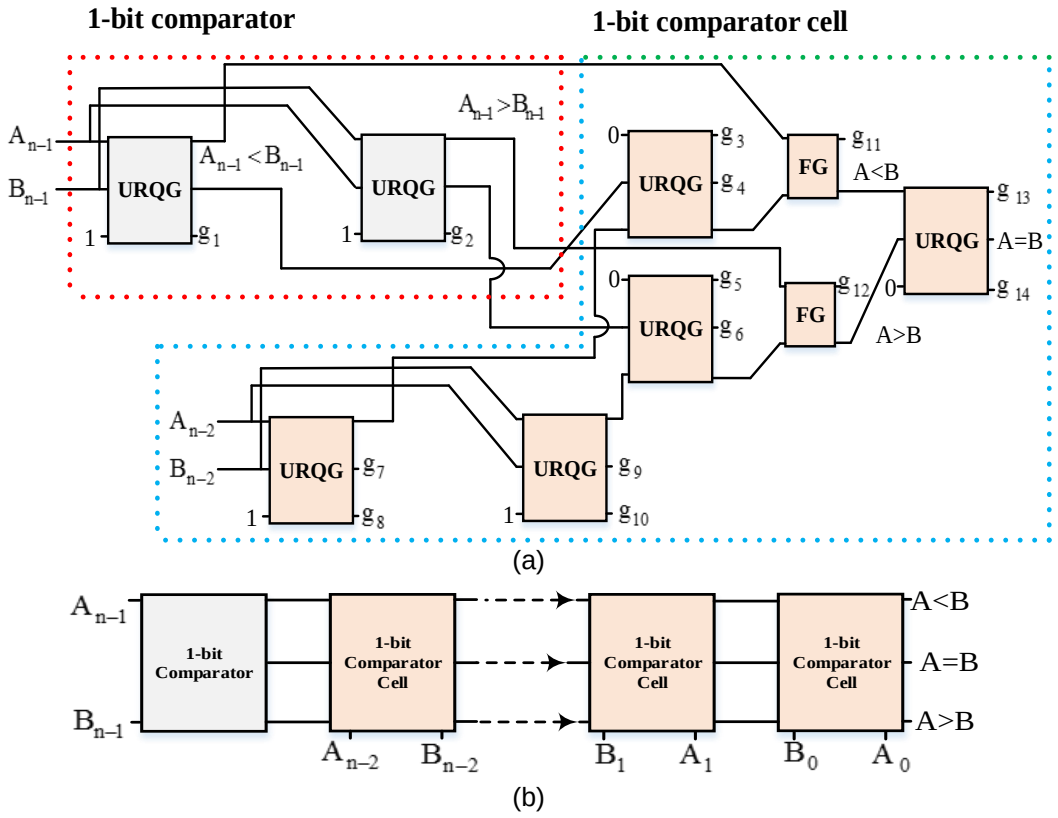


Figure 9. The Proposed Design of Reversible Comparator (a) 2-bit (b) n-bit

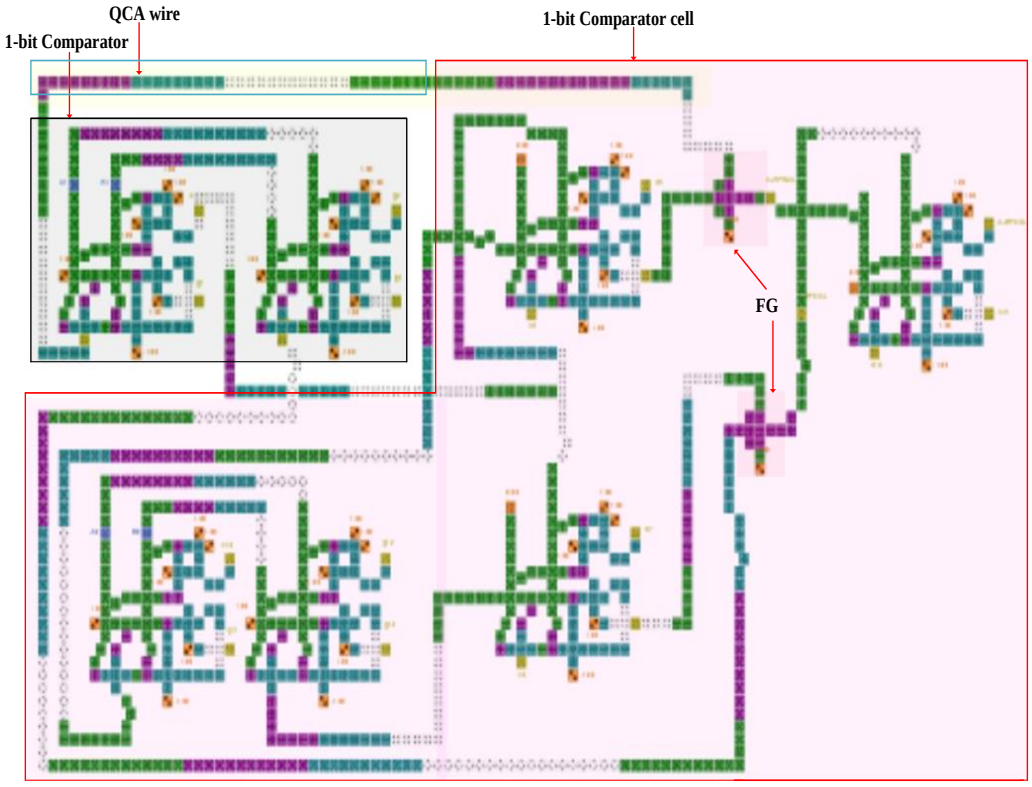


Figure 10. QCA Layout of 2-bit Reversible Comparator Structure

6. Comparision Results and Discussion

The cost comparison has been developed by the proposed layout of the 1-bit reversible comparator and the optimized primitives results have been calculated. The results from the proposed methodology of the layout are in good agreement with the targeted results. Thus the constructed layout of these designs is validated by the simulation result and thus the complexity meet the current nanoelectronics application. The complexity of proposed 1-bit comparator is 31.03% less compare to [9]. We can compute the area is 0.23 μm^2 (32.35%) less than [9], similarly for present layout latency is 0.75 (75%) less than existing design in [9]. Hence it can be said this design of 1-bit reversible comparator is giving compact layout and minimum latency as compared to existing work in [9]. This result is really interesting and encouraging. Table 8 show different size order comparator results in terms of gate used majority gate, the number of the inverter, and area.

Table 7. Cost Comparison of Proposed 1-bit Reversible Comparator

Design	Cell Count	Area (μm^2)	Latency	Quantum cost [6] (Area× Latency^2)
Existing [9]	319	0.34	3.0	3.087
Proposed	220	0.23	0.75	0.129
Improvement in % over [9]	31.03%	32.35%	75%	95.82%

Table 8. QCA Structure Analysis of n-bit reversible Comparators

Design	No. of URQG gates	No. of FG	No. of majority voters	No. of inverters	Total Area
1-bit comparator cell	5	2	34	20	2.01 μm^2
1-bit reversible comparator	2	0	12	08	0.129 μm^2
2-bit reversible comparator	7	2	46	28	2.05 μm^2
3-bit reversible comparator	12	4	80	48	4.15 μm^2
4- bit reversible comparator	17	6	114	68	6.22 μm^2
n-bit reversible comparator	5×(n-1)+2	2×(n-1)	6×(5×(n-1)+2) + 2×2(n-1)	4×(5×(n-1)+2)	-

7. Conclusion

In this work, we have described a 1-bit reversible comparator in QCA that uses a replica of URQG layout to design construction. This layout of 1-comparator again cascaded to 1-bit comparator cell layout to the construction of 2-bit comparator. The QCA wire is used to join this two layout and perform the required logic computation. We also showed that generic n-bit comparator architecture that was used some proposed modules cells to synthesize architecture. However, it has achieved in the layout design of 1-bit and 2-bit comparator that requires 220 cell count, and 2.05 μm^2 area on average. The use of reversible technology in combination with QCA, *i.e.*, reversible-QCA comparator seems to be an attractive solution for future nanoelectronics systems.

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Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of this article.

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