International Journal of Grid and Distributed Computing
Vol. 10, No. 5 (2017), pp.13-24
http://dx.doi.org/10.14257/ijgdc.2017.10.5.02

An Efficient Design of Reversible Subtractor in Quantum-Dot Cellular Automata

Provash Kumar Biswas[1], Ali Newaz Bahar[1*], Md. Ahsan Habib[1], Nur Mohammad Nahid[1] and Mohammad Maksudur Rahman Bhuiyan[2]

[1]*Department of Information and Communication Technology, Mawlana Bhashani Science and Technology University, Tangail, Bangladesh*
[2]*University Grants Commission of Bangladesh, Dhaka, Bangladesh*
**bahar_mitdu@yahoo.com*

Abstract

Quantum-dot cellular automata (QCA) is a beneficial technology which is counted as one potential replacements for typical complementary metal-oxide-semiconductor (CMOS) archetype. QCA has excessive expedient thickness, particular performance speed with exceptionally low power depletion. Researchers have viewed plentiful devices of QCA based logic circuits though, yet not sufficient effort has been appraised on QCA based binary subtractor. This study outlined an optimized reversible binary half and full subtractors with power depletion analysis. The proposed reversible half subtractor has been designed using only 40 cells and occupied 0.0556 μm^2 area. Besides, reversible full subtractor requires only 73 cells and occupies only 0.0831 μm^2 areas. Moreover, the presented half and full subtractor dissipates only 36.78 meV and 81.56meV energy at 0.5 E_k tunneling energy level, respectively. The proposed circuits have been simulated and verified using QCADesigner, an extensively used simulation engine. The proposed layout can be operated to realize the nanoscale computing scheme in communication throughout minimal power utilization.

Keywords*: Quantum-dot cellular automata, Reversible subtractor, Efficient QCA design, 3-input XOR gate*

1. Introduction

Through the previous few eons, affluent the reputation aspect with growing the outstanding power have been efficiently flourished by feasible lithography devised organized on VLSI archetype [1]. However, the condition look like traditional because of dropping the transistor scopes, particular hitches as by way of excessive power utilization with difficulties in distinction outline reduction cannot be unnoticed. Recent survey estimates that CMOS outfits may well perception somatic excelling limits trailblazing 2012 and will be outmoded by precise advancing technologies [2]. Nanotechnology is an alternative direction for these hitches; furthermore the ITRS report a few viable models. Depend on the matching aspect of microelectronic fashions succeeding to nanoscale status significance, nanotech form a perfect circumstance azimuth for itemize systems. QCA is an emergent archetype which offers an advanced method for logic circuits [3-6]. QCA proposed an enhanced comprehensive computational function by the lateral of the nanoscale [7-9] through modifying the fact of a precise electron of this archetype promise advance minimal power, extreme rapidity with particularly compact circuits. Reversible logic gates such as Toffoli gate [10], Double Feynman gate (F2G) [11], Peres gate [12], Fredkin gate [13] and Multiply Complements Logic [14] gates have been designed in QCA. This study proposes a unique and advanced subtractor circuit in QCA. The QCA

* Corresponding Author

ISSN: 2005-4262 IJGDC

based subtractor was first proposed in [15]. This irreversible subtractor involved 178 cells and engaged 0.205μm^2 space. Another QCA based subtractor has been presented in [16] that involved 136 QCA cells. An improved layout of complete subtractor has been organized in [17] engaged 104 cells. DG gate based reversible subtractor has been denoted in [18] which involves 247 QCA cells. In this study, an efficient reversible half and full subtractor have been presented using a novel 3-input XOR gate [19].

2. Fundamental Overview of QCA

QCA configuration of four quantum dots is presented in the following Figure 1. The dots organized to keep electrons within it and these dots are combined within the channeling wire [1-2]. The electrons are organized to the threshold positions for coulombic revulsion. Depending on the site of the electrons, each cell has two arrangement of polarization. Logic '1' or P= +1 and logic '0' or P= -1 are two sorts of electrons polarization [1] as presented in Figure 1.

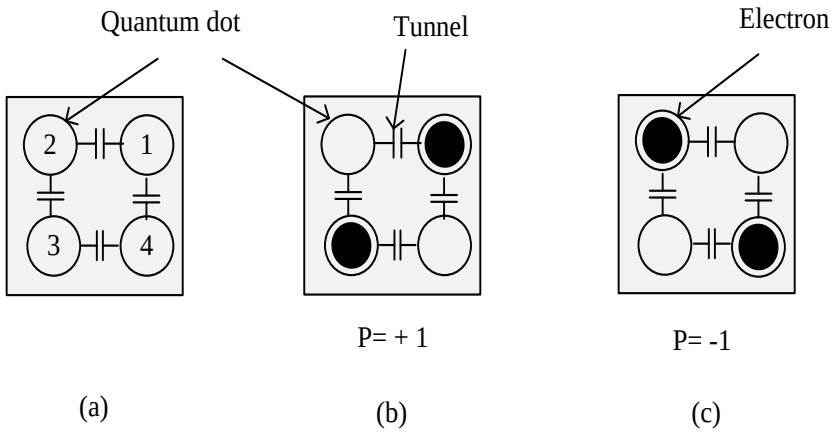


Figure 1. (a) Basic Four dot QCA Cell (b) Binary "1" or Polarizations P=+1 (c) Binary "0" or Polarizations P=-1

Groups of cells can be ordered to realize QCA wire along with all logical functions [1-3]. The electrons retain the reverse place polarization due to their common electrostatic counter-enticement. Whereas, QCA inverter has been used to change the inputs polarization to the opposites polarization as shown in Figure 2 (b).

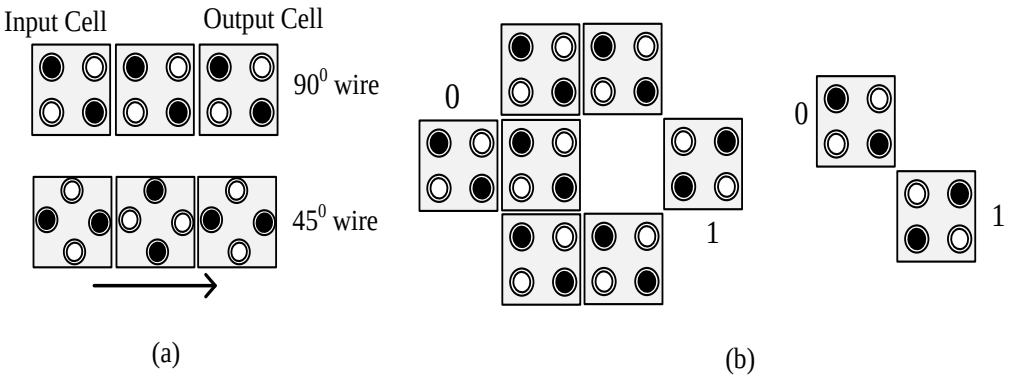


Figure 2. Different Types of QCA (a) Wire and (b) Inverter

The simplest conformation of the inverter, succeeding in Figure 2(b), is mostly complete withholding the cells simply with their junctions emotive. The basic logical unit in QCA is majority voter gate. Three input majority voter (MV_3) gate consists of five cells; three inputs, one output and a middle cell [3]. The middle cell named device cell by reason of its function, switches to major polarization and determines the stable output. Majority gate can be programmed such that it functions as a 2-input AND or a 2-input OR by fixing one of the three input cells to p = -1 or p = +1 respectively as shown in Figure 3.

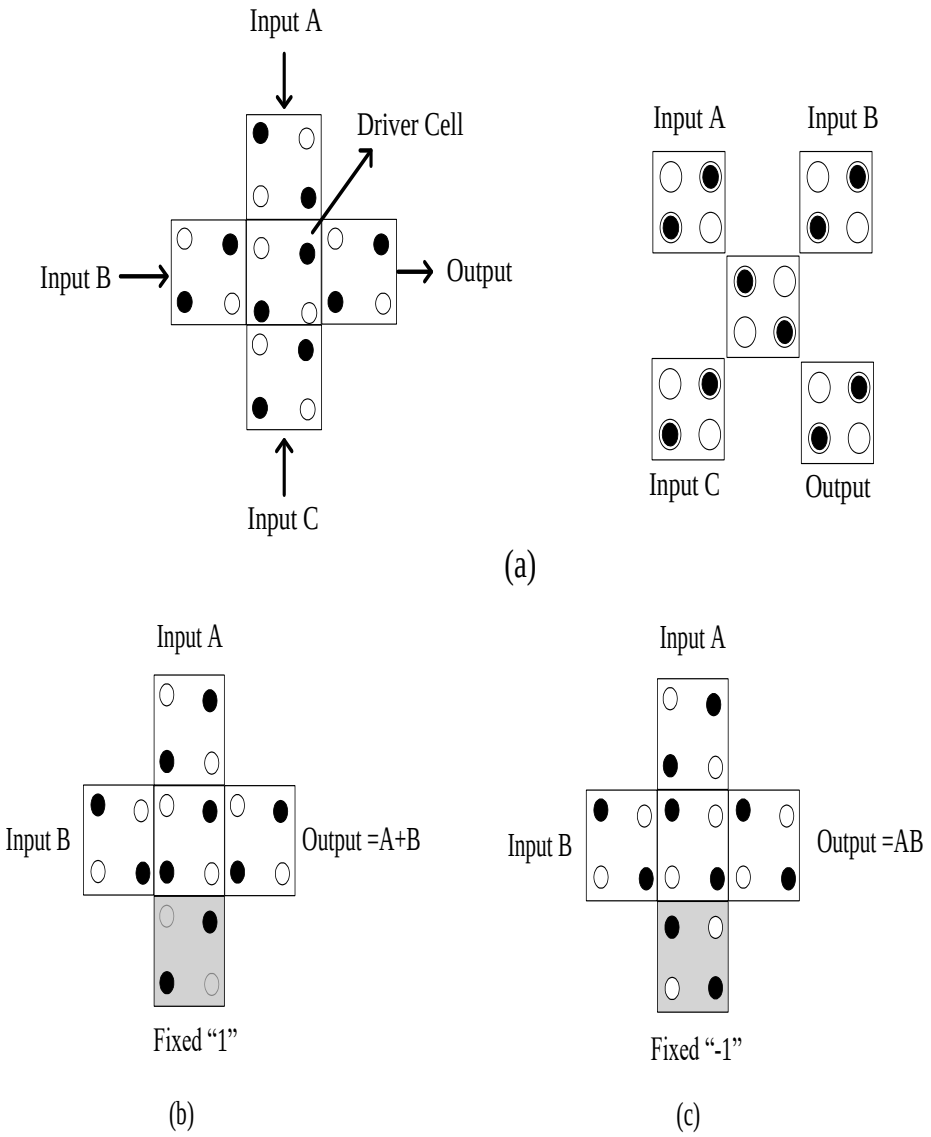


Figure 3. Basic Design of QCA (a) Three Input Majority Gate (b) Programmed as OR Gate (c) Programmed as AND Gate

3. Proposed Circuit

3.1. TR Gate

TR gate is a 3x3 reversible gate was first in [20] and QCA representation of this gate was introduced in [21, 22]. If the three inputs are I_0, $I_1$and I_2, then outputs are mapped as $O_0=I_0$, $O_1=I_0 \oplus I_1$ and $O_2=I_0 I'_1 \oplus I_2$. The block diagram and QCA circuit layout of TR gate is shown in Figure 4.

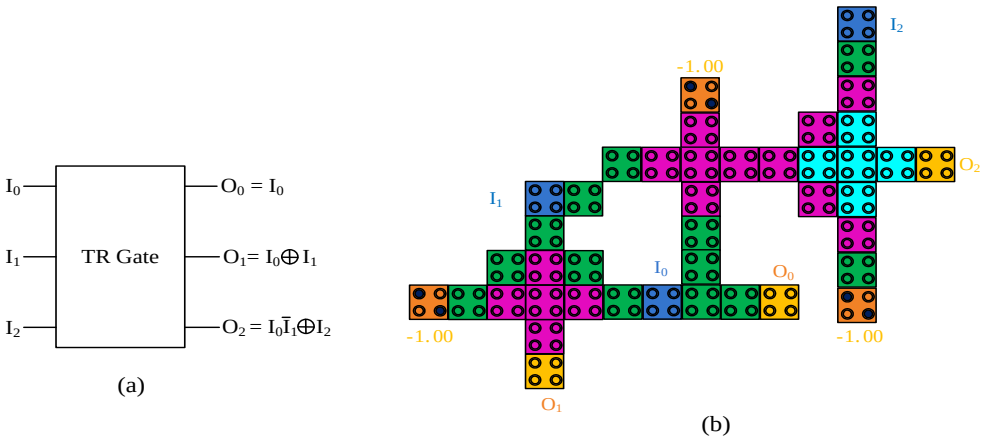


Figure 4. (a) Block Diagram and (b) QCA Circuit Layout of TR Gate

3.2. Half Subtractor

Reversible half subtractor is a 2x2 circuit. Let, the inputs are I_0 and I_1 then the outputs are defined as $G_{out} = I_0$, $Diff = I_0 \oplus I_1$ and Borr = $I'_0 I_1$.The truth table of proposed reversible half subtractor is mentioned in Table 1. Here, the proposed half subtractor has been designed using TR gate. The proposed reversible half subtractor utilizes only 40 QCA cells and the outputs are generated after a delay of 0.75 clock cycle; circuit layout is shown in Figure 5 (a).

Table 1. Truth Table of Preversible Half Subtractor

Input		Output		
I_0	I_1	G_{out1}	Diff	Borr
0	0	0	0	0
0	1	1	1	1
1	0	0	1	0
1	1	1	0	0

Reversible full subtractor contains three inputs I_0, $I_1$and I_2, and four outputs Diff, Borr, G_{out1} and G_{out2}. The logical expressions of difference and borrow are $Diff = I_0 \oplus I_1 \oplus I_2$ and $Borr = I'_0 I_1 + (I_0 \oplus I_1)' I_2$. The truth table of proposed reversible full subtractor is mentioned in Table 2 and the block diagram is given in Figure 5 (b).

Table 2. Truth Table of Proposed Reversible Full Subtractor

Input			Output			
I_0	I_1	I_2	G_{out1}	G_{out2}	Diff	Borr
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	1	0	1	1
0	1	1	1	1	0	1
1	0	0	0	0	1	0
1	0	1	0	1	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

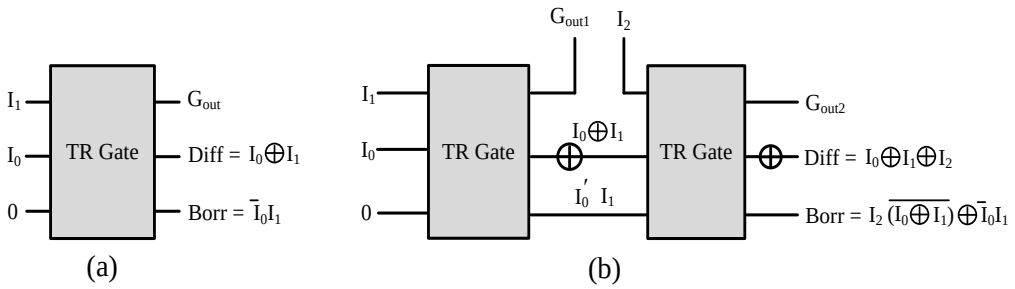
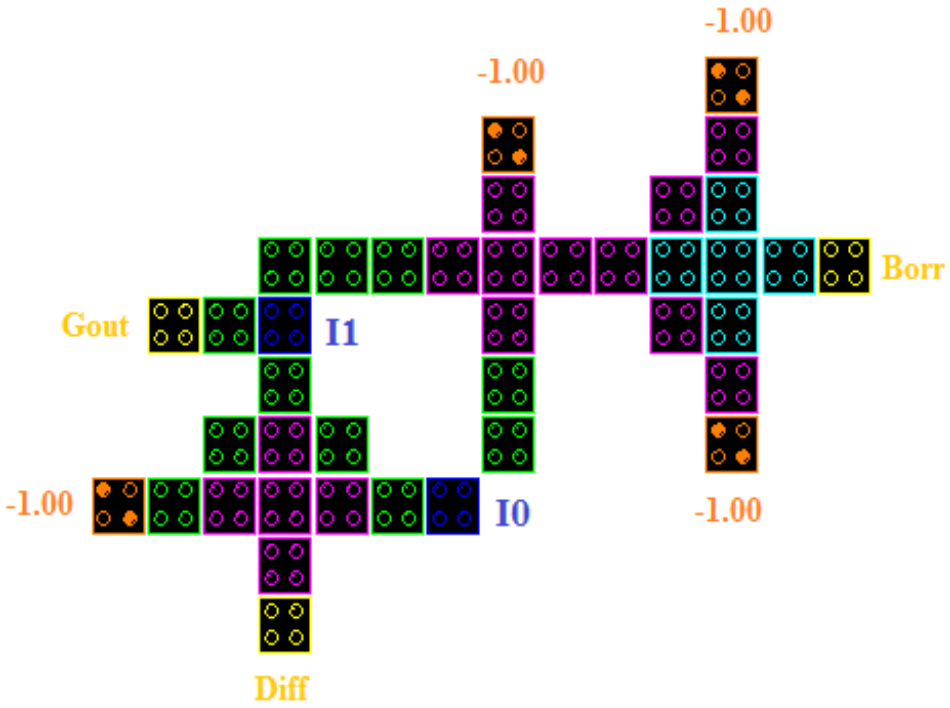


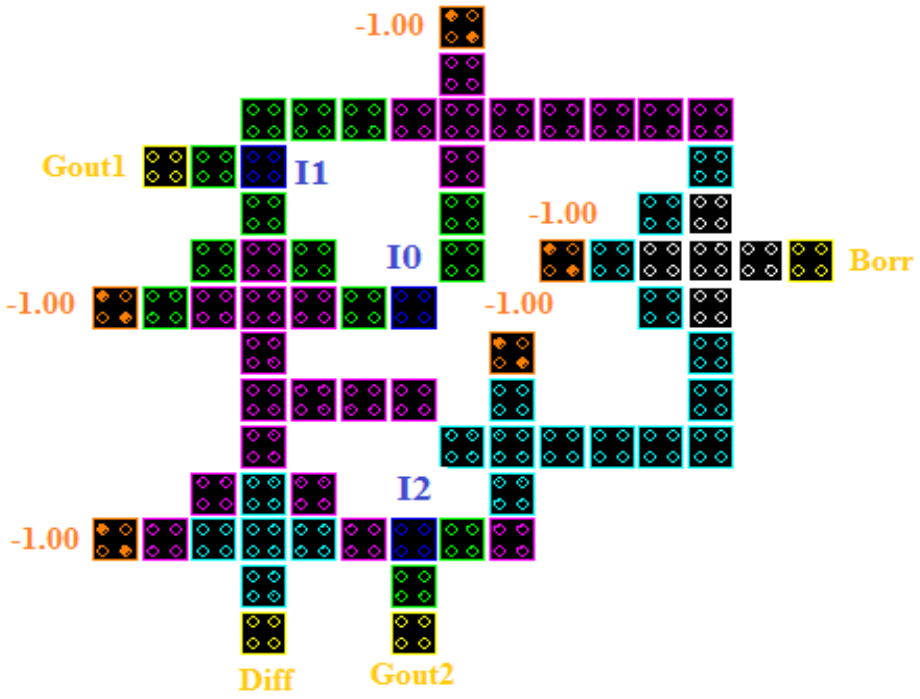
Figure 5. Block Diagram of Proposed Reversible (a) Half Subtractor and (b) Full Subtractor

4. Simulation and Results Analysis

QCADesigner has been employed as a simulation tool [23] to simulate the proposed reversible full subtractor. Moreover, proposed circuit is verified using theoretical values. The following parameters are applied during simulation: radius of effect 65.00 nm, cell width 20 nm, cell height 20 nm, number 10000, relative permittivity 12.900, clock low $3.80000e^{-23J}$, clock high 9.80000 e^{-22J}, clock amplitude factor 2.0000, convergence tolerance 0.001000, and highest iterations per sample 80000.



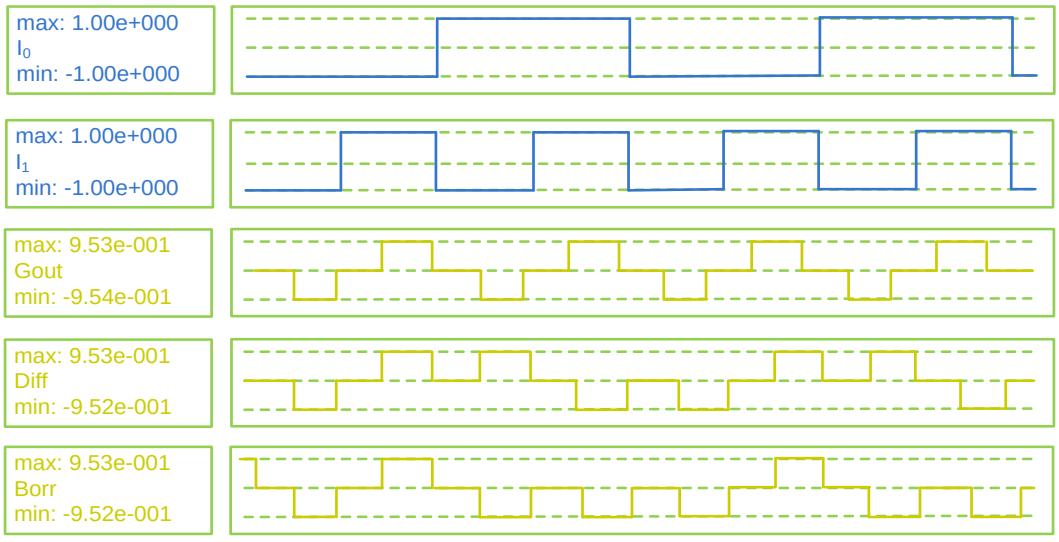
(a)



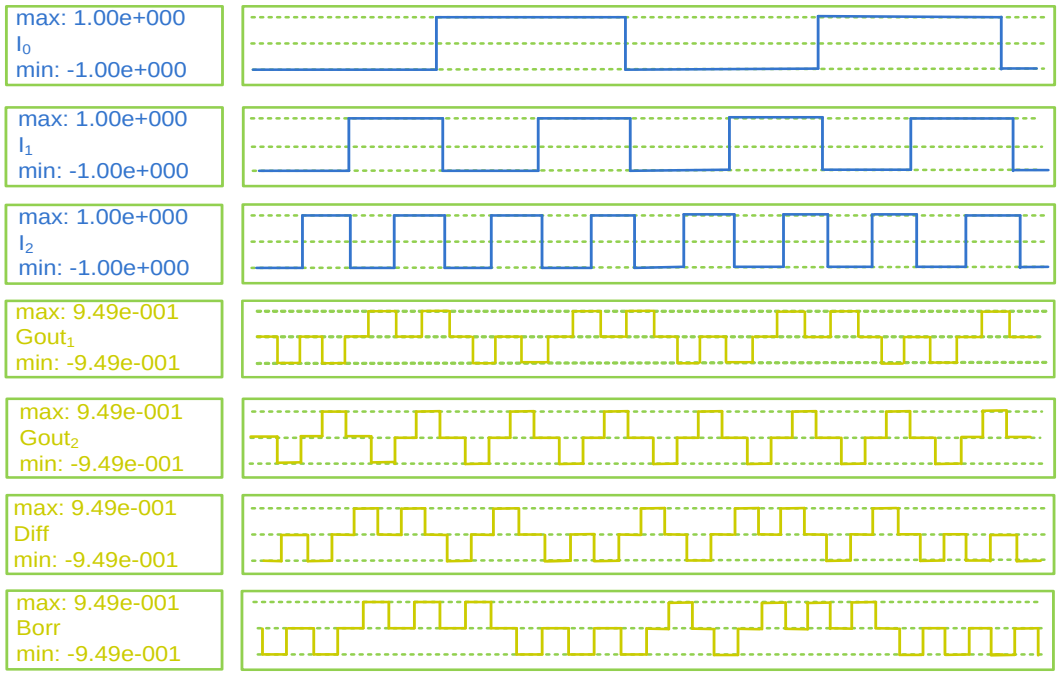
(b)

Figure 6. QCA Circuit Layout of Proposed Reversible (a) Half Subtractor and (b) Full Subtractor

The simulated circuit layout of proposed half and full subtractor is shown in Figure 6. The proposed half subtractor organized using a novel XOR gate with single layer 44 QCA cells, time delay 0.75 clock cycle and covered area around 0.0556 μm^2. Besides, the proposed half subtractor is designed using 73 cells only, 4-clock phase with an extent of around 0.0831 μm2. A brief comparison of proposed design and previous design is given in Table 3.



(a)



(b)

Figure 7. Simulated Input-output Signal of Proposed Reversible (a) Half Subtractor and (b) Full Subtractor

The outcome of the simulation of the outlined reversible half subtractor is in Figure 7 (a). The result shows that if input pin $I_0 = 0$ and $I_1 = 0$ then the outcome will be $G_{out1} = 0$, $Diff = 0$ and $Borr = 0$. When $I_0 = 0$ and $I_1 = 1$, then the consistent outcome will be $G_{out1} = 1$, $Diff = 1$ and $Borr = 1$, and so on. Similarly, the output of reversible full subtractor shown in Figure 7 (b) is matched with the theoretical values given in Table 2.

Table 3. Comparison Results of Proposed Reversible Half and Full Subtractor with Previous Work

Circuit	Type of Subtractor	Number of cells	Approximated area (μm^2)	Latency (clock cycle)
Half Subtractor [15]	irreversible	77	0.0896	0.75
Half Subtractor [16]	irreversible	55	0.0504	0.75
Half Subtractor [17]	irreversible	45	0.0356	0.75
Half Subtractor [18]	reversible	125	0.104	1.0
Proposed Half Subtractor	reversible	40	0.0556	0.75
Full Subtractor [15]	irreversible	178	0.205	2.0
Full Subtractor [16]	irreversible	136	0.168	1.75
Full Subtractor [17]	irreversible	104	0.1043	1.75
Full Subtractor [18]	reversible	247	0.257	2.0
Proposed Full Subtractor	reversible	73	0.0831	1.0

From the above table, it is observed that our proposed reversible subtractor leads all types of earlier reported subtractor in terms of cell count, covered area and latency. Our reported half subtractor required only 40 cells where 125 cells are used in [18] to design the reversible half subtractor. Similarly, the proposed reversible

full subtractor occupies 0.083μm^2 area where previous reversible design [18] occupied 0.257 μm^2 area.

5. Power Analysis

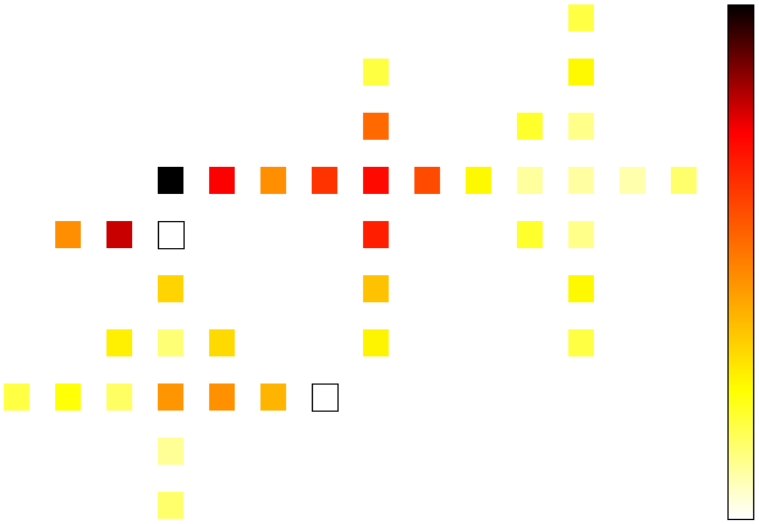
The energy dissipation by a cell is given as

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}\cdot\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}\right] = P_1 + P_2$$

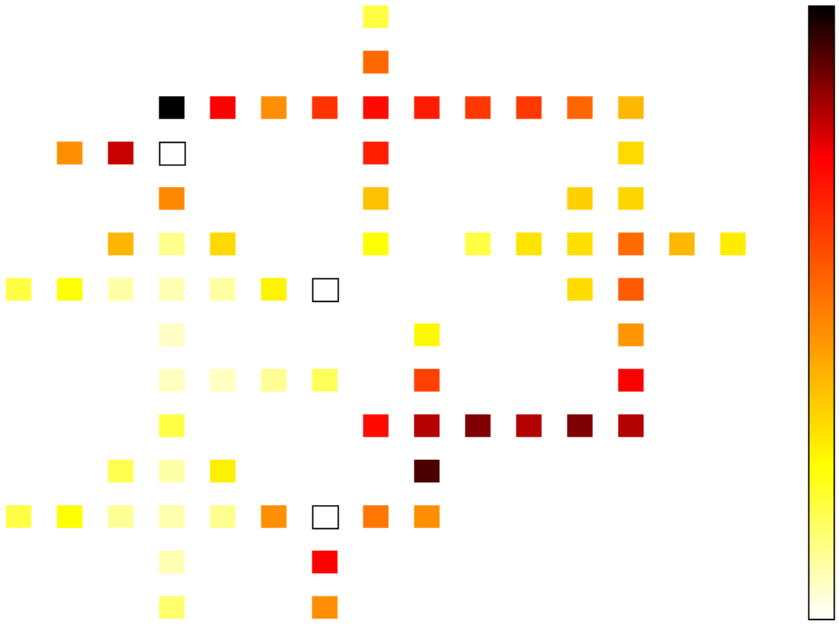
where, P_1 combines the difference of input and output signal powers and clocking power to the cell and the P_2 is the dissipated power (P_{diss}). The dissipated power is calculated using a power estimation tool known as QCAPro [24]. This helps to evaluate the total power loss in a QCA circuit as a combination of leakage and switching power [25]. Table 4 lists the energy dissipation results of proposed gates at three different tunneling energy levels (0.5 E_k, 1.0 E_k, 1.5 E_k) at *2K* temperature. The power dissipation map of the proposed reversible half and full subtractor are shown in Figure 8 under energy level of 0.5 E_k; where higher power dissipation are distinguished by darker colors in the thermal hotspot map.

Table 4. Energy Dissipation Analysis of Proposed Gates at Three Different Tunnelling Energy Levels at *2K* Temperature

	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)			Total energy dissipation (meV)		
Circuits	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k
Half Subtractor	15.57	41.71	70.33	21.21	18.38	15.84	36.78	60.09	86.17
Full Subtractor	25.62	72.62	125.54	55.94	47.16	39.46	81.56	119.78	165.0



(a)



(b)

Figure 8. Power Dissipation Map for the Proposed Reversible (a) Half Subtractor and (b) Full Subtractor at *2K* Temperature and Tunneling Energy of 0.5 E_k

6. Conclusion

In this study, a novel reversible binary half and full subtractor have been developed with QCA archetype. The simulation results resolve that all the designs are effective and fashioned appropriate outcomes. The proposed designs are improved besides cost effective than available ones that the presence of current technology. Besides, the circuit structure is very simple and did not utilize any rotated, translated QCA cells, and offer single layer accessibility to their inputs and outputs. Presented reversible half and full subtractors reduced area complexity by 46% and 68% respectively. This study can be capable to show a meaningful commitment to the QCA-based logic denomination, along with layout and performance of binary subtractors.

References

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, "Quantum Cellular Automata." Nanotechnology, vol. 4, no. 1, **(1993)**, pp. 49-57.
[2] P. D. Tougaw, and C. S. Lent, "Logical devices implemented using quantum cellular automata" Journal of Applied Physics, vol. 75, no. 3, **(1994)**, pp.1818–1825.
[3] I. Amlani, A. O. Orlov, G. Toth, G. H. Bernstein, C. S. Lent and G. L Snider, "Digital logic gate using quantum-dot cellular automata", Science, vol. 284, no. 5412, **(1999)**, pp. 289-291.
[4] M. Abdullah-Al-Shafi and A. N. Bahar, "Novel Binary to Gray Code Converters in QCA with Power Dissipation Analysis", International Journal of Multimedia and Ubiquitous Engineering, vol. 11, no. 8, **(2016)**, pp. 379-396.
[5] M. Abdullah-Al-Shafi and A. N. Bahar "QCA: An Effective Approach to Implement Logic Circuit in Nanoscale", 5th International Conference on Informatics, Electronics & Vision (ICIEV), **(2016)**, pp. 620-624.
[6] A. N. Bahar, M. A. Habib and N. K. Biswas, "A novel presentation of toffoli gate in Quantum-dot Cellular Automata (QCA)", International Journal of Computer Applications, vol. 82, no. 10, **(2013)**, pp. 1-4.

[7] V. Vedral, A. Bareno and A. Ekert, "Quantum networks for elementary arithmetic operations", Physical Review A, vol. 54, no. 1, **(1996)**, p. 147.
[8] M. Abdullah-Al-Shafi and A. N. Bahar, "Optimized design and performance analysis of novel comparator and full adder in nanoscale", Cogent Engineering, vol. 3, no. 1, **(2016)**, pp.1237864.
[9] S. Islam, M. A. Shafi and A. N. Bahar, "Implementation of Binary to Gray Code Converters in Quantum Dot Cellular Automata", Journal of Today's Ideas – Tomorrow's Technologies, vol. 3, no. 2, **(2015)**, pp. 145-160.
[10] A. N. Bahar, M. S. Uddin, M. Abdullah-Al-Shafi, M. M. R. Bhuiyan, and K. Ahmed, "Designing Efficient QCA Even Parity Generator Circuits with Power Dissipation Analysis", Alexandria Engineering Journal, **(2017).**
[11] A. N. Bahar, S. Waheed, M. A. Uddin and M. A. Habib, "Double Feynman Gate (F2G) in Quantum-dot Cellular Automata (QCA)", International Journal of Computer Science Engineering, vol. 2, no. 6, **(2013)**, pp. 351-355.
[12] A. Sarker, A. N. Bahar, P. K. Biswas and M. Morshed, "A novel presentation of Peres Gate (PG) in Quantum-dot Cellular Automata (QCA)", European Scientific Journal, vol. 10, no. 21, **(2014)**, pp. 101-106.
[13] A. N. Bahar, S. Waheed, and M. A. Habib, "An Efficient Layout Design of Fredkin Gate in Quantum-dot Cellular Automata (QCA)", Düzce Ü niversitesi Bilim ve Teknoloji Dergisi, vol. 3, no. 1, **(2015)**, pp. 219–225.
[14] S. S. Islam, S. S. Farzana and A. N. Bahar, "Area efficient layout design of Multiply Complements Logic (MCL) gate using QCA technology", Global Journal of Research in Engineering, vol. 14, no. 4, **(2014)**, pp. 7-10.
[15] S. K. Lakshmi, G. Athisha, M. Karthikeyan, and C. Ganesh, "Design of subtractor using nanotechnology based QCA", In Communication Control and Computing Technologies (ICCCCT), 2010 IEEE International Conference on IEEE. **(2010)**, pp. 384-388.
[16] H. Dallaki, and M. Mehran, "Novel Subtractor Design Based on Quantum-Dot Cellular Automata (QCA) Nanotechnology", International Journal of Nanoscience and Nanotechnology, vol. 11, no. 4, **(2015)**, pp. 257-262.
[17] J. I. Reshi, and M. T. Banday, "Efficient Design of Nano Scale Adder and Subtractor Circuits using Quantum dot Cellular Automata", in: 3rd International Conference on Electrical, Electronics, Engineering Trends, Communication, Optimization and Sciences (EEECOS), **(2016)**, pp. 89–94.
[18] J. C. Das, and D. De, "Reversible binary subtractor design using quantum dot-cellular automata", Frontiers of Information Technology & Electronic Engineering, **(2016)**.
[19] A. N. Bahar, S. Waheed, N. Hossain, and M. Asaduzzaman, "A Novel 3-Input XOR Function Implementation in Quantum-Dot Cellular Automata with Energy Dissipation Analysis." Alexandria Engineering Journal, vol. 56, **(2017)**.
[20] H. Thapliyal, and N. Ranganathan, "Design of efficient reversible binary subtractors based on a new reversible gate", VLSI, 2009. ISVLSI'09. IEEE Computer Society Annual Symposium on, IEEE, **(2009)**, pp. 229-234.
[21] A. N. Bahar, M. M. Rahman, N. M. Nahid and M. K. Hassan, "Energy dissipation dataset for reversible logic gates in quantum dot-cellular automata", Data in Brief, vol. 10, **(2017)**, pp. 557–560.
[22] A. N. Bahar, S. Waheed and N. Hossain, "A new approach of presenting reversible logic gate in nanoscale", SpringerPlus, vol. 4, no. 1, **(2015)**, p. 153.
[23] K. Walus, T. J. Dysart, G. A. Jullien and R. A. Budiman, "QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata", IEEE transactions on Nanotechnology, vol. 3, no. 1, **(2004)**, pp. 26-31.
[24] S. Srivastava, A. Asthana, S. Bhanja, and S. Sarkar, "QCAPro - An Error-Power Estimation Tool for QCA Circuit Design." In 2011 IEEE International Symposium of Circuits and Systems (ISCAS), (2011) 2377–80.
[25] M. Abdullah-Al-Shafi, A. N. Bahar, P. Z. Ahmad, F. Ahmad, M. M. R. Bhuiyan, and K. Ahmed, "Power Analysis Dataset for QCA Based Multiplexer Circuits." Data in Brief, vol. 11, **(2017)**, pp. 593–596.

Authors

Provash Kumar Biswas received his B.Sc. (Engineering) in Computer Science and Engineering from Mawlana Bhashani Science and Technology University (MBSTU), Tangail-1902, Bangladesh in 2009. He is currently pursuing M. Sc. (Engineering) in Information and Communication Technology at Mawlana Bhashani Science and Technology University. His research area includes Quantum-dot Cellular Automation and Thin Film Solar Cell.

Ali Newaz Bahar received his M.Sc. (Engineering) in Information and Communication Technology from Mawlana Bhashani Science and Technology University (MBSTU), Tangail-1902, Bangladesh in 2015. He is currently an Assistant Professor in the Department of Information and Communication Technology of Mawlana Bhashani Science and Technology University. His research area includes Quantum-dot Cellular Automation, Thin Film Solar Cell, Big Data Analysis, WSN and Fuzzy Set.

Md. Ahsan Habib received B.Sc. in Computer Science & IT and M.Sc. in Computer Science & Engineering from Islamic University of Technology, Bangladesh. He is an Associate Professor in the Department of Information and Communication Technology in Mawlana Bhashani Science and Technology University, Bangladesh. His research interests include wireless sensor network, QCA gates, bio-informatics, data mining etc. He is a member of IEB, IEEE, ACM, Bangladesh Physical Society, Bangladesh Computer Society and Lions Club International.

Nur Mohammad Nahid received his B.Sc. (Engineering) Information and Communication Technology from Mawlana Bhashani Science and Technology University (MBSTU), Tangail-1902, Bangladesh in 2017. His research area includes Quantum-dot Cellular Automation (QCA) and reversible logic synthesis.

Mohammad Maksudur Rahman Bhuiyan received his Ph.D. from the University of New England, Armidale, Australia. Currently, he is on deputation in Higher Education Quality Enhancement Project (HEQEP), ICT Unit, World Bank Finance Project. He works on Routing and switching system design, Cloud computing, Computer voice network, Nano-communication network and Quantum-dot Cellular Automation.

