International Journal of Grid and Distributed Computing
Vol. 10, No. 1 (2017), pp.43-50
http://dx.doi.org/10.14257/ijgdc.2017.10.1.05

Universal Reversible Gate in Quantum-Dot Cellular Automata (QCA): A Multilayer Design Paradigm

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Abstract

Quantum-dot cellular automata (QCA) has been analyzed methodically as a rising nano technological model where coulombic interaction has been used to carry out binary operations. QCA draw an enormous attention for its extreme speed, low power and exceptionally dense integration comparing the conventional Complementary Metal–Oxide–Semiconductor (CMOS) technology. This article presents universal reversible logic gate based on the conventional QCA cell and multilayer design model along with the quantum cost. The power depletion by the layout is appraised, which confirms the prospect of nano-device functioning as a complementary stand for the presentation of reversible circuits. The constancy of the proposed design is evaluated under thermal randomness indicating the operational efficacy of the circuit. The simulation outcome of the proposed layout is verified with abstract values, presenting the precision of the layout. For confirming and simulating the suggested design QCADesigner, a known verification, and simulation tool has been used.

Keywords*: Quantum Cellular Automata; Universal Reversible Gate; QCADesigner; Power Dissipation; Reliability.*

1. Introduction

With scaling down of usual CMOS, certain critical difficulties in this robust technology arise that influence researchers to attempt and obtain an explanation or else a substitute technology. Quantum dot cellular automata is a convincing substitute among nanotechnology resolutions and effective alternate of CMOS technology [1, 2]. QCA has several powerful features some of which are not presented in CMOS and it is supposed to attain ultra-low power consumption, high-level clock frequency and extreme device density [1-3].

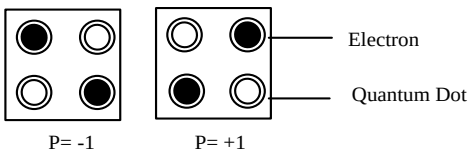


Figure 1. Illustration of Four Doted QCA Cell with Binary Encoding Representation

ISSN: 2005-4262 IJGDC

The major component in QCA is a four dot squared cell and it contains two mobile electrons [1, 2]. Because of the coulombic connection, these electrons employ the dots transversely repulsion [2]. Disparate CMOS technology, QCA converts binary information by a comparative structure of the charges rather than current and therefore application of QCA designs directs toward lesser extents and rapid operation [1].

The coulombic connection among the electrons creates two firm arrangements P = -1 and P = +1, which are allocated to fixed a logic "0" position and logic "1" position, correspondingly, as shown in Figure 1. The cell polarization equation [10] is presented below:

$$P = \frac{(\rho_2 + \rho_4) - (\rho_1 + \rho_3)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)} \tag{1}$$

Where, the charge at dot *i* expressed by ρ_i

QCA wire is a cluster of organized QCA cells along with the similar polarization and binary information transfers from input to output channel due to the coulombic relations between cells. Two distinct shapes of QCA wire are formed to shift data in QCA [4]. First one is binary QCA wire formed by 90° cells and another is the inverter orders of QCA cells which are formed by 45° cells. Figure 2 clarifies the arrangement of two wire forms.

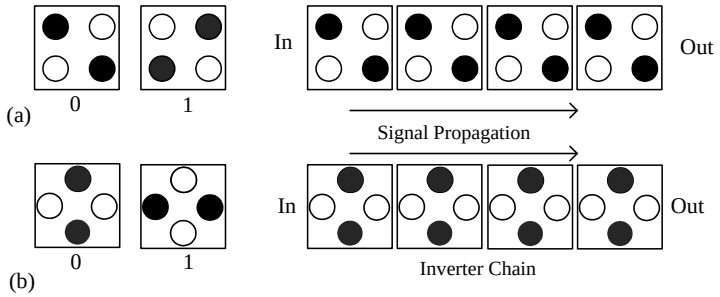


Figure 2. Signal Propagation through Binary Wire (a) Normal Array or 90^0 QCA Wire (b) Inverter Chain or 45^0 Wire

The essential Boolean basic in QCA is the majority voter and various proficient formations of QCA circuits applying majority voters have turned into pervasive [2-9]. Three input majority voter (Maj_3) is the elemental logic gate in QCA which can be recognized by five cells, three input cells, one exclusive central cell and one output cell. The central cell also identified as device cell that changes to principal polarization and regulates the stable output. Maj_3 can be organized as an OR and the AND logic gates [1-3], merely by setting the polarization of one of the inputs of the MV gate to P = +1 (logic "1") and P = -1 (logic "0"), respectively shown in Figure 3. The logical illustration of Maj3 is as follows:

$$MV(A,B,C) = AB + BC + CA \tag{2}$$

To compose "AND" and "OR" logic gate, we need to fix one of the MV input stables to zero or one. Equation (3) exhibits the AND function where, input "C" is set to "0" and Equation (4) exhibits the OR function where input "C" is set to "1".

$$MV(A,B,0) = AB + A.0 + B.0 = AB \tag{3}$$

$$MV(A,B,1) = AB + A.1 + B.1 = A + B \tag{4}$$

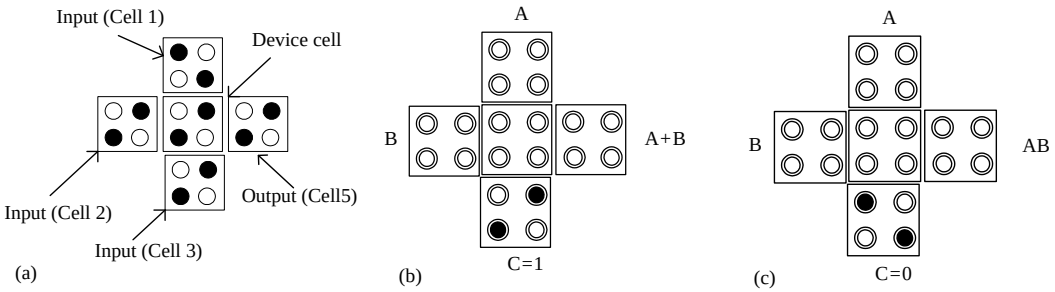


Figure 3. Primary Sructure of 3-input Majority Gate (a), Programmed as 2-input OR Gate (b) and 2-input AND Gate (c)

The inverter in QCA returns the reverse of the input value. The input polarization is apportioned into two polarizations and in time, two chains connect and compose the opposite polarization [1-2] shown in Figure 4.

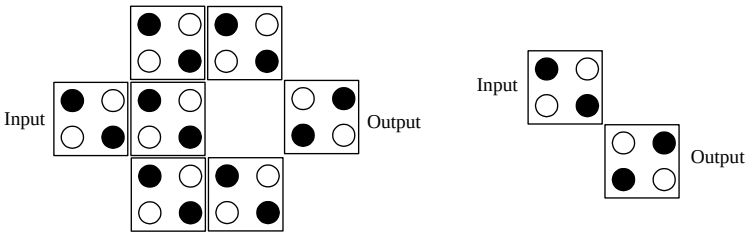


Figure 4. Different forms of Inverter Gate in QCA

2. Methodology

The projected layout has been functionally verified and simulated with the QCADesigner [10]. An appraisal is fulfilled to achieve the requisite tools and to confirm the suggested design. At the design level, small joining block of QCA is devised and then simulated for checking its accuracy. Later these small building blocks are combined together through QCA wire to generate the proposed design. The proposed layout is simulated and confirmed by means of QCADesigner ver. 2.0.3. The Bistable simulation tool has been utilized through the simulation transmission between cells; clearly, the interaction intensity connecting two cells decomposes perversely with the fifth power of the thickness unraveling them. In this estimate, not all the cells result are reflected. Barely cell within the radius of R are being pondered. For cell i, the precisely model have depicted by the following Hamiltonian:

$$H_i = \sum_j \begin{pmatrix} -\frac{1}{2} P_j E^k_{i,j} & -\gamma \\ -\gamma & \frac{1}{2} P_j E^k_{i,j} \end{pmatrix} \tag{5}$$

$E^k_{i,j}$ is the kink energy between the two cells (i and j); Pj denotes the polarization for cell j and channeling energy is Υ. For each cell i, the quantity of the Hamiltonian is done all cells (i.e., j) within its radius of effect R.

3. Proposed Circuit

Reversible computing is a computational pattern where a number of inputs and outputs are equal with a one-to-one mapping. Reversible logic has obtained enormous

consideration because of their dimensions to reduce the power dissipation.

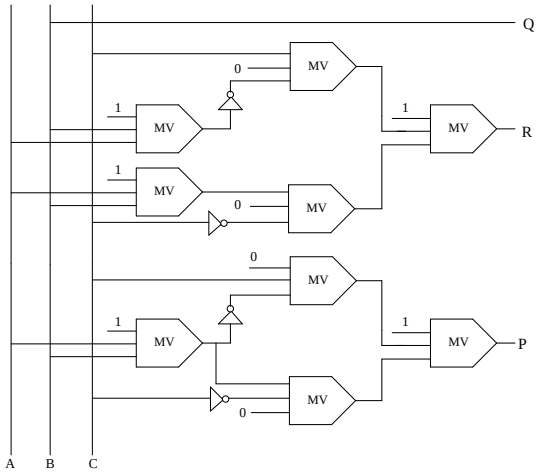


Figure 5. Schematic QCA Block Diagram of Proposed URG

The finest remarkable function of reversible logic remains in quantum computing [13] and it can be realized through quantum dot cellular automata [11-20]. This paper represents the layout formation of a reversible "URG" logic gate.

3.1. URG Gate

Universal Reversible Gate [21] (URG) is a 3×3 logic gate with input vector I (A, B, C) and output vector O (P, Q, R). The output expression is P = (A+B)⊕C, Q = B, and R = AB⊕C. Figure 5 indicates the QCA circuit diagram of 3×3 Universal Reversible gate and Table 1 presents the truth table of this logic gate.

Table 1. Truth Table of Proposed Universal Reversible Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	1
1	1	1	0	1	0

4. Simulation and Results

For verifying the functionality of proposed logic circuit, the following default bistable approximation parameters have been considered: cell size = 18 nm, number of samples = 50000, radius of effect = 65.000000nm, convergence tolerance = 0.0000100, relative permittivity = 12.900000, clock high = 9.800000e–022 J, clock low = 3.800000e–023J, layer separation = 11.500000, clock amplitude factor = 2.000000, and maximum iterations per sample = 100. These values are the stable criterions in QCADesigner [22].

The quantum cost of any 2x2 reversible circuit is one, while reversible 1x1 circuit has a quantum cost of zero. The quantum cost of a QCA design can be obtained from the area. The proposed QCA URG has area 0.036 μm^2 and latency 1. Therefore, the quantum cost of URG is area×latency^2=0.036.

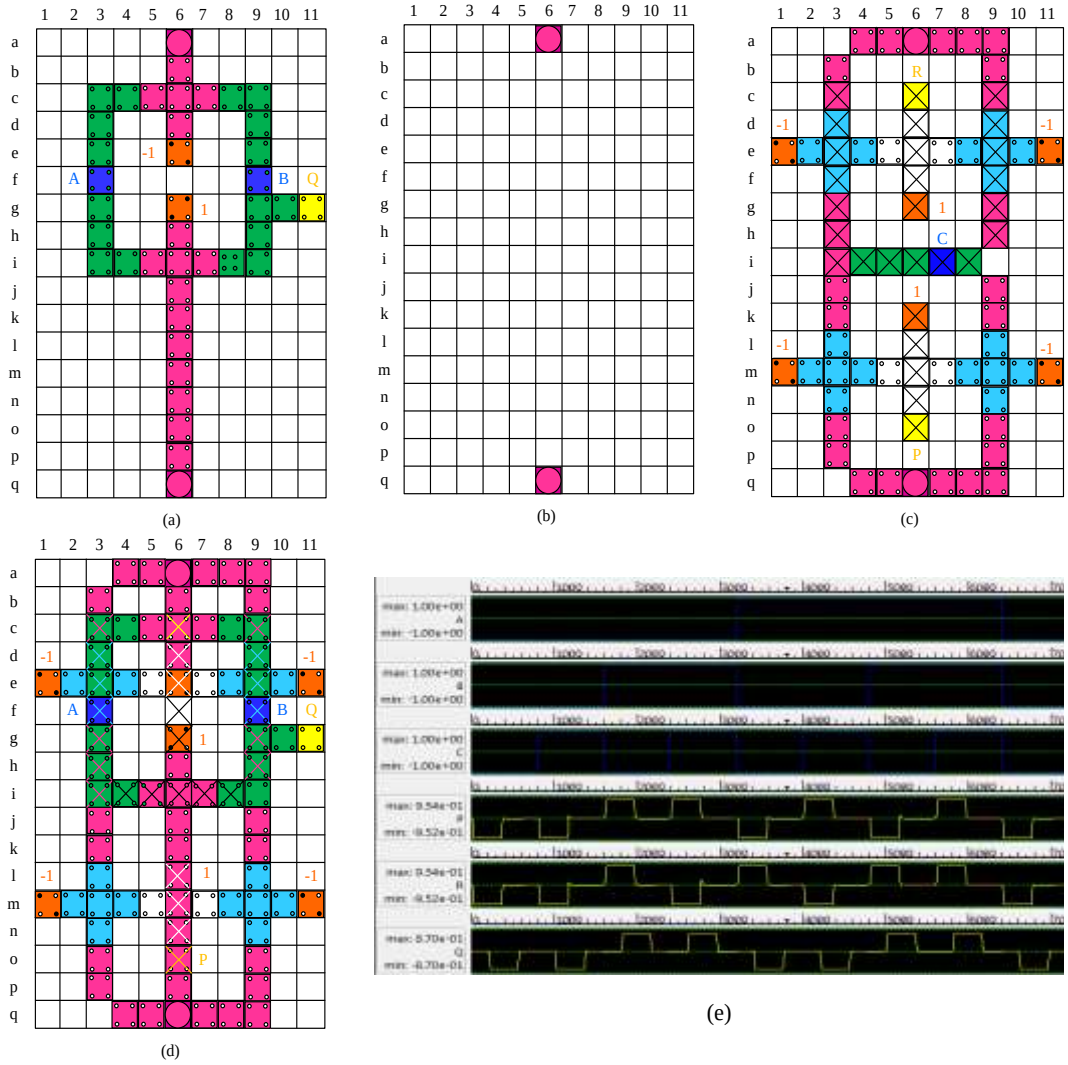


Figure 6. Simulated Circuit Layout of Proposed Universal Reversible Gate (a) Main Layer (b) Layer-1 (c) Layer-2 (d) Top View of the Proposed Circuit and (e) Simulated Input-output Wave Form

The proposed gate has been designed in the conventional single layer with multilayer wire crossing fashion. In the circuit layout, three layers (Layer 1, Layer 2 and Layer 3) and two static polarization P = -1.00 and P = 1.00 has been used. A two-dimensional coordinate system has been employed to recognize each cell position. Layer 1 containing two inputs "A" and "B", and one output Q. In this layer, both "A.B" and "A+B" operation take place shown in Figure 6 (a), and the result of those operations has been passed to the next layer. Layer 2 is used only for passing the signal to the next layer shown in Figure 6 (b), and the Layer 3 containing one input cell "C" and two outputs "P" and "R" shown in Figure 6 (c). The overall circuit layout of the proposed universal reversible logic gate is shown in Figure 6 (d). All the output values are tested with the truth table given in Table 1 and the input-output waveform ensure the precisions of the proposed logic gate shown in Figure 6 (e). Total 114 cells are used, where 40 cells are needed in layer 1, two are used in

layer 2 and 72 cells are used in layer 3. The comparison between proposed universal reversible logic gates with the previous design is given in Table 2.

Table 2. Performance Comparison of QCA-based URG [21] Design and our Proposed Design

Circuit	Number of cells	Approximated area (μm^2)	Latency (clock)	Gate count (MV + Inverter)
URG [21]	134	0.173	1	13
Proposed URG	114	0.078	1	13

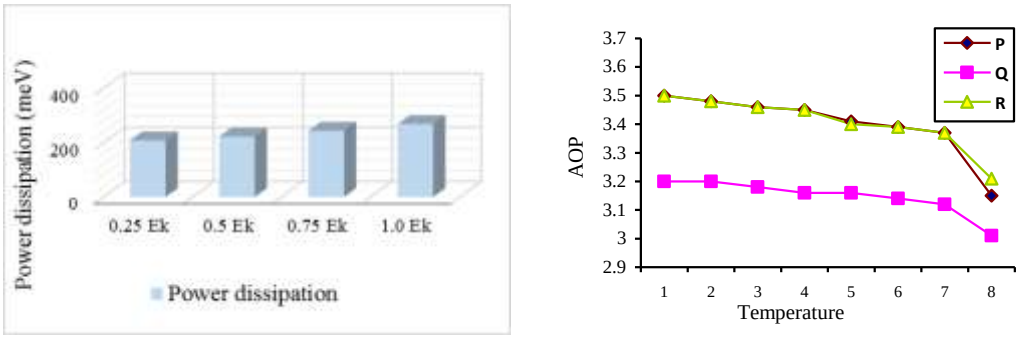
5. Power Dissipation and Reliability of the Proposed Layout

Every QCA cell exposes uniform power depletion. Through the process in one clock phase, the power depletion by the complete circuit is projected by counting the computation of power dissipation of all majority voters with inverters [23, 24]. The technique stated in [25, 26] is applied to analysis the power depletion of the proposed QCA layout at temperature *T=2K* in discrete tunneling energy. The effects are presented in Table 3 and Figure 7 (a). Here, E_k, γ, and T signify the kink energy, tunneling energy, and functioning temperature, correspondingly. Average output polarization (AOP) of any QCA output cell is decreased by increasing the temperature.

Table 3. Power Dissipation by the Proposed URG

Power dissipated at T=2K			
$0.25E_k$	$0.50E_k$	$0.75E_k$	$1.0E_k$
209.2	223.4	244.8	269.8

The result of temperature on the AOP of the proposed QCA design is displayed in Figure 7 (b). The circuit works effectively between 1K and 7K. To produce the AOP at various temperatures, the proposed circuit is simulated by the QCADesigner and the lowest and highest polarizations for every cell are noted.



(a) (b)

Figure 7. (a) Energy Dissipated by the Proposed Circuit and (b) Temperature Impact on AOP

6. Conclusion

In this article, a novel multilayer based layout of Universal Reversible Gate (URG) has been presented. The utilization of URG in the progress of combinational circuits would be productive respecting delay and power saving due to the designing paradigm. Quantum cost based estimation settles that the signified circuit has extremely small quantum cost and the design has particularly low heat power depletion, showing that QCA nano-devices are suitable for using reversible circuits. The assessment of consistency of the proposed layout under thermal randomness shows the stability of the circuit. The evaluation of simulation results of the proposed design with abstract significances confirms the functionality of the circuit.

This design gives great amount flexibility to a designer to modify their designs according to their requirements. Therefore, it resolves that the proposed design should be promising move towards the purpose of low power architecture in nanotechnology.

Acknowledgments

We would like to thanks the anonymous reviewers for their valuable comments.

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