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Switchable Direct-Conversion Receiver for 2GHz and 5GHzwith Sub-harmonic Mixer

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Abstract

This paper reports on a fully-integrated CMOS switchable direct-conversion receiver for 2GHz, 5GHz.Switchable low noise amplifier is proposed for suiting for multiband (2GHz, 5GHz).Sub-harmonic mixing is used for down-conversion to minimize the DC-offset due to LO-leakage. The residual DC-offset is cancelled by a digital-to-analog converter at the output of mixer. For quadrature down-conversion with sub-harmonic mixing, octa-phase LO signals are generated by an integer-N type frequency synthesizer. Implemented in a 0.18m CMOS technology, the receiver dissipates 97mA from a 1.8V supply voltage and has 6.5dB noise figure (NF) and -4dBm input third-order intercept point (iIP3). The phase noise of the closed-loop VCO is -108dBc/Hz at 1MHz offset.

Keywords*: Switchable DCR, Frequency synthesizer, VCO, Sub-harmonic mixing*

1. Introduction

Among various kinds of wireless communication system, multi-band is most popular for short range communications due to its high data rate. For low cost and low power implementation of WLAN terminal, fully-integrated CMOS RF transceiver is required for which low-IF or zero-IF (direct-conversion) architecture is most suited because the number of external components is minimized [1]. Low-IF architecture provides much higher immunity for DC-offset and flicker noise than direct-conversion architecture but high-level of matching between signal paths is required for sufficient image rejection [2]. The 2GHz, 5GHzWLAN standard, IEEE 802.11a, b are employing OFDM where the first sub-carrier is not used and the channel bandwidth is wide [3]. Therefore,Switchable low noise amplifier is proposed for suiting for multiband (2GHz, 5GHz) and also it is relatively immune to DC-offset and flicker noise and direct-conversion receiver architecture has been a popular choice [4].

In this paper, a fully-integrated CMOS switchable (DCR) direct-conversion receiver including frequency synthesizer is described for 2GHz, 5GHz WLAN applications. Sub-harmonic mixing minimizes the DC-offset and the residual DC-offset of baseband circuits is compensated by a digital-to-analog converter. Octa-phase local oscillator (LO) signals required for quadrature sub-harmonic mixing are generated by an integer-N type frequency synthesizer. The architecture and circuit implementation of the receiver are described and the detailed experimental results are given.

2. Direct Conversion Receiver

The overall block diagram of the 2GHz, 5GHz direct-conversion receiver is shown in Figure 1. Bandgap reference generates required bias voltages and currents for each block. Serial port interface (SPI) is used to provide the various control signals such as

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gain-control of low-noise amplifier (LNA) and programmable gain amplifier (PGA).

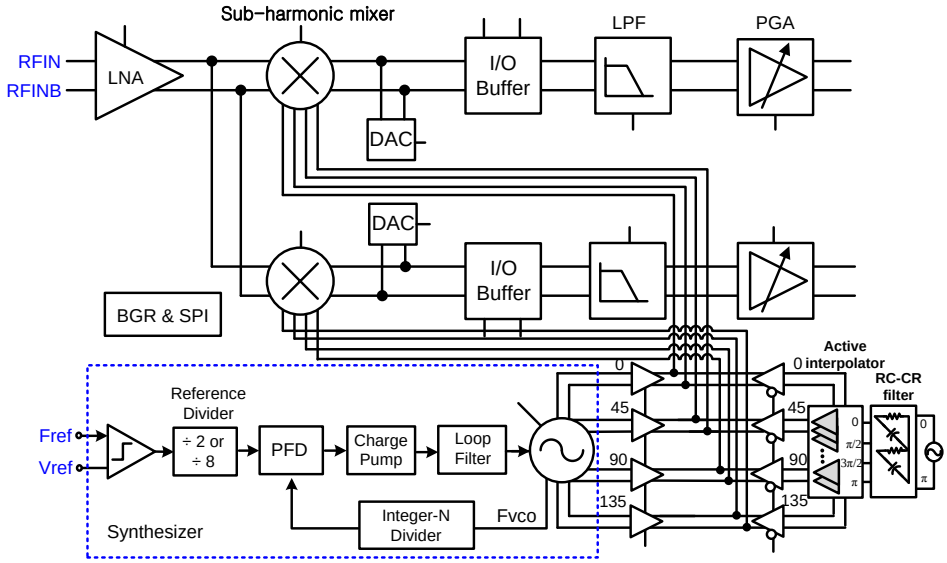


Figure 1. Direct-conversion RF front-end architecture of 2GHz, 5GHz WLAN

To minimize the DC-offset due to LO self-mixing, sub-harmonic mixing is used for down-conversion. The residual DC-offset of baseband circuits is cancelled by a DAC at the output of down-conversion mixer. All the signal paths are fully differential to minimize noise coupling and even-order harmonic distortion. For quadrature down-conversion with sub-harmonic mixing, octa-phase LO signals are generated by an integer-N type frequency synthesizer. The channel-selection filtering is performed by a fifth-order Chebyshev active-RC filter which is followed by a programmable gain amplifier (PGA).

1. RF front-end

A. Low noise amplifier

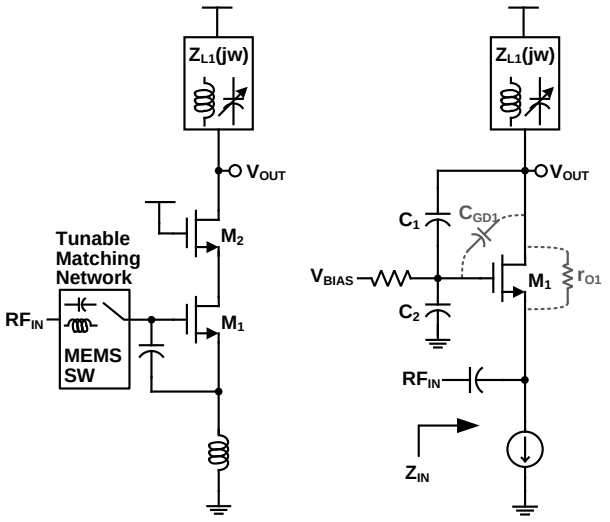
In switchable RF front-end, LNA is the most challenging block because of its high sensitivity to parasitic effects and variation. The performance of the LNA should not be traded off with the switchability. In terms of the performance, it is known the common-source degenerated LNA is the best among the various architectures of narrow-band LNA in Figure2-(a). However, because of the narrow-band frequency characteristic of its input matching network, it is not easy to have switchable input matching network. Either internal MOS or external MEMS switches can be used to change the resonant frequency of the input matching network. However, any switch in the input matching network degrades noise figure (NF) due to its loss and external MEMS switch can increase the cost and form factor of the system.

Another solution for switchable LNA is the common-gate LNA with capacitive feedback as shown in Figure2-(b). Unlike the conventional common-gate stage, the LNA shows narrow-band input matching characteristics by employing a capacitive voltage feedback with C_1 and C_2. The input impedance Z_{IN} is given as:

$$Z_{IN} = \frac{1}{g_{m1}} + \left(\frac{C_1}{C_1 + C_2} \right) \cdot Z_{L1}(\omega_0) \quad (1)$$

where g_{m1} and $Z_{L1}(\omega_0)$ are the transconductance of the input transistor and the load impedance at the frequency ω_0, respectively. Equation (1) shows that the input

matching network can be easily



(a) (b)

Figure 2. (a) Common Source Degenerated LNA with Tunable Matching Network. (b) Common Gate LNA with Capacitive Feedback

reconfigured by controlling the resonant frequency of the load impedance Z_{L1}. The noise factor F can be easily derived as:

$$F = 1 + \frac{\gamma}{g_{m1}R_S} + \frac{R_S}{R_{L1}}\left(1 + \frac{1}{g_{m1}R_S}\right)^2 \quad (2)$$

where γ is a noise parameter and R_{L1} is the equivalent load resistance of $Z_{L1}(\omega_0)$. The equation (2) is exactly the same as that of a conventional common gate LNA. But, in common gate topology, g_{m1} is fixed to $1/R_S$ for input matching and its minimum NF is limited to about 3dB [11]. For the common-gate LNA with capacitive feedback, the voltage feedback allows g_{m1} to be higher than $1/R_S$=1/50and thus the NF of the LNA can be greatly improved.

In the equation (1), however, the parasitic effects are ignored and if we include the parasitic effects of the transistor M_1, the input impedance Z_{IN} changes as:

$$Z_{IN} = \frac{1}{g_{m1}} + \left(\frac{C_1 + C_{GD1}}{C_1 + C_2 + C_{GD1}}\right) \cdot Z_{L1}(\omega_0) + \frac{Z_{L1}(\omega_0)}{g_{m1}r_{O1}} \quad (3)$$

where C_{GD1} and r_{O1} are the gate-drain parasitic capacitance and the output resistance of M_1. The gate-drain capacitance C_{GD1} changes the feedback factor and the output resistance r_{O1} provides unwanted feedback. Thus, the input impedance is affected by the unpredictable parasitic and secondary effects. For low NF, the transconductance g_{m1} of the transistor M_1 is desired to be as large as possible, which means large size of M_1 and in turn large C_{GD1}. Larger C_{GD1} means lower impedance level at the output node, which limits the achievable gain of the LNA. Therefore, there must be a trade-off between the NF and gain.

To solve this problem, in this work, a switchable cascode transistor is inserted between the input transistor and the load network as shown in Figure 4. The feedback factor is no longer affected by parasitic capacitance and the input impedance can be found as:

$$Z_{IN} = \frac{1}{g_{m1}} + \left(\frac{C_1}{C_1 + C_2} \right) \cdot Z_{L1}(\omega_0) + \frac{r_{O2} + Z_{L1}(\omega_0)}{g_{m1} r_{O1} g_{m2} r_{O2}} \quad (4)$$

This equation shows the third term of the equation (3) due to the unwanted feedback is reduced by the cascode transistor as expected. The cascode transistor also eliminates the need for the trade-off between the gain and NF. For low NF, the size of the input transistor M_1 can now be freely chosen. Because the size of the cascode transistor can be smaller than the input transistor, the effect of the parasitic capacitance of the cascode transistor on the gain is not severe. Therefore, the performance optimization towards lower NF and larger gain becomes much easier.

Additional advantage of using cascode transistor is that the cascode transistor can be used as a switch to select the optimum load network for different RF band. If the load network is implemented with an inductor and switchable capacitor bank to reconfigure the resonant frequency, the load impedance would be too small for lower RF band, which means degraded gain. To ensure sufficient gain for the whole RF band, separate LC load networks are provided for each RF band. The signal current from the input transistor is switched by the cascode transistor to the suitable LC load network. The switching of the cascode transistor is done by toggling its gate voltage between 0V and the bias voltage for cascoding.

Figure 3 shows the schematic of the LNA which has three load networks for 2GHz, 5GHz bands respectively to have optimum impedance level at the output. Because the cascode transistors act as switch, the input transistor can be shared for all the frequency bands. But, in the current design, there are two input transistors each of which is for 2~3GHz and 5GHz bands in order not to have too large parasitic capacitance on the drain node of the input transistor. The input transistors are also switched by toggling their gate voltages between 0V and the bias level.

The LNA has dual gain modes to relieve the linearity requirements on the following stages. If the bias condition and/or load network are changed to control the gain, the input matching condition is changed because the load impedance determines the input impedance. So, the low-gain mode output is obtained by the capacitive voltage divider C_3 and C_4 which is always connected to the load network

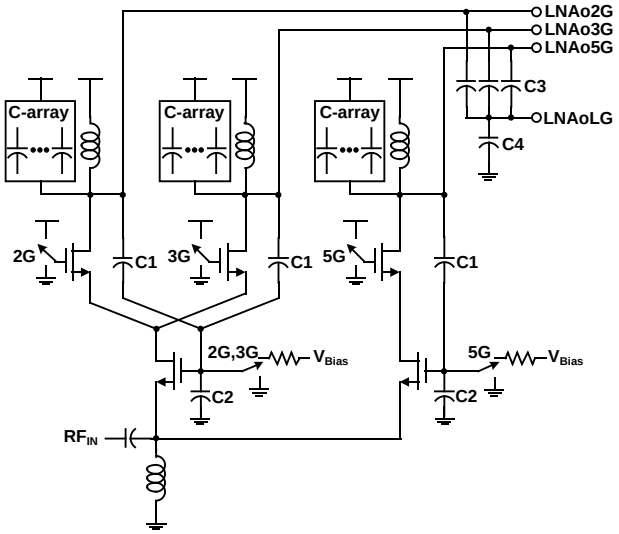


Figure 3. Switchable Low Noise Amplifier

and thus does not change the load impedance at the low gain mode. Because the

capacitance of C_3 is very small, the effect of the capacitive divider C_3 and C_4on the load impedance is negligible. The LNA has four outputs, *LNA*2*G*, *LNA*3*G*, *LNA*5*G* which are 2GHz, 3GHz, 5GHz high gain mode outputs and low gain mode output, respectively. The LNA has 23dB/1dB voltage gain and 2.5dB NF at high-gain mode while consuming 10mA from a 1.8V supply.

B. Sub-Harmonic Mixer

To remove the DC-offset due to the LO self-mixing, the double-balanced sub-harmonic mixer shown in Figure 4 is used for quadrature down-conversion. The frequency of the LO is the half of that of RF input frequency and therefore octa-phase LO signals spaced by 45^o are required for quadrature down-conversion. As shown in the figure, the I-mixer uses 0^o, 90^o, 180^o, and 270^o LO signals while for Q-channel, 45^o, 135^o, 225^o, and 315^o LO signals are used.

The output of the transconductance stage is AC-coupledto the switching stage to prevent the low-frequency even-order harmonics and DC-offset of the transconductance stage from being leaked to the mixer output. Additional advantage of the AC-coupling is the independent biasing of the transconductance and switching stages, facilitating the design optimization such as the conversion gain, noise figure, and linearity. The output current of the mixer is converted to voltage by a first-order filter whose cut-off frequency is tuned by the same code as the channel selection filter following the mixer.For sub-harmonic mixing, conventionally two stacked LO switching stages are used requiring large voltage headroom [5-6].The switching stage is composed of pMOS transistors to minimize the flicker noise [7-8].

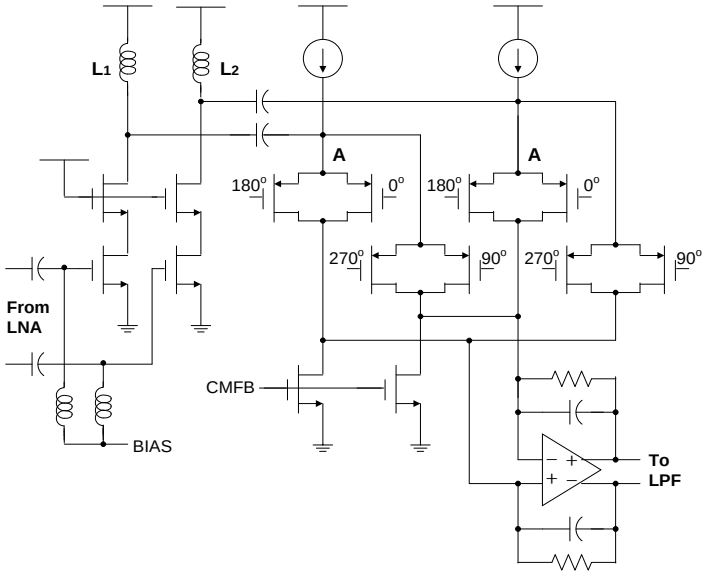


Figure 4. Sub-harmonic Mixer for I-channel

In this work, only one stack of switching stage is used to allow the low-voltage operation and the principle of harmonic mixing is illustrated in Figure 5.

The conversion gain of the mixer is ;

$$G = 20 \log \left(\frac{2}{\pi} g_{mRF} \cdot R_{out} \right) \quad (5)$$

where $g_{m,RF}$ and R_{out} are the transconductance of the RF input transistor and the

output impedance, respectively.

The input referred noise is given as ;

$$\overline{v_{n,in}^2} = \frac{2kT\pi^2}{g_{m,RF}^2}\left\{\gamma_n g_{m,RF} + \gamma_p g_{m,SW}\frac{T_{SW}}{T_{LO}} + \frac{1}{R_{out}}\left(1+\frac{\overline{v_{n,opamp}^2}}{8R_{out}}\right)\right\} \quad (6)$$

where the first term shows the noise of the transconductance stage transferred to the mixer output, assuming a conversion gain of $2/\pi$, the second term is the output noise due to the two switches and the third term is due to the two load resistors R_L. And the fourth term is the OP-amp input noise shown in front of mixer due to first order filter. The first term where γ_n is transconductance stage channel noise factor, traditionally 2/3 for long channel MOSFET's. The second term where γ_p is switching stage channel noise factor. The second term where $g_{m,sw}$ is the transconductance of the switching transistors. T_{LO} and T_{sw} are the cycle time of LO and the duration when the two switching pairs are simultaneously turned on, respectively. The thermal noise of the switching transistors appears at the output during only T_{sw}. From the equations (5) and (6), the conversion gain and the noise figure of the mixer can be improved by increasing the transconductance $g_{m,RF}$ of the RF input transistor. Larger *W/L* ratio increases the parasitics and thereby limits the high-frequency operation, so the overdrive voltage is increased for higher $g_{m,RF}$. Higher overdrive voltage renders additional benefit of better linearity [9]. To minimize the noise contribution from the switching transistors, it is required to reduce the DC bias current of the switching stage and increase the LO amplitude as much as possible. The noise contribution of the switching stage is further reduced by resonating the parasitic capacitance at the node *A* with the inductors L_1 and L_2 [10].

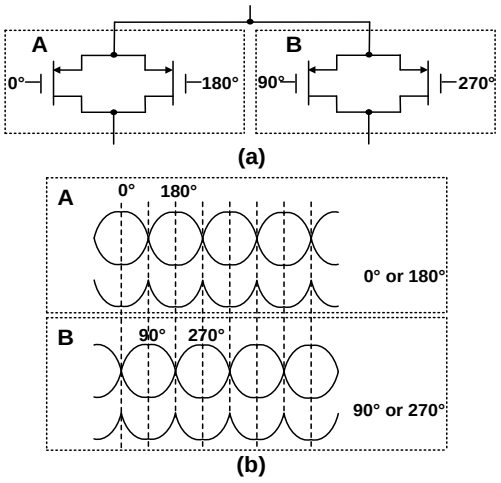


Figure 5. Operation Principle of Sub-harmonic Mixing

2. Analog Baseband

The analog baseband consists of I/Q signal paths which have channel selection filter, programmable gain amplifier (PGA), and digital-to-analog converter (DAC) for DC-offset cancellation.At the input of the channel selection filter, I- and Q-paths have separate DC-offset canceling R-2R ladder type DAC with 7-bit resolution shown in Figure 6.

For channel selection filtering, a fifth-order chebyshev filter shown in Figure 7 is used because it provides, relatively large stopband attenuation with moderate group delay variation within passband. The dynamic range of the filter is maximized by scaling the resistor values to have the same maximum signal swing for all internal nodes. The simulated cut-off frequency of channel selection filter can be controlled from 6.3MHz to 15.45MHz as shown in Figure 8.

The gain of the programmable gain amplifier (PGA) in Figure 8can be controlled from 2.5dB to 52.5dB with 0.5dB step.

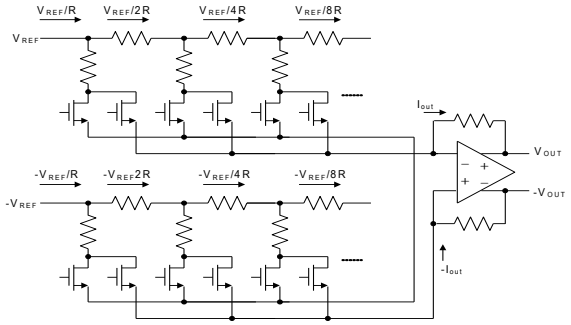


Figure 6.R-2R Ladder Type DAC for DC-Offset Cancellation

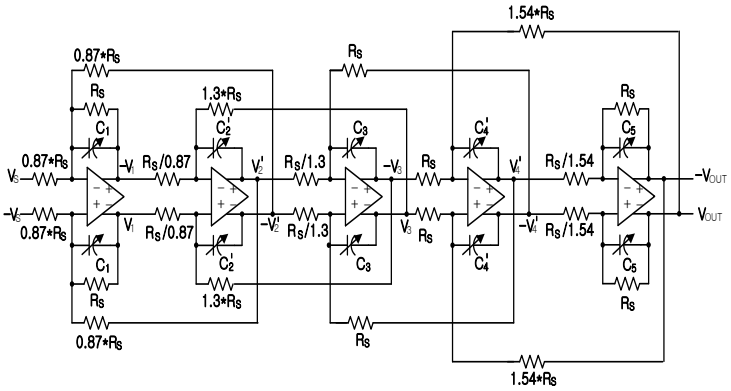


Figure 7. 5th-order Chebyshev Active-RC Filter

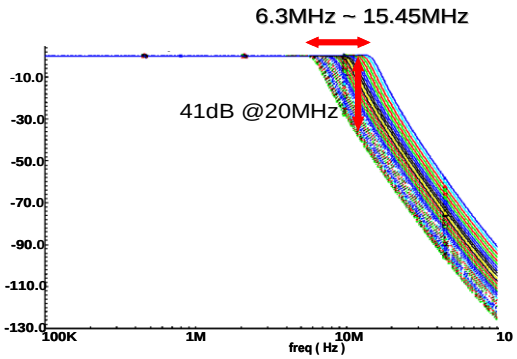


Figure 8. Simulated Channel Selection Filter Frequency Response

In order to achieve the accurate gain value, the resistors are implemented with the array of unit resistance. To minimize the variation and silicon area, high-resistivity poly-Si layer is used for the implementation of the resistors. Because the operational amplifier (op-amp) for channel selection filter and PGA should be able to provide virtual ground for out-of-band signals, the required bandwidth of op-amp is much higher than the channel bandwidth. With conventional frequency compensation using Miller capacitor, however, large bandwidth can be obtained only with large power consumption. The op-amp of this work is employing the current re-using feedforward frequency compensation method to save power [11-12].

3. Octa-phase LO Generation

For quadrature down-conversion with sub-harmonic mixing, octa-phase local oscillator (LO) signals are required at half of the RF input frequency. A ring-type four-stage LC voltage controlled oscillator (VCO) shown in Figure 9 is used for octa-phase LO generation. The biasing transistors of the LC resonators are switched on and off to reduce the flicker noise of the biasing transistors by periodically releasing the trapped electrons [13-15]. In order to have wide frequency range with small VCO gain (K_{VCO}) for low phase noise, two bit digital input, VCN1 and VCN2, coarsely control the oscillation frequency with capacitor bank.

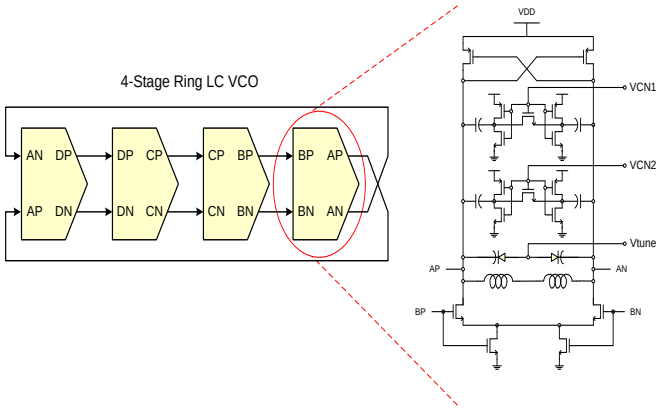


Figure 9. Octa-Phase Ring-Type LC VCO

To obtain the required LO frequency, the LC VCO is embedded in a phase locked loop (PLL) of integer-N architecture as shown in Figure 10-(a). The divide-by-N block of the PLL shown in Figure 10-(b) has multi-modulus (16/17/18/19) prescaler instead of normally used dual-modulus one. If with conventional dual-modulus prescaler, the counting ratio of asynchronous programmable counter can be as large

as 256, resulting in large delay and the re-timing with the prescaler output becomes very difficult. The programmable and swallow (P/S) counters are merged together to decrease the silicon area. The output of the merged P/S counter is re-timed by the output clock of multi-modulus prescaler to reduce the jitter of divided-by N clock. The loop filter of the PLL is implemented off-chip.

The octa-phase outputs of the VCO are buffered by Cherry-Hooper type amplifier to have sufficient voltage swing. The phase noise of the open-loop and closed-loop octa-phase VCO is -120dBc/Hz and -108dBc/Hz, respectively at 1MHz offset. The phase error between the octa-phase LO signals is smaller than 1^{o} for whole frequency range.

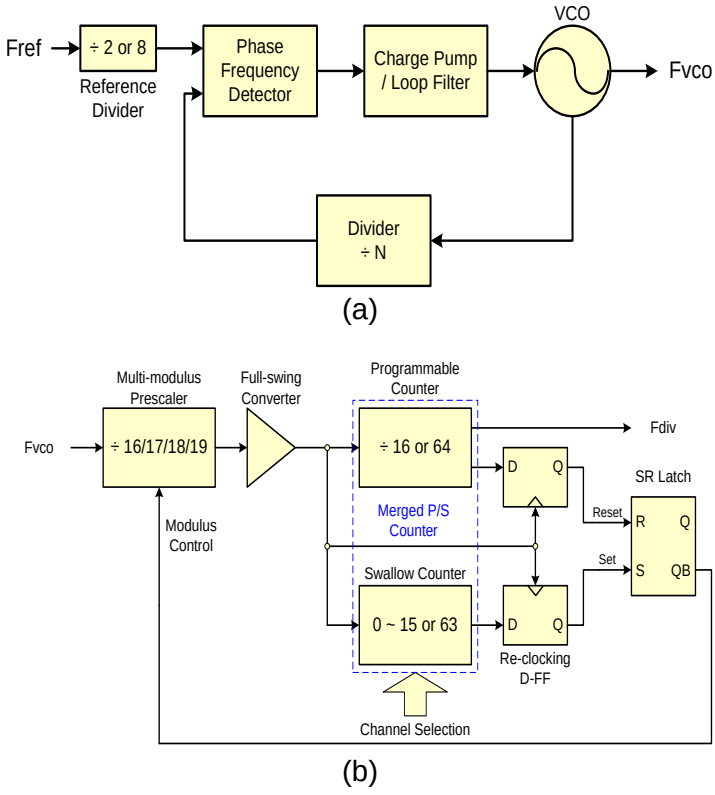


Figure 10. (a) Frequency Synthesizer and (b) Divider-by-N

3. Experimental Results

The 5GHz direct-conversion receiver has been implemented in a 0.18μm CMOS technology whose microphotograph is shown in Figure 11. The die occupies a core area of 5.76mm^2 and is packaged in a 48-pin MLF package with an exposed die.

The measured results of several building blocks such as RF front-end, DC offset calibration circuit, channel selection filter, PGA, and VCO can be obtained respectively.

Beacause LNA consists of the cascoded differential pairs, an external balun is needed for the single-ended to differential conversion of the signal source. And also, because of implementing all differential circuits, differential prove is need for the differential to singe-ended conversion of the measuremet equipment.

The measured voltage gain of the overall receiver is from 71dB to 73.5dB in the 2GHz, 5.15~5.35GHz range as shown in Figure 12. Measured noise figure at LNA input is from 6dB to 6.5dB in the from 5.15 to 5.35GHz range.

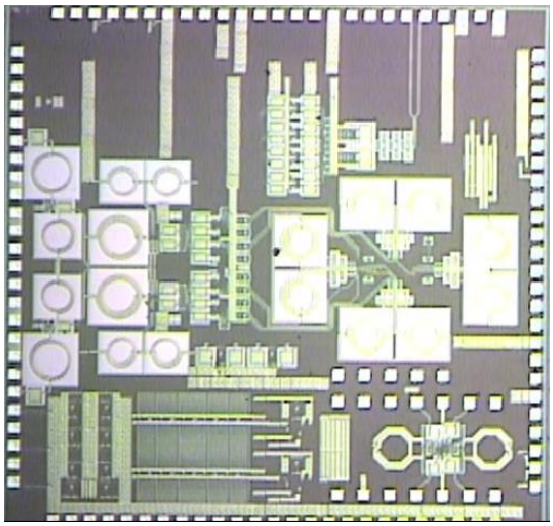


Figure 11. Die microphotograph of the Direct Conversion Receiver

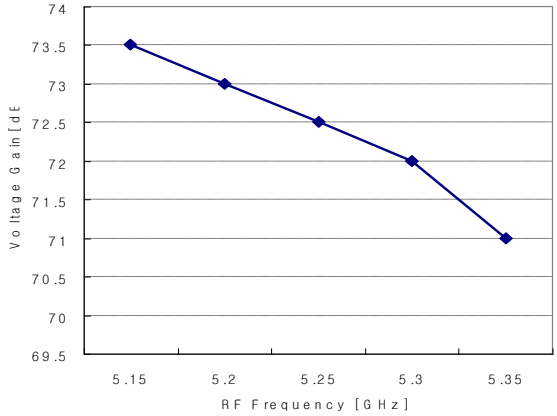


Figure 12. Measured Voltage Gain of the overall Receiver

When the LO is at 2.5675GHz and two-tone RF signals are applied at 5.15GHz and 5.157GHz to result in down-converted baseband fundamental tones at 15MHz and 22MHz, the iIP3 of the receiver in high-gain and low-gain modes is -16dBm and -4dBm, respectively. Measured P1dB of receiver is -15dBm in LNA, PGA low-gain mode. The measured cut-off frequency of channel selection filter can be controlled from 5MHz to 12.7MHz.Measured result of the stop band rejection is less than -41dB.

The gain error of PGA is smaller than 0.25dB for whole gain control range. Measured performance of RF Front-end agrees well with the simulations except for the noise figure performance. The LNA and the sub-harmonic mixer achieve from 35dB to 37.5dB voltage gain in the 5.15 ~ 5.35GHz range and achieve from 3.1dB to 3.9dB noise figure in the same frequency band. The out-of-band iIP3 of the receiver in high-gain modes is -13dBm. The LNA and the sub-harmonic mixer consume 62.4mW from 1.8V. Measured performance of DC offset is summarized, as shown in Table 1. In order to measure static dc-offset, LO, RF signals are not present, the output CM level difference is less than ± 27mV. The value of LO self-mixing to RF is less than ±5mV. Compare to pre-calibration, calibrated measured DC offset value is less than ±1mV. Table 2 summarizes the overall receiver performances. The receiver achieves from 71dB to 73.5dB voltage gain in the 2GHz, 5.15 ~ 5.35GHz range and achieves from 6dB to 6.5dB noise figure in the same frequency band. The out-of-band iIP3 of the

receiver in high-gain and low-gain modes is -16dBm and -4dBm, respectively. The receiver consumes 97mA from 1.8V.S11 less than -10dB at LNA input is achieved in the 2GHz, 5.15 ~ 5.35GHz range. After calibration, the calibrated measured DC offset value is less than ±1mV.

Table 1. Measured Performance of DC Offset Cancellation

Rx Full Path DC offset measurement < CMREF = 899mV >					
RF	LO	I	IB	Q	QB
ON	ON	864	931	881	909
OFF	ON	864	931	881	909
OFF	OFF	867	929	876	914
After calibration		898	897	894	895

Table 2. Summarized Performance of the Receiver

Specification	Measurement	
Frequency band(GHz)	2, 5.15~5.35	
Voltage Gain(dB)	71~73.5	
Noise Figure(dB)	6~6.5	
iIP3(dBm)	Low Gain mode	-4
	High Gain mode	-16
S11(dB)	<-10	
DC-offsetcalibration(mV)	±34(Before calibration), ±1(After calibration)	
Power(mA/V)	97/1.8	

4. Conclusion

A fully-integrated CMOS direct-conversion receiver for 2GHz, 5GHz wireless LAN has been developed. Switchable Low Noise Amplifier is proposed for suiting for multiband (2GHz, 5GHz). To minimize the DC-offset due to LO self-mixing, sub-harmonic mixing is used for down-conversion. For quadrature sub-harmonic mixing, octa-phase LO signals are generated by an integer-N type frequency synthesizer. Implemented in a 0.18μm CMOS technology, the receiver dissipates 97mA from a 1.8V supply voltage and has 6.5dB NF and -4dBm iIP3.

Acknowledgment

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