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A Driver Circuit of Spatial Light Modulator

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Abstract

Spatial light modulator (SLM) driving circuit is an important constituent of photoelectric signal conversion system which has a very broad application prospects in various fields such as image display, image recognition, high-speed optical computing and optical communication system. In this study, a high speed and high precision driving circuit was developed, which was applied in 2 level grayscale image processing. This driving circuit adopted Charter .35μm technology. The testing results demonstrated that detection signal was able to follow the driving voltage of modulator and control the modulator on optical signal modulation.

Keywords: *Spatial light modulator (SLM), driving circuit, grayscale*

1. Introduction

The driving circuit which is based on multi-quantum well spatial light modulator (SLM) plays an important part in implementation of photoelectric signal conversion. It is also a bridge connecting the optical signal and the high speed circuit, which has a broad application in diverse fields such as optical computing, optical interconnection and free space optical communication, *etc*.

Modulator based on multi-quantum (nucleation) are particularly interested in its response to a single pixel can be greater than 5 GHZ, faster than the SLMs based on other materials [1]. Into the SLMs photoelectric signal processing and optical computing have made outstanding achievements. A new optical digital signal processing (DSP) based on nucleation SLM 8000 Giga MAC/s and 5 mw/Giga power consumption of the MAC [2]. SLMs development set the new request driver circuit at a higher speed, lower power consumption and higher precision. Previously, some reports have described a multi-chip module array CMOS driving and four pieces of digital to analog converter (DAC) [3-9].This solution allows high frame rate and high power consumption. In addition, the clock signal pathways in motherboard need synchronous drive and 4 DAC chip. Further extension, e lock synchronize all pieces of the path is too long, to support high-speed transmission. Put forward the construction of a sewage DAC each pixel as a possible solution. It integrates all blocks in a chip, reduce the energy consumption and solve the problem of data synchronization, the disadvantage is that the accuracy of the DAC depends on its integral capacitance value significantly limited processing technology. In this application, the output of the relative error is 10% or more of the serious capacitor mismatch, it should not be ignored.

In some image display and graphics recognition systems, usually only the spatial light modulator whose reflected lights show a change in brightness is needed. Therefore, a two level gray-scale modulator driving circuit is designed. The driving circuit of two level gray-scale modular is only required to produce high and low electrical levels, thus the unit

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pixel can be simply designed as two latch units whose converters are cascade connected. However, many uncertain factors exit in flip chip bonding technology, which may cause damage to modulator and driving chip as well as make short-circuit during indium bump interconnection. Therefore, we need to have a full understanding of the data storage status in driving chip before and after the flip chip bonding. Thus, the driving circuit is required not only to drive modulator chip, but also to read each pixel signal which reflects the effects of processing technology on chip.

2. Circuit Design

Since the unit pixel in two level grayscale SLM driving circuit only receives '0' and '1' control signal, thereby outputting low and high driving voltage respectively, therefore, only one digit input signal is required per pixel per frame. Take 112x112 array SLM driving circuit as an example, whose structure is shown in Figure 1. 28-bit parallel port input is adopted. 28 bit digital input signal is converted to 112-bit wide signal through shift register, which is then transmitted to level conversion circuit after being cached by input register. Level conversion circuit converts 3.3V digital signal to 4V analog signal and transmits it to unit array. The digital control circuit on the left side (Ctrl Cir) is used to gate corresponding pixel, while the output circuit on the right side is applied in detecting storage signal. This circuit can not only realize the modulator driving, but also detect the accuracy of the storage signal in driving circuit chip after devices flip chip bonding.

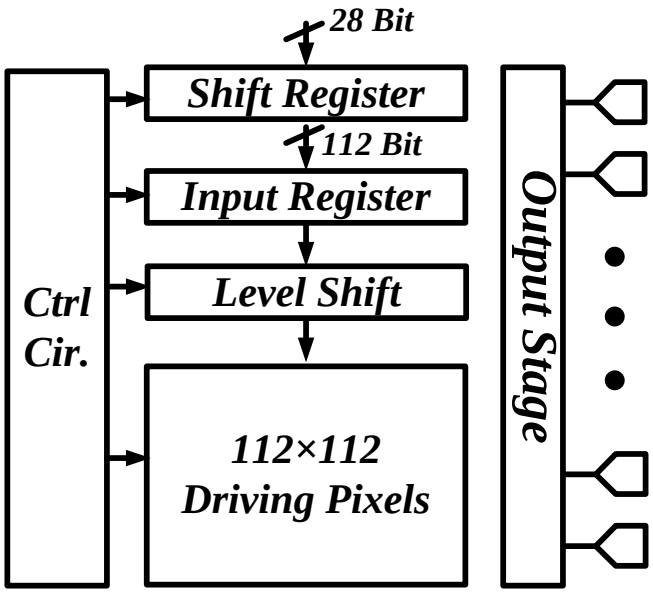


Figure 1. The Structure of 112×112 SLM Driver Circuit

2.1. Circuit Working States

Driving circuit has 4 working states including Scan mode (SCAN), Test mode (TEST), Reset mode (RESET) and set mode (SET).

1. SCAN mode (By default): control circuit gates drive unit in line- by- line form until completing scanning of one frame. Drive unit is similar to a latch where the input data is stored.

2. TEST mode (TEST is set high): there is no data input. Drive units are inter cascade connected. The stored signals are readout via the output circuit through shift operation.

3. RESET mode (RESET is set high): all pixel outputs are "0", namely the minimum potential.

4. SET mode (SET is set high): all pixel outputs are "1", namely the supply voltage.

2.2. Drive Unit Circuit

Drive unit is shown in Figure 2, which is composed of a dual 2- circuit (MUX 2 to 1), register (D flip-flop), and a large CMOS switch. TEST, SET, TEST are state control signals, DATA signal is an input digital signal from level conversion circuit. Lin_scan/CLK signal can switch between row selection control signal and clock signal. Vframe is frame refreshing signal which can control a unifying output of a frame signal. CELL_OUT of each drive unit not only serve as modulator drive, but also is connected to the CELL_IN in the previous drive unit.

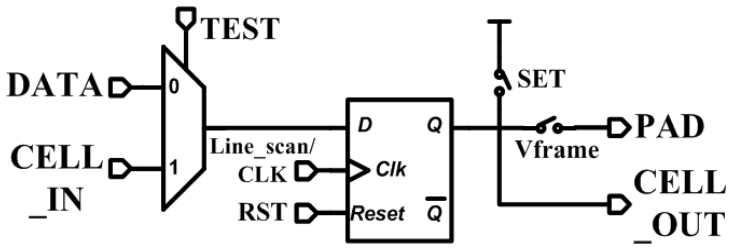


Figure 2. The Pixel Structure of Driver Circuit

The input to circuit is selected by using a dual 2 circuit. By default, the TEST is set 0, DATA serves as drive unit input. Under the control of line scan signal (Line_scan), the data is stored by D flip-flop. When the circuit is converted to TEST mode, TEST signal is set "1", signal CELL_IN serves as drive unit input. Since CELL_IN in each unit is connected to CELL_OUT in previous unit, so the unit arrays can be considered as cascade connection of 112x112 D flip-flops. The trigger signal of D flip-flop is converted to clock by row scan signal, through which the stored data is shifted out.

2.3. Digital Control Circuit

The digital control circuit of two level grayscale driving circuit includes pipeline cache, controller of array circuit, row cache deserializer module, and main control logic of system control digital circuit.

The main function of digital circuit is to continuously read in 28-digit data through pipeline cache, and then to transmit data to each pixel of driving circuit through controller.

2.4. Layout Design

With respect to 112x112 SLM driving circuit, its driving unit circuit is designed within 42x42 μm2 pixel. The driving circuit is located in the middle of pixel, surrounded by power line, ground wire and control signals which are overspread on the entire chip. There is a 20x20 μm2 PAD in each of pixel which is used for voltage output. During fipchip bonding, indium ball with about 20 μm diameter is generated in the PAD.

3. Testing Results and Analysis

3.1. The Results of Simulation and Analysis

The simulation was conducted on entire driving circuit based on HSIM simulator. Because an innovative hierarchical data storage and isomorphism algorithm were adopted, there is no restrictions for the circuit scale of simulation. The simulation speed is also much quicker than that of simulators such as HSPICE and Spectra. Although HSIM shows a shortcoming in simulation accuracy, it is a very ideal simulation software for large scale digital circuits.

By using 50MHZ reference clock, simulation made the circuit completely store 112x112 random '0', '1' input signals in SCAN mode first, and then let the circuit output

signals in TEST mode. The output data is sorted in accordance with the end-to-end order of drive unit, which is not the same with the input signal. Therefore, the sequence of input data was adjusted by using MATLAB, which was compared with that of output data and confirmed to be consistent. In addition, the timing function of the entire chip was also tested to be successful. Figure 3 is the part of simulation results.

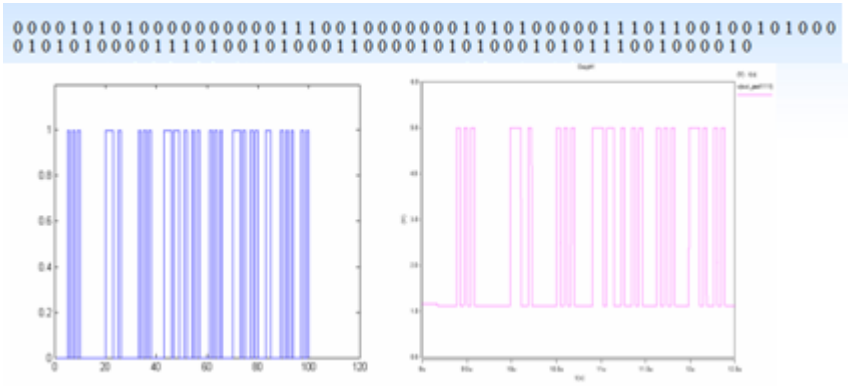


Figure 3. The Contrast of Input and Output Simulation Results

Due to influence of factors such as synchronous switch noise, a stable 3.3V or 4V voltage was not guaranteed by power when chip were working. To observe the effects of voltage changes on chip performance, we respectively simulated D.C. supply change of digital control part from 2.8V to 3.8V, as well as level shifter within chip, pixel array, and the change of D.C. supply of two non-overlapping clock generating circuit from 3.8V to 4.2V. The results show that the chip can work normally. To prevent noise ripple effect on chip, a large amount of filter capacitors were added into chip. In addition, power of triangular wave with 10mV peak value was superposed in the simulation. The results demonstrated that the outputs were still correct, indicating that the noise ripple with 10mV peak value didn't affect chip function.

3.2. Chip Testing Results and Analysis

Chip circuit testing is divided into two parts, electrical testing and optical testing. Electrical testing is to verify whether the driving chip can accurately output expected voltage to drive modulator chip. Optical testing is to test the capacity of circuit and modulator chip to process optical signal after flip flop bonding. The results of optical testing can be confirmed by that of electrical testing to determine the effect of flip flop bonding.

(1) The electrical testing

The electrical testing system of driving circuit is shown in Figure 4, including a two-way D.C. supply which supplies 3.3V or 4V power; FPGA which is used to generate clock, control signal and input data; PCB board, shown in Figure 5, was used to generate chip required bias voltage and power signal filtering; oscilloscope or logic analyzer which was used to observe output signal. In order to prevent light path block, COB encapsulation mode was adopted. And the chip was measured by directly fixing on PCB board.

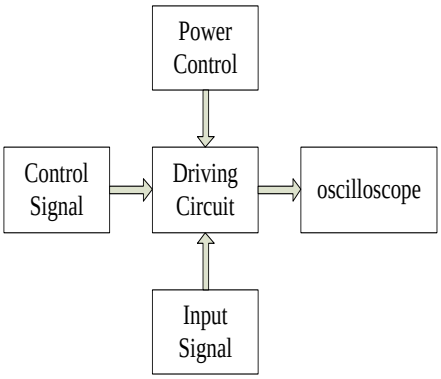


Figure 4. The Electrical Test System of Driver Circuit

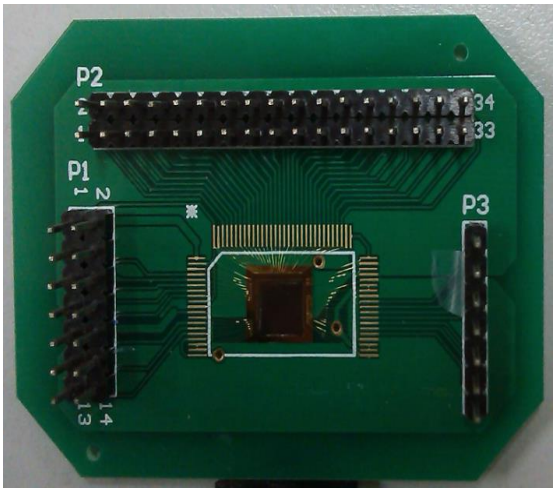


Figure 5. The Test PCB

To test whether the modulator outputs expected voltage controlled by driving chip. The driving voltage was serial shift outputted through driving unit cascade connection, and then compared with input signal. 28-bit input signal was composed of 14 “0” and 14 “1”. Therefore, the output signal is also a 14 alternating armaments of “0” and “1”. Namely, 28 “1” will appear in odd line breaks, while “0” will appear in even line breaks.

The testing results are shown in Figure 6. The chip output data were compared to be the same with input data after transpose in MATLAB, indicating driving circuit working normally.

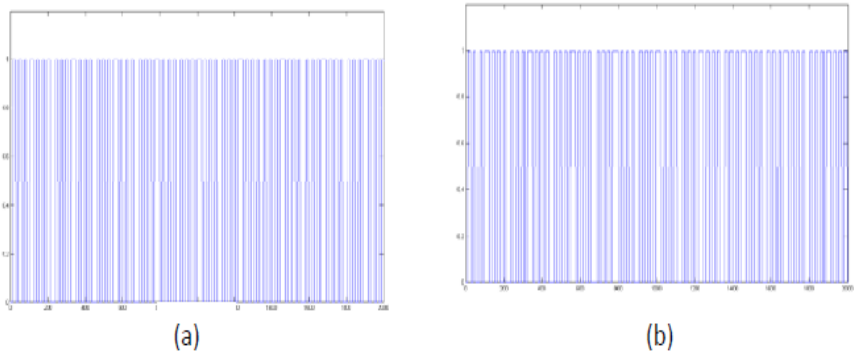


Figure 6. The Electrical Test Results

(2) Optical testing

Optical testing system is composed of 850nm wavelength laser, an actuator, a magnifying lens, a projection lens and a photosensitive detector. To reduce the influence of mixed lights on the testing results, two irises are added in optical path which reassures that the signal received by detector are completely from the reflection of modulator, as shown in Figure 7.

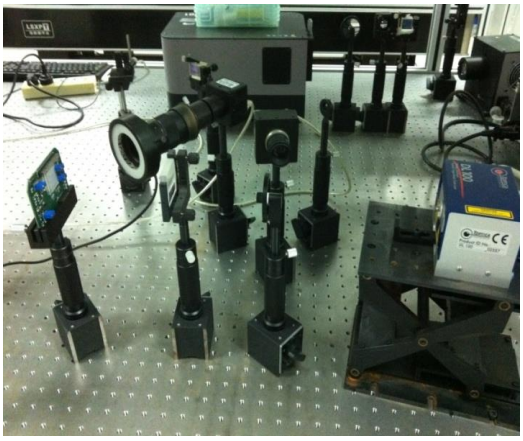
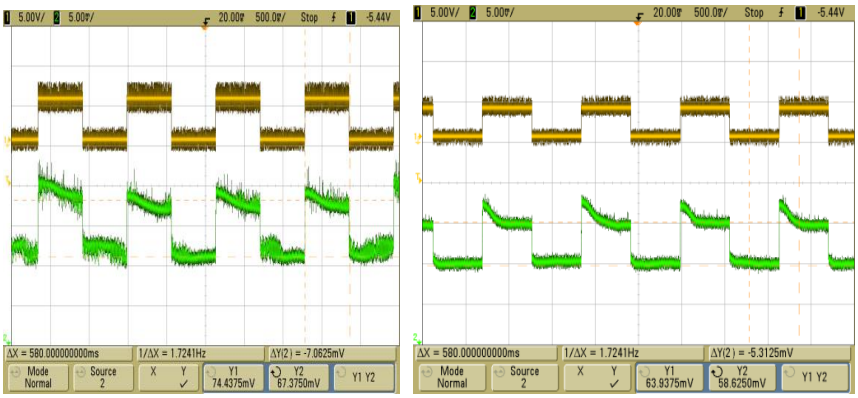


Figure 7. Optical Test System

Figure 8 shows observation results in oscilloscope, with 3.5V supply voltage and 5V supply voltage shown in Figure 8 (a) and Figure 8 (b) respectively. The top of each figure is driving voltage input, while the bottom is detecting results. When the modulator voltage changes between 0V and 3.5V, the detected signal intensity by detector is 58.6nV, the strength of modulation signal is 5.3 mV, modulation depth is 9%, and modulation frequency is 2 Hz. When driving voltage changes from 3.5V to 5V, modulation depth jumped to 7.1mV/67.4mV=10.5%. The results indicate that detection signal of detector coordinates well with driving voltage of modulator, therefore driving circuit can control the modulator to modulate the optical signal.



(a) (b)

Figure 8. The Detector Output with the Change of the Driving Voltage

4. Conclusion

A two-level gray-scale driver circuit of MQW SLM is designed in this paper. It can produce high and low two-level driver voltage, the pixel is designed to a latch unit with two inverters in cascade. The testing results show that the detection signal from the detector and the driving voltage of the modulator followed very well, the driver circuit can control modulator optical signal modulation.

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