International Journal of Future Generation Communication and Networking
Vol. 9, No. 12 (2016), pp. 395-404
http://dx.doi.org/10.14257/ijfgcn.2016.9.12.36

RF Transceiver Circuit FPGA Program Design and Development

Ruiqiang Liu[1]* and Fengmei Gao[2]

[1]*Chongqing College of Electronic Engineering, Chongqing, 401331, China*
[2]*Xinxiang Medical University, Xinxiang, Henan, 453003, China*
E-mail: ruiqiang.liu@aliyun.com, gfmemail@126.com

Abstract

As the communication technology is developing rapidly and the communication system and standard are updated constantly, people proposed the concept that the virtual radio is realized through software to achieve the interconnection among equipment. The paper shows the basic structure and module composition of virtual radio RF front-end, highlighting the key technology for hardware design of the whole RF front-end as well as the FPGA local control logic. The hardware, consisting of FPGA module and its control module, is provided with the relative design of circuit diagram. Moreover, the tests on RF front-end board are presented in the paper, proving that the board has favorable commonality to serve as the RF front-end for receiving and sending of wireless signals in software radio system, being used as wireless access card device and wireless system experiment device, and for building the industrial private communication system.

Keywords*: video circuit, FPGA, program design, wireless communication*

1. Introduction

In this society of fast-pace development, people have more and more request on wireless communication [1]. The wireless communication has become more and more important in the modern communication, varying from single-function single-band mode to multi-function multi-band mode. As for traditional wireless communication, the digital signals are processed completely by the DSP of hardware [2]. Once the demand is different, the hardware system will also be changed accordingly, thus the cost of wireless communication system will be increased, the flexibility and commonality will be become poorer, furthermore the demand of increasingly developing wireless communication protocol cannot be satisfied [3].

The virtual radio is a new tendency of the software radio. It is a technical method that uses the computation capacity of universal PC to realize multiple wireless communication functions, and further achieve software-based wireless communication system through combining the universal RF front-end [4]. The virtual radio differs from the software radio mainly because the rapid and advanced workstation device is selected for the virtual radio instead of the DSP device, besides, the special device is replaced by the universal computer to achieve all functions, and only the software programming of the computer is used for the processing of digital signals, boasting better flexibility, commonality and openness than the software radio structured by special programmable device [5].

2. Structure of Virtual Radio RF Front-end

2.1. Structure of Virtual Radio

Research purpose of virtual radio system: the AD/DA conversion part and other hardware are placed as close to the antenna as possible, or the conversion from the hardware to broadband RF signal is mainly performed firstly, and then the converted date

ISSN: 2233-7857 IJFGCN

will be transferred to the controlling terminal (PC or workstation) through high-speed transmission channel, finally the other radio functions will be realized on the controlling terminal through the software program [6].

The hardware of wireless radio is constituted by the RF front-end of multi-band, and the RF signal will be converted into IF signal in the RF band scope, next the IF signal will be converted into AD and the digital signal is transferred to the main memory of the controlling terminal for processing and the realizing receiving function. The digital signal is transmitted to the RF front-end through the controlling terminal, and will be emitted by antenna after being converted into analog signal from DA to achieve the emission function. The processing of IF and the below is realized through software [7-8].

The basic framework of virtual radio is shown in Figure 1:

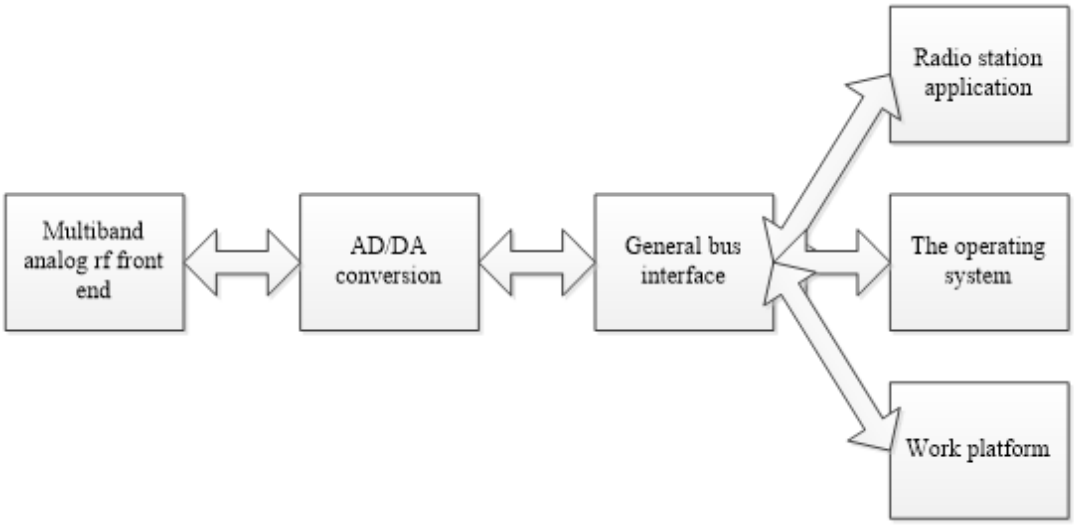

Figure 1. Basic Structure of Virtual Radio

2.2. Key Technologies of Virtual Radio

In virtual radio system, the analog signal collected by antenna of RF front-end is converted into digital signal thorough AD converter and transmitted to the main memory of the computer via universal interface, and at this moment a RX process is finished. In contrast, the data in main memory of the computer is transmitted to DA converter and converted into analog signal, and then emitted by antenna, and at that time a TX process is finished. The process of sending the collected data to the main memory of the computer is regarded as DMA (direct memory and access) method [9]. In order to realize this function, the universal I/O bus interface system is needed to be developed and the programmable application environment should be constructed, and these are the two key technologies for building up virtual radio of the computer [10].

(1) According to the demand of performance, the PCI and PCI Express bus interface are relatively proper universal I/O bus interface for the virtual radio system [11]. PCI Express is the updated version of PCI interface, which at most can support 32 transmission channels with the basic transmission rate of 2.5Gbps for each. As the transmission delay is leveled as microsecond, the LTE and Wi Max can meet the demand of most of communication protocol [12].

(2) The programmable environment should support the real-time and self-adaptable data processing capacity [13]. In the below are the working principles: from the input to output of the controlled process, the data process is from input to output. Only when the uploading module needing data will the downloading module start to process to minimize the total processing capacity. Furthermore, the cache memory is fully used to propose the

data for each module, so as to greatly reduce the processing delay of the signal and realize the instantaneity [14].

2.3. RF Front-end Structure

Because virtual radio is a multi-band, multi-protocol and multi-function wireless communication system, the RF front-end shall be networked with multi-band configurable channels, and the different protocols and functions may be existed simultaneously [15]. The virtual video system is configured through switch network, in which the broadband RF front-end of each branch may be involved in any functional tread of the system. Therefore, the broadband RF front-end of each branch should support the signal transmission of multiple debugging means of the multi-function system. The structural diagram of multi-access RF front-end is shown in Figure 2.

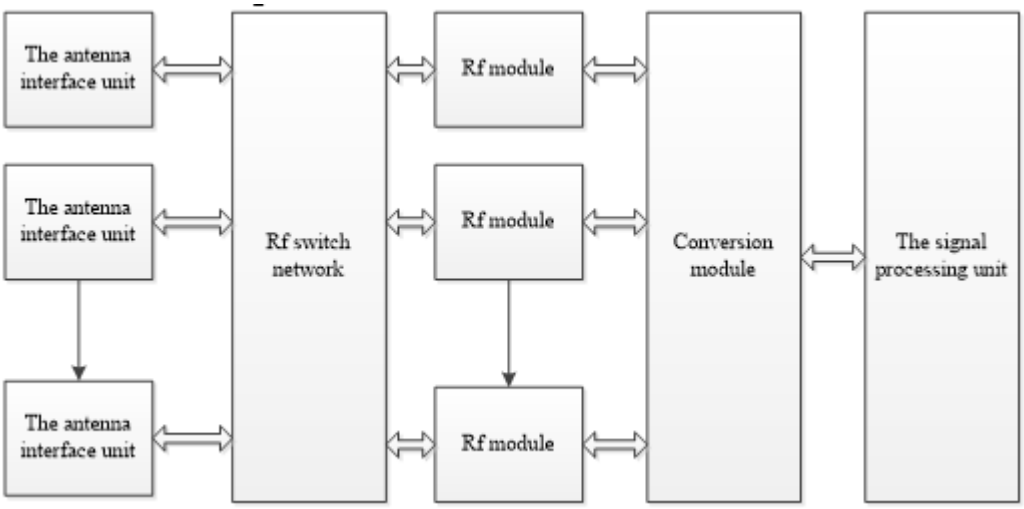

Figure 2. The rf Front-end Structure

Common RF front-end structure is composed of direct conversion RF front-end structure and low IF front-end structure.

(1) Direct conversion RF front-end structure

The direct conversion RF front-end structure is also called as zero IF structure that can work out the conversion between IF signal and baseband signal, not needing the multiple conversions [16]. Compared with super heterodyne structure, the direct conversion structure is simple with fewer devices, becoming easier for integrating in the circuit. The entire covering area of PCB is decreased [17]. The structural diagram of typical direct conversion RF front-end is shown in Figure 3:

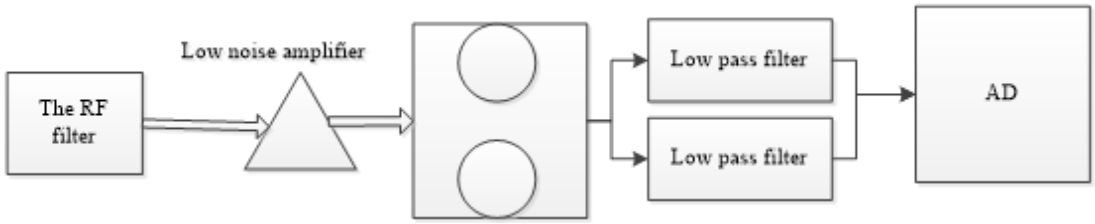

Figure 3. Direct Frequency Structure of rf Front End

(2) Low IF front-end structure

The low IF structure not only has the good performance of super heterodyne structure, but also combine the easy-integration advantage of the direct conversion structure. As for

the processing of low IF band, the easy-integrated band-pass filter is used as the post-frequency filter. The low IF structure maintains its high performance also because it is not sensitive to noise, LO signal leakage, DC deviation and other problems [18]. The structural diagram of low RF front-end is shown in Figure 4:

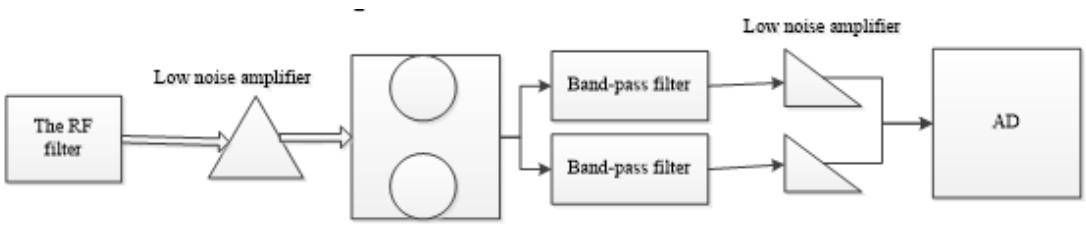

Figure 4. Intermediate Frequency rf Front-end Structure

3. Overall Hardware Design Scheme

The RF front-end based on virtual radio is mainly composed of five modules, including FPGA module, power supply module, clock module, PCIe interface module and RF module. Distribution of those modules is shown in Figure 5:

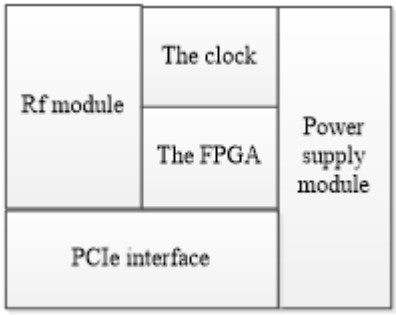

Figure 5. Hardware Module distribution as a Whole

Main functions of those modules:

(1) FPGA module: parameter setting of chips, buffering treatment of data, management of overall data transmission flow, and management of PC high-speed data interface.

(2) Power supply module: the main power supply is at 12V, and in total five power supply conversion modules are aligned for management of solid-plate power supply.

(3) Clock module: providing clocks of FPGA module and RF module.

(4) PCIe interface module: for data interacting interface with PC.

(5) RF module: the RF module integrates two RF channels, and both of them have the receiving and sending functions.

The overall hardware framework of RF front-end is shown in Figure 6:

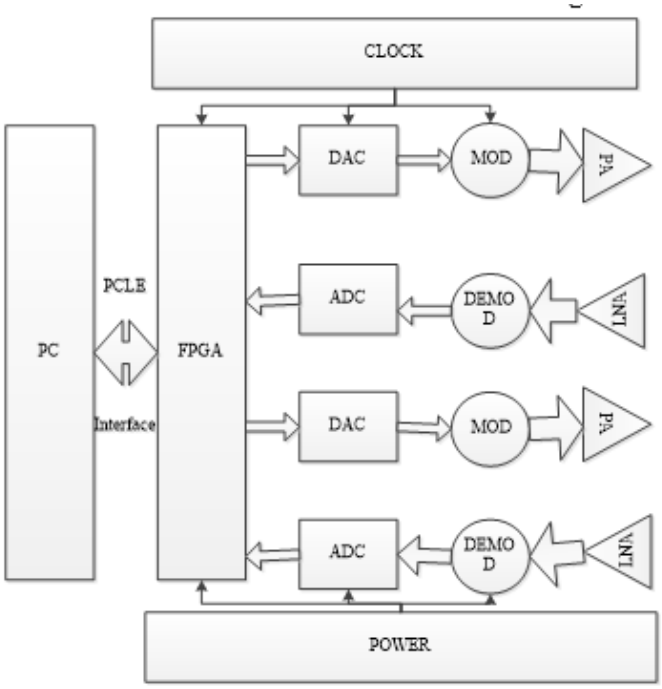

Figure 6. Rf front-end Hardware Structure Diagram

4. FPGA Program Design and Realization of Virtual Radio Front-end

4.1. General FPGA Design Scheme

Provide high-speed data channel PCIe interface during data transmission between CPU memory and RF ADC/DAC. PCIe is a point-to-point interconnection agreement and has high bandwidth data transmission performance with high reliability, which helps to meet the requirement for low delay of communication system. Besides the basic high speed data transmission performance, FPGA is also responsible for relevant configuration of RF, such as RF transceiver switch, transmission power control, receiver gain adjustment, startup and shutdown of PA and LNA and switch method of RF antenna. In accordance with the RF front-end design requirements, FPGA mainly achieves the following functions:

(1) Support high speed data transmission of PCIe×8 and achieve efficient DMA transmission mechanism and ADC data collection and DAC data transmission of two LMS6002D chips.

(2) Support the timing function and regular or irregular RF switch and insert the timing information into data and transmit it to PC by PCIe.

(3) Support data collection and transmission of two antennas, *i.e.* double-emission and double-receiving, and also support the single-emission and single-receiving mode.

(4) Support SPI parameter configuration of two LMS6002D chips and SPI parameter configuration of clock chip CDCE62005.

The Paper divides the FPGA program design into the following main modules in accordance with the functions, that is PCIe IP Core, DMA_CTRL module, ANT_SEL module, FIFO literacy control between TX/RX module, data collection (ADC) and data transmission (DAC) of two LMS6002D chips, timing control module and parameter configuration module.

Functions of each module are described as follows:

PCIe Core: achieving a high speed data port between the RF front-end and PC.

DMA_CTRL module: DMA:Control module, including TX_Engine, RX_Engine and BMD_CTRL and achieving an efficient transmission mechanism.

ANT_SEL module: antenna selection module. Controlling the two antennas, achieving RF transceiver switch and selection of LMS6002D chips

FIFO between TX/RX modules: achieving buffering of data receiving and transmission.

Timing control module: achieving startup and shutdown in a timing way, uploading timing information and completing the timing switch function.

Parameter configuration module: achieving initial configuration for chip parameters and supporting correcting the chip parameters on PC directly.

4.2. Design and Achievement of FPGA Functional Modules

(1) FPGA design of DMA_CTRL module

DMA_CTRL module is an important part of the whole RF front-end system, controlling the whole process of RF front-end transmission and receiving. It can achieve efficient DMA transmission mechanism; meanwhile, it can control the functional modules of other parts of FPGA: timing control module and parameter configuration module. In the DMA_CTRL module, TX_Engine module, RX_Engine module and BMD_CTRL module are included.

(2) FPGA design of ANT_SEL module

The main function of ANT_SEL is to control antennas. There are two LMS6002D chips in total at the RF front end in the Paper, and meanwhile, each chip uses an antenna and achieves various working modes of the RF front end by controlling the antenna, such as one transmitting antenna and one receiving antenna, two transmitting antennas and two receiving antennas, simultaneous transmission and reception and simultaneous stopping. See Table 1 for configuration modes of double antenna:

Table 1. Double Antenna Configuration Mode

Register	Address	Ant-sel-model	Function
REG22	58-5B	00	Effective(LMS6002D-0), Antenna(0)work
		01	Effective(LMS6002D-1) Antenna(1)work
		10	Antenna(1 and 0)work
		11	Antenna(1 and 0)stop work

(3) FPGA design of timing control module

Data interaction of PC and FPGA is achieved through PCIe interface. There is time delay for data transmission in PCIe interface, and the exact value of the delay time cannot be obtained and the delay time consumed in each data transmission process is different, therefore, to achieve the simultaneous data transmission and reception performance in a high speed operating system, it is necessary to add the timing control.

Relevant operation of timing control mainly includes timing transmission start and stop and timing receiving start and stop. The four types of operation correspond to four registers of DMA. The four timing processes are independent from each other; therefore, each timer corresponds to a timing module and executes relevant RF operation after time is out. Meanwhile, relevant timing operation can also be explained as control of timing switch of RF receiving and transmission states. After initialization of the system, set the initial state of RF front-end as a receiving state. See Table 7 for state transfer:

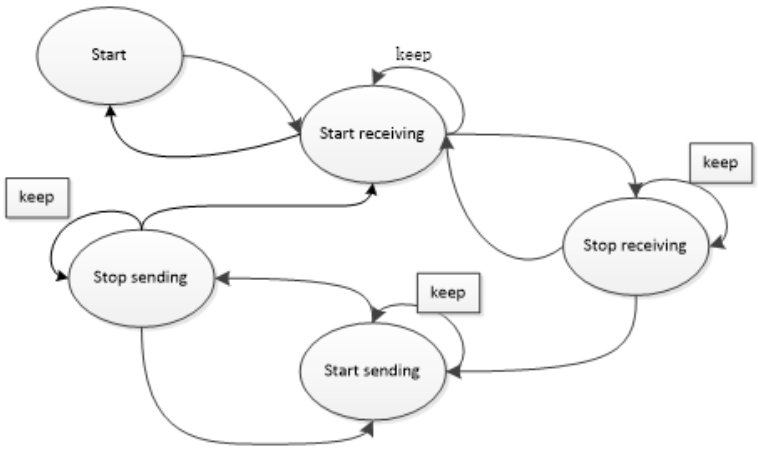

Figure 7. Timing Control State Transition Diagram

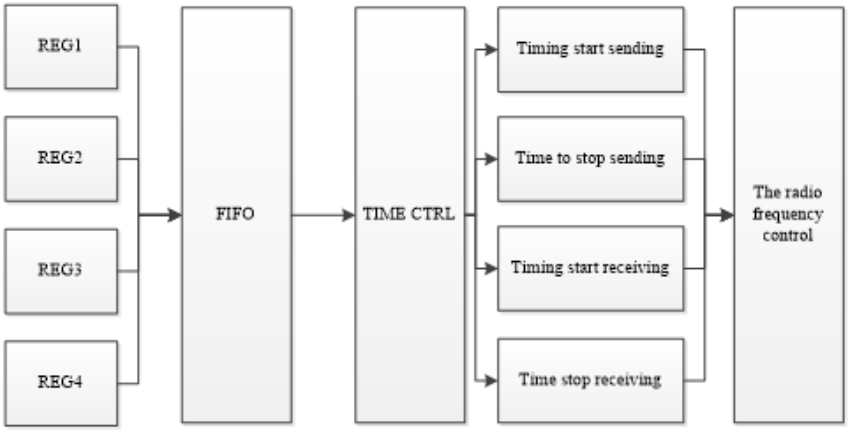

Figure 8. Timing Control Principle

What is shown in Figure 8 is a timing control diagram. Firstly, timing values are written in FIFO through a register and the system clock 250MHz is adopted for the part; TIME_CTRL module reads values in FIFO and carry out relevant operation in accordance with the timing value, and the timing control module achieves the timing control function through comparison between the current clock count value and moment value read from FIFO. The work clock of the part is 40MHz.

See Table 2 for list of timing-related DMA controllers:

Table 2. Timing Related DMA Control Registers

	Register	Address	Function
Send	REG1	60-63	Start sending
(TX DAC)	REG2	64-67	Stop sending
Receive	REG4	68-6B	Start receiving
(RX ADC)	REG5	6C-6F	Stop receiving

4.3. FPGA Design of Parameter Configuration Module

FPGA supports configuring two LMS6002D RF transceiver chips and a CDCE62005 clock chip through SPI serial interface. FPGA carries out initial configuration for the three chips after resetting. After entering normal operation after resetting, the system will

firstly write the initialization parameters of the required configuration into FIFO through writable registers and then read parameters gradually from FIFO for chip configuration. This method can reduce the consumption of FPGA resource and improve system stability. See Figure 9 for flow diagram of initial configuration:

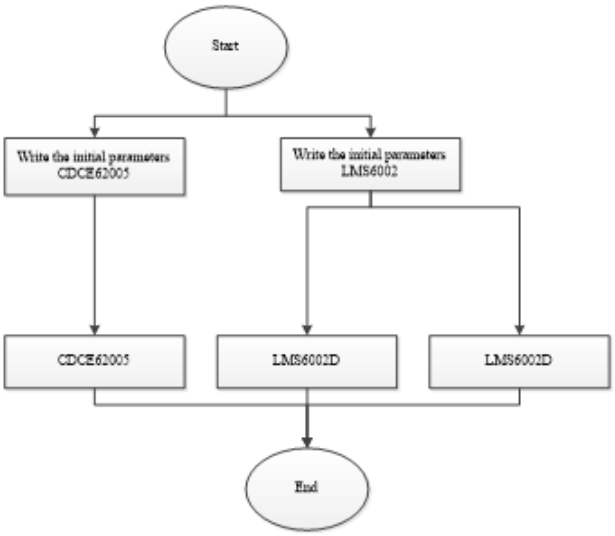

Figure 9. The Flow Chart of the Initialization Configuration

In the process of system debugging, chip parameters need modifying. The method of initialization parameter modification will undoubtedly increase a large amount of work. Each modification will cause recompilation of program, and also it will take a long time to compile once. Therefore, the method is not desirable. The Paper supports the method of directly modifying chip parameters on PC, writing the configured parameters into FIFO of FPGA through read-write shift registers and configuring them to the corresponding chips from FIFO. The process is similar with the initial configuration process. See Table 3 for relevant control registers of configuration parameters.

Table 3. Parameter Configuration Control Registers

Register	Address	Function
REG28	70-75	CDCE62005
REG29	78-81	LMS6002D

5. Test and Analysis of Virtual Radio RF Front-end

The following conclusions are drawn by analyzing test data in the table 4:

The designed virtual radio RF front-end transmitting terminal has a good transmission signal at middle-frequency band (700MHz-900MHz) and the receiving terminal has a good receiving performance at the overall frequency band. The lower the frequency is, the better the sign receiving quality is.

The signal quality of the transmitting terminal is good and the EVM is mainly caused by two aspects, one being IQ unbalance and LO leakage brought by the direct up-conversion scheme adopted for the RF front-end part, and the other being the linearity shortage of power devices.

Table 4. EVM

The center frequency	Launch	Receive

point		
300MHz	-29.35dB	-24.12 dB
500 MHz	-28.45 dB	-25.68 dB
700 MHz	-27.12 dB	-25.89 dB
1300 MHz	-31.65 dB	-27.65 dB

The signal part of receiving terminal is influenced by noise and there are discrete points appearing around each constellation point. The system noise is mainly from interference of clock chip and power part to RF and partially from the noise of device at the RF front-end and RF matching problem. To provide system sensitivity, carry out layout and wiring optimization for the clock part of the system, increase RF part shielding, improve the layout and wiring pattern of RF ends and try to reduce noise factors brought by the RF front-end.

6 Conclusions

The Paper has introduced the design of virtual radio RF front-end based on FPGA in detail from two aspects-hardware architectures and software design, including hardware platform design of RF front-end and design and achievement of module functions of FPGA, and has given test results of the hardware platform. The RF front-end designed in the Paper has good commonality, and can work under multiple communication protocols such as LTE, Wi Max, 802.11a/b/g and CMMB and also can modify the RF front-end FPGA program in accordance with different demands to achieve protocol switching. The hardware platform can also be used in a software radio system for data collection, and can be used as a special communication network system of industries, wireless access card device, instrument and device test equipment and wireless system experiment equipment.

Acknowledgment

Project Supported by Scientific and Technological Research Program of Chongqing Municipal Education Commission (Grant Nos. are KJ1602907 & KJ1602901).

References

[1] T. S. Mak, G. Rachmuth, K. P. Lam and C. S. Poon, "A component-based fpga design framework for neuronal ion channel dynamics simulations", IEEE Transactions on Neural Systems & Rehabilitation Engineering, vol. 14, no. 4, **(2006)**, pp. 410-418.
[2] E. Monmasson and M. N. Cirstea, "Fpga design methodology for industrial control systems—a review", IEEE Transactions on Industrial Electronics, vol. 54, no. 4, **(2007)**, pp. 1824-1842.
[3] S. Jin, J. Cho, X. D. Pham, K. M. Lee, S. K. Park and M. Kim, "Fpga design and implementation of a real-time stereo vision system", IEEE Transactions on Circuits & Systems for Video Technology, vol. 20, no. 1, **(2010)**, pp. 15-26.
[4] S. Roy and P. Banerjee, "An algorithm for trading off quantization error with hardware resources for matlab-based fpga design", IEEE Transactions on Computers, vol. 54, no. 7, **(2005)**, pp. 886-896.
[5] Y. W. Chang, D. F. Wong and C. K. Wong, "Universal switch modules for fpga design", Acm Trans Design Automation of Electronic Systems, vol. 1, no. 1, **(1996)**, pp. 80—101.
[6] D. Chen, J. Cong and P. Pan, "Fpga design automation: a survey", Foundations & Trends in Electronic Design Automation, vol. 1, no. 3, **(2006)**, pp. 139-, 2006.
[7] J. Valls, M. Kuhlmann and K. K. Parhi, "Evaluation of cordic algorithms for fpga design", Journal of Vlsi Signal Processing, vol. 32, no. 3, **(2002)**, pp. 207-222.
[8] K. R. S. Shayee, J. Park and P. C. Diniz, "Performance and area modeling of complete fpga designs in the presence of loop transformations", IEEE Transactions on Computers, vol. 53, no. 11, **(2003)**, pp. 1420-1435.
[9] J. Cong and Y. Y. Hwang, "Structural gate decomposition for depth-optimal technology mapping in lut-based fpga designs", Acm Transactions on Design Automation of Electronic Systems, vol. 5, no. 2, **(1996)**, pp. 726-729.

[10] J. Liu, Y. V. Zakharov and B. Weaver, "Architecture and fpga design of dichotomous coordinate descent algorithms", Circuits & Systems I Regular Papers IEEE Transactions, vol. 56, no. 11, **(2009)**, pp. 2425-, 2009.
[11] R. Foist, A. Ivanov and R. Turner, "An fpga design project: creating a powerpc subsystem plus user logic", IEEE Transactions on Education, vol. 51, no. 3, **(2007)**, pp. 312-318.
[12] A. Kumar and M. Anis, "Fpga design for timing yield under process variations", Very Large Scale Integration Systems IEEE Transactions on, vol. 18, no. 3, **(2010)**, pp. 423-435.
[13] T. S. Mak, G. Rachmuth, K. P., Lam and C. S. Poon, "A component-based fpga design framework for neuronal ion channel dynamics simulations", IEEE Transactions on Neural Systems & Rehabilitation Engineering, vol. 14, no. 4, **(2006)**, pp. 410-418.
[14] U. Meyerbaese and A. Meyerbaese, "Discrete wavelet transform fpga design using matlab/Simulink", Proceedings of SPIE - The International Society for Optical Engineering, 624703-624703-10, **(2006)**.
[15] S. Roy and P. Banerjee, "An algorithm for converting floating-point computations to fixed-point in matlab based fpga design", **(2004)**, pp. 484-487.
[16] G. M. Wu, M. Shyu and Y. W. Chang, "Universal switch blocks for three-dimensional fpga design", IEE Proceedings - Circuits Devices and Systems, vol. 151, no. 1, **(2004)**, pp. 49-57.
[17] A. Plaza, "Fpga design and implementation of a fast pixel purity index algorithm for endmember extraction in hyperspectral imagery", Proceedings of SPIE - The International Society for Optical Engineering, 5995, 599508-599508-10, **(2005)**.
[18] G. Chiurco, M. Mazzotti, F. Zabini and D. Dardari, "Fpga design and performance evaluation of a pulse-based echo canceller for dvb-t/h", IEEE Transactions on Broadcasting, vol. 58, no. 4, **(2012)**, pp. 660-668.

