International Journal of Future Generation Communication and Networking
Vol. 9, No. 10 (2016), pp. 327-338
http://dx.doi.org/10.14257/ijfgcn.2016.9.10.28

A Heterogeneous Multi-core DSP Architecture for OFDM-Based Communication Systems

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Abstract

As a kind of wireless communication system, OFDM systems are widely used in the current and next generation wireless communications. According to the characteristics of OFDM systems, this paper proposed a new heterogeneous multi-core DSP architecture for OFDM system - HeteroM-DSP. Hetero M-DSP based on VLIW DSP core, which has good Data-Level Parallelism and Instruction-Level Parallelism. Each independent DSP core through sharing memory, task scheduling bus and bus controller based open-ring interconnection, improve the communications parallelism between DSP cores. Meanwhile, in order to implement different OFDM systems flexibly, each DSP core has different computational capabilities. It is also improved processor performance/ power rate. Experimental results for the IEEE 802.11a receiver show that Hetero M-DSP can efficiently use for OFDM systems.

Keywords*: Heterogeneous multi-core DSP; Open-ring interconnection; VLIW; Wireless communication baseband digital signal processing*

1. Introduction

In recent years, with continuous development of radio communication field, various communication standards emerge in endlessly and in the meantime standards for radio communication are becoming more and more complicated. By virtue of its high spectral efficiency and good anti-multipath interference ability, OFDM system has been extensively applied to the current and the next generation of radio communication systems such as WiFi, UWB and WiMax. In addition, more and more mobile devices are expected to support multiple protocols and standards, and mobile devices also need to meet certain power consumption indexes in instruction to guarantee service life. In instruction to adapt existing platforms to high-speed, diversification and complication tendencies of radio communication, people put forward the concept of software-defined radio (SDR). Software-defined radio is generally based on DSP [1] and flexibly realizes different radio communication standards through software upgrading and hardware units.

However, existing DSPs can't support OFDM system's requirements for computing power and power consumption. Firstly, general DSP is primarily designed by orienting at many digital signal processing fields, and it's hard for it to be optimized again according to specific applications [2]. While OFDM system has characteristics of synchronous data flow (SDF), and its algorithm has realized operations like a large quantity of complex operations and FFT, *etc*. Secondly, DSP needs to satisfy certain power consumption indexes while meeting processing requirements of communication system. Many software-defined radio platforms adopt multi-core architecture and hardware accelerator in instruction to realize high-speed operation while neglecting power consumption of multi-core DSP. In addition, although basic processing processes of different OFDM systems are the same, they have different requirements for DSP computing power and

ISSN: 2233-7857 IJFGCN

throughput, then DSP needs certain flexibility while guaranteeing throughput of the system.

Directing at characteristics of OFFDM system, this paper proposed a kind of heterogeneous multi-core DSP architecture- HeteroM-DSP used for OFDM system. HeteroM-DSP consists of DSP cores based on VLIW instruction set architecture with good instruction set parallelism and data-level parallelism. Each independent DSP core is interconnected through open-loop interconnection structure consisting of shared memorizer, task scheduling bus and bus controller, which improves parallelism of inter-nuclear communication of multi-core DSP. In the meantime, DSP cores have different computing power, making the processor be able to highly efficiently and flexibly realize various OFDM systems and further improve performance/power consumption ratio of the processor.

This paper is arranged as follows: chapter two introduces relevant work of multi-core DSP; chapter three briefly introduces baseband digital signal processing of OFDM system; chapter four specific ly expounds HeteroM-DSP architecture; chapter five, taking IEEE 802.11a as an example, displays design flow of HeteroM-DSP and performance and power consumption analysis of the processor; the final part is the conclusion.

2. Relevant Work

According to different varieties of DSP cores, multi-core DSP can be divided into isomorphic multi-core DSP and heterogeneous multi-core DSP [3]; According to different interconnecting modes among cores, it can also be divided into hierarchical bus network, mesh network and other interconnection structures [4], as shown in Figure 1.

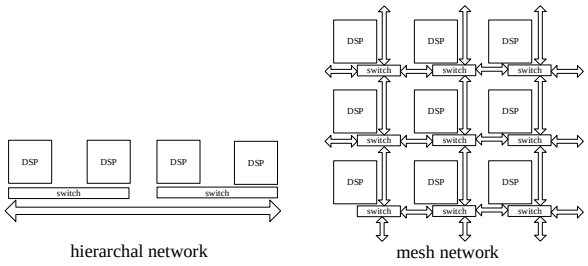

Figure 1. Mesh Network and Hierarchical Bus Network

TNETV3020 [13] multi-core DSP platform of Texas Instruments is mainly designed for application of streaming media transmission in radio communication field, the platform includes 6 TMS320C64x+DSP cores, and each DSP core can operate at 500Mhz. Application objective of SB3011[14] heterogeneous multi-core DSP platform of SandBridge is software-defined radio which includes one ARM processor cores and four DSP cores operating at 600MHZ, their cores are in bus-type interconnection, and SIMD instruction set architecture is used within cores to support vector operation in data flow. Literature [5] proposed a heterogeneous multi-core processor which adopted hierarchical interconnection structure. The processor was mainly designed for high-speed radio communication fields such as bit-level configurable unit, word-level configurable core and general programmable core. NoC (Network on Chip) featured by advanced prediction was adopted to accelerate intercommunication among processor cores, making multi-core processor have good flexibility and extendibility. Literature [6] designed a multi-core DSP for radio communication which adopted network structure and guaranteed time accuracy required during intercommunication in a way that DSP core operated at different frequencies.

It can be seen that different multi-core DPSs are a kind of optimization in architecture for this specific application. In other words, it’s necessary to design micro-architectures

such as instruction set architecture and interconnection structure of multi-core DSP by analyzing characteristics of different applications.

3. Baseband Digital Signal Processing of OFDM System

As shown in Figure 2, processing procedures of one typical OFDM system includes radio front end, ADC/DAC, baseband digital signal processing and MAC layer processing. Baseband digital signal processing is responsible for demodulating data frames after radio front-end analog-to-digital conversion into bit stream data to send to MAC layer (receiving end), or modulating bit stream data submitted at MAC layer into physical-layer data frames to send out through radio front end. DSP mainly conducts baseband digital signal processing in OFDM system. Baseband digital signal processing of OFDM system can be divided into three parts according to different processing intents.

Digital front end (DFE) part mainly conducts operations such as digital filtering and DC offset removing by directing at sampling values. Modem mainly includes modulation and demodulation while also including some synchronization techniques as well as estimation and equilibrium of information channel, frequency offset estimation and compensation, *etc*. This part involves a large quantity of complex sampling (I/Q pair) operations such as complex multiplication and relevant operations among complexes and FFT/iFFT, *etc*.

Codec executes operations of based on bit stream such as scrambling, interweaving, encoding (convolutional code, RA code, RS code, *etc*.), decoding (Viterbi decoding, min-sum decoding, *etc*.), *etc*.

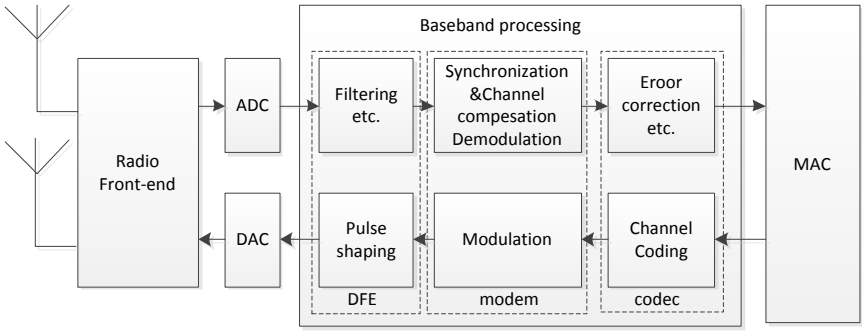

Figure 2. Processing Procedures of OFDM System

It can be seen from currently popular OFDM system (such as WiFi, WiMAX, *etc*.) that all baseband digital signal processing of various OFDM systems are processing process in which data flow takes a lead with characteristics of synchronous data flow (SDF) [16]. In the meantime, most calculations in baseband digital signal processing of OFDM system are conducted in interior circulation, while these algorithms have high data-level parallelism and instruction-level parallelism, and control flow is relatively simple [7]. Moreover, baseband digital signal processing of OFDM system based on IEEE 802.11a standard is analyzed; complex multiplication in the majority is a typical feature of baseband digital signal processing of OFDM system [1]. These features provide feasibility for multi-core DSP which is applied to OFDM system with high performance/power consumption ratio.

4. HeteroM-DSP Multi-Core Processor Architecture

Author names and affiliations are to be centered beneath the title and printed in Times New Roman 12-point, non-boldface type. Multiple authors may be shown in a two or three-column format, with their affiliations below their respective names. Affiliations are

centered below each author name, italicized, not bold. Include e-mail addresses if possible. Follow the author information by two blank lines before main text.

4.1. HeteroM-DSP

As shown in Figure 3, HeteroM-DSP mainly consists of DSP core used for intensive data processing, bus controller unit for task scheduling scratchpad memory. HeteroM-DSP is an architecture of optimized design which is applicable to radio communication field, and this architecture can provide flexible DSP core design (including computing power and quantity of DSP cores) under fixed interconnection structure among cores. Two neighboring DSP cores conduct data transmission through share memory, and each DSP core is connected to a bus control unit and complete transfer and reception of task scheduling information through this unit. Inside DSP core also includes a private memory unit used to store intermediate data generated during DSP program execution process in instruction to reduce visits of external memory and reduce total power consumption.

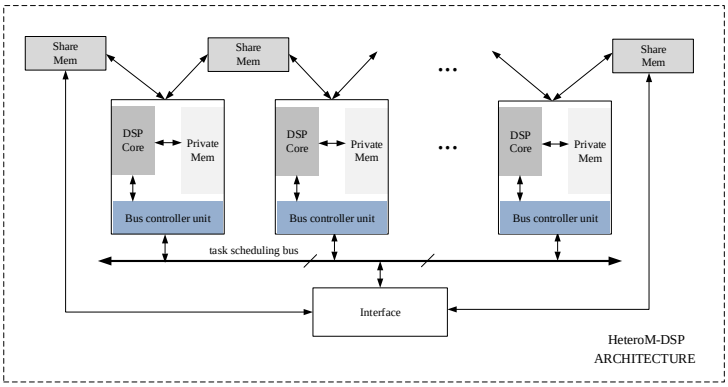

Figure 3. HeteroM-DSP Architecture

4.2. Open-Loop Interconnection Structure

As OFDM system has characteristics of synchronous data flow, inside its algorithm has strong parallelism, then when one DSP core obtains data needed in current execution, it can transfer data which have been processed to other DSP cores for next-step processing.

This paper adopted open-loop interconnection structure for HeteroM-DSP. Data transmission in open-loop interconnection structure is realized by share memory among DSP cores. In the meantime, OFDM system is a hard real-time system, so data transmission and algorithm execution need to be completed within a predictable period. In instruction to make parallel data transmission and program execution controllable to the programmer, this paper designed a task scheduling unit inside DSP cores.

Different from other interconnection structures, open-loop interconnection structure proposed in this paper has two features. Firstly, hardware implementation of open-loop interconnection structure is simple. Compared with hierarchical bus interconnection means, open-loop interconnection structure doesn't need to design complicated switch unit with increasing number of processor cores interconnected on multi-core processor, so it's of good extensibility. In the meantime, when the number of processor cores interconnected on multi-core processor is within a one range, multi-core processor adopting open-loop interconnection structure has better computing performance than that adopting mesh network [8]. Secondly, open-loop interconnection structure makes task scheduling of the programmer controllable. According to requirements of task scheduling, the programmer can realize task scheduling among DSP cores by compiling a task scheduling instruction.

DSP generates task scheduling information through bus control unit, and architecture of bus control unit is as shown in Figure 4. Bus control unit includes control logic, arbiter logic, FIFO memory and gate, *etc*., and it mainly realizes three functions:

1: If the left bus control unit sends arbiter signal and has applied for task scheduling bus, the current bus control unit will forward this arbiter signal to the right bus control unit. In the meantime, task scheduling information sent by left bus control unit will be saved into FIFO memory and forwarded.

2: If current DSP core needs applying for bus, it will send through control logic in bus control unit to arbiter logic, and then arbiter signal will be generated, in the meantime, it will forward current task scheduling information to the left and right bus control units.

3: If the left bus control unit has already applied for bus while the current DSP core also needs to apply for bus, the current control unit will save current task scheduling information, and only arbiter signal and task scheduling information of left bus are forwarded. After the left bus control unit finishes bus control, current arbiter signal and task scheduling information will be forwarded.

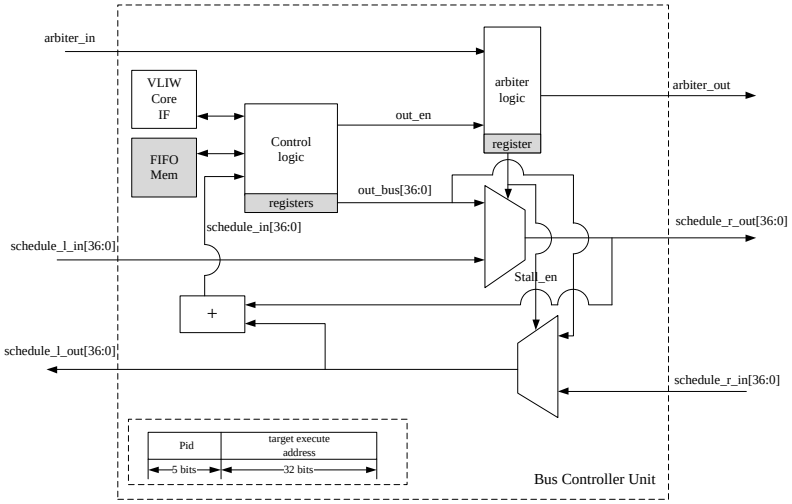

Figure 4. Architecture of Bus Control Unit

Task scheduling information, a kind of data with bandwidth being 37bits, is used to identify DSP core number needed in the next task and start address of program executed by DSP. Implementation of open-loop interconnection structure through share memory and bus control unit can effectively improve throughput of multi-core DSP and parallelism among multi-core DSP cores.

4.3. DSP Core Architecture

DSP core architecture is as shown in Figure 5 including f*etc*her, decoder, controller unit, data communication unit, computer unit and register bank, and it supports 32bits and 16bits fixed-point operations (why supporting the two operations). DSP cores adopt VLIW to coordinate with computer unit and memory control unit in implementing high instruction-level parallelism and data-level parallelism by executing multiple microinstructions within one cycle. Besides VLIW, Superscalar can also realize instruction-level parallelism of the processor. Superscalar adopts dynamic instruction distribution, and supports out-of-instruction execution, and implementation of dynamic instruction distribution needs complicated hardware unit. Different from Superscalar, VLIW depends on static instruction distribution of compiler, and the compiler needs to accurately stipulate specific executed operation of each functional unit within each instruction cycle. It's obvious that compared with Superscalar, VLIW lacks flexibility, but

hardware implementation sacrifice of VLIW is obviously less than that of Superscalar, and deficiencies of VLIW complier can be overcome through artificial compiled assemble program and instruction utilization efficiency can be improved. For this reason, currently most DSPs adopt VLIW instruction set architecture.

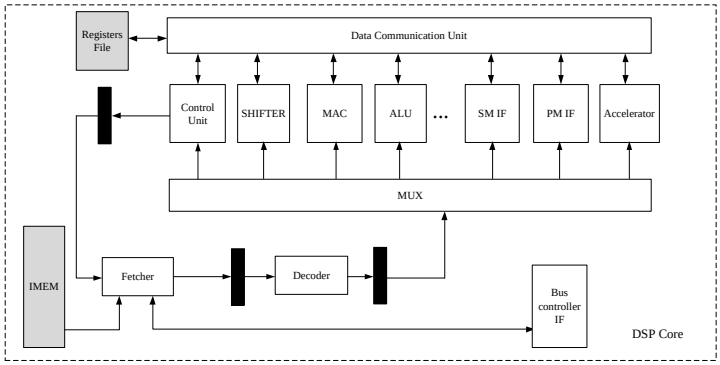

Figure 5. DSP Core Architecture

VLIW instructions on DSP cores not only include immediate slot, branch slot, control slot, private memory slot and public memory slot of fixed lengths but also include CU (computer unit) of unequal quantities as shown in Figure 6. Each CU slot is corresponding to a specific CU microinstruction. CU in DSP cores not only includes ALU arithmetic logic unit) but also include MAC (Multiply-Accumulator) and SHIFTER used for algorithms like complex operation and CORDIC in OFDM system. In the meantime, it can also add accelerating units used for specific processing according to requirements of OFDM system, such as Viterbi decoder, LDPC decoder, *etc*. Adopting different numbers of CU will influence length of VLIW instruction. The user can configure CU (number and kind) and form corresponding VLIW instruction sets when implementing specific DSP cores according to actual requirements of different protocols.

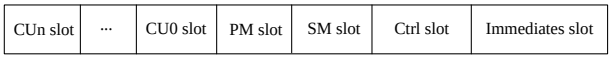

Figure 6. VLIW Instruction Structure

DSP cores finish execution of instructions through three-level pipeline-f*etc*h, decoding and execution. At f*etc*h stage, DSP cores f*etc*h instructions to decode according to value of PC register; at decoding stage, DSP cores decode instructions on instruction register and send decoding results to all CU and private memory controller and public memory controller; at execution stage, CU, private memory and public memory will execute corresponding actions. And at execution stage, each CU and memory control unit read-write register bank through data communication unit, while control unit will compute CU and then obtain address of the next instruction and write it back to PC register.

As different types of DSP cores can be implemented by changing CU kind and number when DSP cores are being designed, this kind of heterogeneous multi-core architecture can improve performance/power consumption ratio of HeteroM-DSP, and because some processing modules have high real-time requirements in OFDM system, it can be realized by designing high-performance DSP cores; while some processing modules have low real-time requirements, and this can be realized by DSP cores with low power consumption in order to satisfy power consumption requirements of the whole processing process. Heterogeneous multi-core architecture plays a non-negligible role in improving overall performance of HeteroM-DSP.

5. Assessment and Implementation

Taking baseband digital signal processing at receiving terminal of IEEE 802.11a as an example, hereby we further describe designing process of DSP cores on HeteroM-DSP architecture and mapping method of baseband digital signal processing on multi-core DSP. In the meantime, assembly language in HeteroM-DSP is used to compile processing modules at receiving terminal of IEEE 802.11a, and computing power of each DSP core is analyzed through a cycle-level precise instruction simulator. Verilog HDL is used to finish RTL-level implementation of HeteroM-DSP. HeteroM-DSP power consumption and area are assessed by a comprehensive tool and implemented by Xilinx Vietex4 FPGA.

5.1. Standard Receiving Terminal of IEEE 802.11a

As stated in IEEE 802.11a standard [12], baseband digital signal processing at receiving terminal includes: frame sync, fractional CFO, CFO compensation, integer CFO, guard remove as well as channel estimation, guard remove, 64-bit FFT, channel equalization, pilots remove, demodulation, de-interleave, de-puncture, Viterbi decofing, de-scramble.

This paper adopts task driven method to design DSP cores, and task refers to minimum processing process constituting the whole baseband digital signal processing, and task combination can constitute different processing modules in Figure 7. It can be seen by analyzing standard physical layer of IEEE802.11a that complex multiplication operations in these baseband processing occupy a major proportion. In addition, modules like FIR, CORDIC and cumulated summation repeat in baseband processing of different protocols, while these operations can also be split into processing modules equivalent to calculated amount of complex multiplication. Hence, we finally limit task granularity within the scope which is approximate to calculated amount of linear complex multiplication.

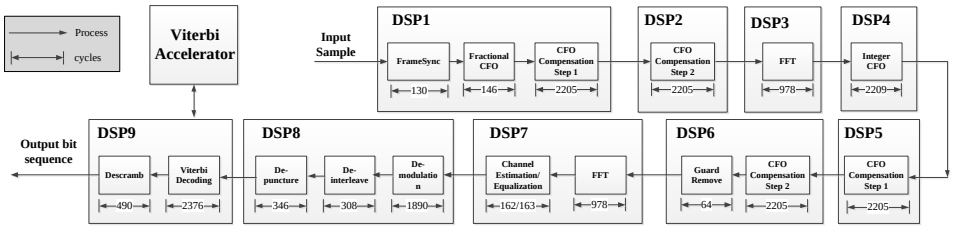

Figure 7. Mapping of Baseband Processing at Receiving Terminal of IEEE.802.11a on Multi-Core DSP

According to characteristics of complex multiplication, the task needs to meet the following conditions:

(1) As complex multiplication needs 4 input data, we limit data input of task within 4 ones.

(2) The task should implement functional modules in baseband processing by means of internal auto cycle. For example, when implementing complex multiplication operation, multi-group complexes can be implemented by cyclically using complex multiplica-tion. Parallel execution is possible among the same tasks or different tasks.

(3) As the shortest execution time of single complex multiplication on HeteroM-DSP is 8 cycles, we select 12 cycles as upper limit of task execution time (execution time also includes data input & output time) on HeteroM-DSP.

It can be seen by analyzing baseband processing at receiving terminal that receiving terminal of IEEE 802.11a mainly includes 4 different types of tasks as shown in Table 1.

Table 1. Task Types in Baseband Processing at Receiving Terminal of IEEE 802.11a

No.	function	input	output	cycle
1	Complex Multiplication	4	2	5
2	Four Figures Adding Operation	4	1	3
3	One-Route Operation in Butterfly Pattern of Baseband 2	4	2	8
4	First-Order CORDIC	4	3	8

Table 2. DSP Cores in Heterogeneous Multi-Core DSP

DSP Core	CU Number and Kind
Core1	4alu+2mac+2shifter
Core2	
Core5	
Core6	
Core3	2alu+2mac+2shifter
Core7	
Core4	1alu+2mac+1shifter
Core8	
Core9	1alu+1shifter+Virtebi Accelerator

Processing modules in baseband digital signal processing at receiving terminal are implemented through combination of these tasks, and this paper has designed HeteroM-DSP with 9 DSP cores, computing performance of each DSP core is as shown in Table 2. Finally mapping of baseband processing at receiving terminal of IEEE 802.11a on multi-core DSP is as such: processing modules are mapped onto HeteroM-DSP, the whole receiving-terminal baseband digital signal processing is implemented through coarse-grained pipeline execution among DSP cores as shown in Fiugre 8. After figure 1 finishes processing modules mapped onto Core1, it can transmit them to Core2 to finish the next processing module. And at this time, Core 1 can conduct the next data processing. The rest can be done in the same manner, and different data can be processed with coarse-grain execution among DSP cores, which can improve processing speed of HeteroM-DSP for the whole receiving-terminal baseband digital signal processing as well as average utilization rate of DSP cores.

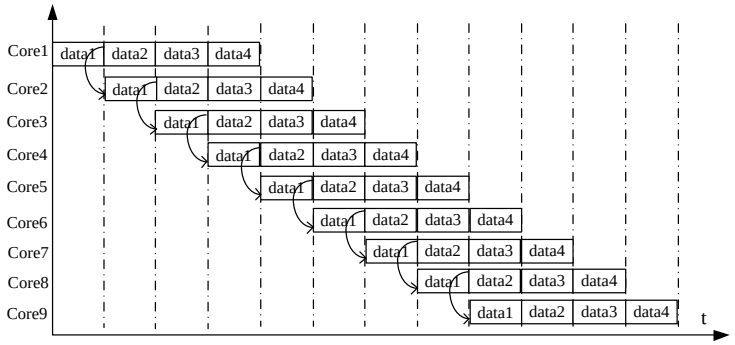

Figure 8. Coarse Pipeline Execution among DSP Cores

5.2. Assessment of Performance and Power Consumption

Sampling is represented by 1 pair of 32 bits fixed-point integers. In the meantime, as execution time of CFO Compensation processing module is quite long, we split it into two parts which are respectively mapped onto different DSP cores. In addition, in order to improve HeteroM-DSP performance, Viterbi decoding is implemented by hardware accelerator. Here, five processing modules (Fractional CFO, CFO Compensation, 64-FFT, Demodulation and De-Puncture) under the most complicated 54Mbps transmission rate (64 QM modulation mode, 3/4 convolutional code rate) are taken as testing examples to compare HeteroM-DSP and other processors in computing performance.

AsAP is a isomorphic multi-core DSP used for software radio and proposed by Davis branch of University of California. Implementation results of various modules on AsAP are obtained according to Literature [15]. In addition, FFT is implemented by hardware accelerator in AsAP. Implementation on Intel processor is based on Intel I7-920. In the meantime, for some testing example, SSE instruction sets based on SIMD instruction set architecture are used to conduct acceleration processing. Processing time of different processors when processing testing examples is as shown in Table 3. Test modules on AsAP operate on single processor core, and test modules on Intel processor operate on single processor by means of single thread. As HeterM-DSP is heterogeneous multi-core DSP, experimental results as shown in Figure 7 map the time used for processing these test modules on DSP cores.

Compared with AsAP, each processor core on HeteroM-DSP has a certain performance elevation when processing modules in OFDM system. While compared with Intel processor, performance of each processor core on HeteroM-DSP is basically approximate to that of Intel processor when processing 64-FFT and Demodulation, but the performance is obviously superior to that of Intel processor when processing other examples. Moreover, as HeteroM-DSP has 9 processor cores, it has better parallel processing capacity than 4-core I7-920. Experiment shows that HeteroM-DSP is applicable to OFDM system.

Table 3. Processing Time Comparison of Different Processors When Implementing Key Algorithms at Receiving Terminal of IEEE 802.11a (Unit: Cycle)

Module	AsAP	Intel	HeteroM-DSP
Fractional CFO (CORDIC Implementation)	183	497	146
CFO Compensation (CORDIC Implementation)	15120	14380 (SSE)	4410

64-FFT Adopt baseband 2 butterfly pattern to implement)	205 (Accelerator)	953 (SSE)	978
Demodulation (De-64QAM)	2352	1755	1890
De-Puncture	576	885	346

In the meantime, we select FreePDK [11]45nm-technology standard cell library to integrate HeteroM –DSP (memory part not included) through Synopsys Design Compiler tool. And we conduct the implementation on Xilinx Vietex4 FPGA hardware platform as shown in Figure 9, and use 2 FPGAs to respectively complete receiving terminal of sending terminal of IEEE 802.11a. Multi-core DSP operating at above 400Mhz can satisfy time regulation of IEEE.802.11a protocol. Under 400Mhz processor frequency and 1.1v global voltage, power consumption and area of each DSP core is as shown in Table 4, and it can be seen that overall power consumption of HeteroM-DSP is 1305.96mW and its area is 3.43mm2.

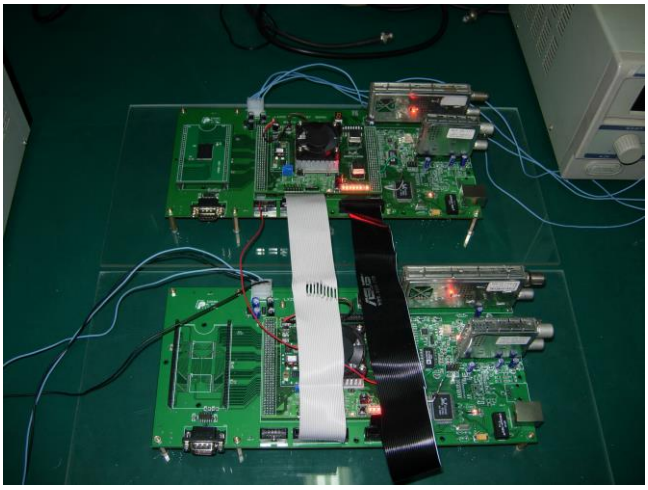

Figure 9. FPGA Implementation Platform

Table 4. Power Consumption and Area of DSP Cores when 45nm Technology and 1.1V Supporting Voltage Operate At 400MHZ (Unit: mW, mm2)

DSP Core	1	2	5	6	3	7	4	8	9
Power	181.95				139.44		102.56		94.16
Area	0.46				0.38		0.29		0.25

6. Conclusion

Directing at characteristics of OFDM system, this paper proposed a kind of heterogeneous multi-core DSP architecture--HeteroM-DSP used baseband digital signal processing in radio communication. HeteroM-DSP consists of DSP cores based on VLIW instruction-level architecture. Each independent DSP core is interconnected through open-loop interconnection structure consisting of share memory, task scheduling bus and bus controller. In addition, each DSP has different computing power according to features of OFDM system. Assessment and implementation results show that processing capacity of HeteroM-DSP is superior to

some existing multi-core DSPs and general processors, and it can be highly efficiently applied to OFDM system.

Acknowledgments

This work was supported by the follows: National Natural Science Foundation of China (61502256), Zhejiang Provincial Natural Science Foundation of China (LY15F020011, LY12F01002), Foundation of Zhejiang Educational Committee of China (Y201327685, Y201224456).

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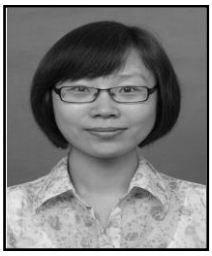

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