

Exploiting the Routing Efficiency for DMesh Networks

Xinyu Wang^{1a}, Tingting Han^{1b} and Haikuo Liu^{1c}

¹*College of Management Science and Engineering, Dongbei University of Finance and Economics, Dalian, China*

^a*distribute_2008@163.com; ^btingtinghan_2015@163.com; ^chaikism@hotmail.com*

Abstract

A rising horizon in on-chip interconnection is the design of high-radix routers as the ever increasing pin bandwidth. Compared to mesh, DMesh introduces many crossing physical channels, and effectively lower down the diameter and average distance, which directly influence performance of the overall chip. However, the original algorithm DXY could not efficiently make use of physical channels, as it always prefers to use the crossing links. In this paper, we present a novel deadlock-free and livelock-free routing algorithm based on DMesh network in order to make better use of different channels. Moreover, the new scheme can be used to both wormhole and virtual-cut-through switched networks. Extensive simulation results validate the effectiveness of novel proposed routing scheme as compared to the original DXY routing, originally proposed for DMesh networks.

Keywords: *on-chip network, DMesh, routing algorithm, deadlock-free, livelock-free*

1. Introduction

With semiconductor technology scaling, it has enabled the integration of many different intelligent IP cores into a single chip [1]. With the proliferation of NoCs, it devotes to an important role in determining the overall performance and power consumption of the entire chip.

An NoC consists of a number of interconnected heterogeneous elements [2], and these devices need to communicate with each other efficiently. Communication between different devices is achieved by sending packets through the fundamental on-chip communicating network. Typically, such an NoC is usually characterized by three primary design parameters: topology, routing, and flow control.

The network topology defines the number and placement of routers, the number of physical links and the connectivity among those routers. Once established, some physical properties of the network will be fixed, such as network diameter, average hops, and minimal distance between any two routers, bisection bandwidth, bisection link count. These properties establish the basic bounds for overall network performance and network cost [3].

The flow control technique governs communication between routers. Particularly, it determines when packets (or flits) can be forwarded from the current router to the downstream one. Consequently, flow control usually regulates resource utilization and thus has a significant impact on performance [4]. Constrained strictly by area, flit-level flow control is used to minimize the amount of buffering per router and hence its area footprint.

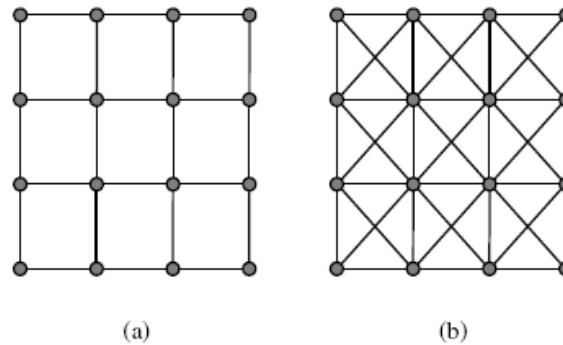


Figure 1. A 4 × 4 Network: (a) Mesh, (b) DMesh

In the rest of the paper, we present related work in Section 2. Section 3 illustrates the idea behind the proposed routing scheme for DMesh networks, and also gives the livelock-freedom and deadlock-freedom proof. Section 4 gives the performance comparisons by comparing with DXY algorithm. Finally, Section 5 concludes the paper.

2. Related Work

Pin bandwidth of routers is extended to T b/s from the order of G b/s in the early 90s, and will be expected to P b/s in the future. High radix router, as a hot topic in research in NoC, is more effective in converting pin bandwidth to reduced latency and enhanced throughput. Through 2D Mesh was widely used in both commercial and experimental machines in the past, they are not applicable to design of NoC today for their higher diameter and average hop counts compared to network with high-radix routers. Based on high-radix router, many different topologies has been proposed, such as clos [5], flattened butterfly [6-7], DMesh [8], Dragonfly [9].

Among the proposed various topologies based on high-radix router, DMesh is migrated from 2D Mesh without long links incorporated, and it holds many superior properties in Mesh, Figure 1 (a) and (b) shows the 4 × 4 Mesh and DMesh networks. In [8], Ouyang proposed a deadlock-free minimal algorithm (called DXY) for DMesh. In DXY, the crossing channel is always selected if the both offsets along dimension X and Y are non-zero. However, DXY routing algorithm did not exploit the balancing use of links in DMesh.

As known, routing algorithm [10-13], as well as buffer management [12], contributes to the performance of the whole network. In this paper, based on DMesh network, we analyze the unbalancing use of physical links in DXY algorithm, and present a novel routing algorithm to exploit routing adaptivity in order to improve performance of the overall chip.

3. Revised DXY Routing in DMesh Network

In DMesh network, we call the physical links along dimensions X and Y regular links, and links along line $y = x$ and line $y = -x$ crossing links. In DMesh, each router has 9 different ports, with 1 connected to local processor and 8 others connected to neighbor routers. For ease of description, we define the directions of the 8 output ports as shown in Figure 2.

3.1. Description of the Proposed Algorithm

The DXY routing algorithm always routes packets along C or T port if neither of the offsets along X and Y is zero, which lays heavy load on C and T links. Based on the

above observation, we propose a novel revised DXY routing algorithm with no extra virtual channel.

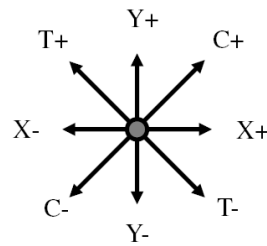


Figure 2. Eight Different Directions of Ports in One Router

Algorithm 1 shows the pseudo code of the revised DXY (RDXY) routing algorithm in DMesh networks. Taking the coordinates of the current and destination routers as inputs, it returns a selected channel as the output. First, compute the offsets along dimension X and Y, and label them with $offx$ and $offy$. If both $offx$ and $offy$ are greater than 0, the packet can route along direction X+ and C+. Here, the packet has some adaptivity compared to DXY algorithm. Similar options take place when the two offsets are none zero in other three situations. If only one offset is none zero, packet is routed along that dimension; while if both of the two offsets are zero, packet is now in the destination router, and will be transmitted to its local processor via L output port. The select function in the table means to return one free output channel from the candidate channel set (cset), and if more than one channel is free, the C and T channels usually hold a higher priority. While if none of the candidate channels is free, the packet will wait until one channel is released.

Algorithm 1: The revised DXY routing algorithm.

Input: Coordinates of current router (x_c, y_c) and destination router (x_d, y_d);

Output: A selected output channel.

1. $offx = x_d - x_c, offy = y_d - y_c, cset = \emptyset$;
 2. if $offx > 0$ and $offy > 0$ $cset = \{X+, C+\}$;
 3. if $offx > 0$ and $offy == 0$ $cset = \{X+\}$;
 4. if $offx > 0$ and $offy < 0$ $cset = \{X+, T-\}$;
 5. if $offx < 0$ and $offy > 0$ $cset = \{X-, C+\}$;
 6. if $offx < 0$ and $offy == 0$ $cset = \{X-\}$;
 7. if $offx < 0$ and $offy < 0$ $cset = \{X-, C-\}$;
 8. if $offx == 0$ and $offy > 0$ $cset = \{Y+\}$;
 9. if $offx == 0$ and $offy == 0$ $cset = \{L\}$;
 10. if $offx == 0$ and $offy < 0$ $cset = \{Y-\}$;
 11. return $select(cset)$.
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In the new RDXY algorithm, the select function gives high priority to the crossing output channels when there is more than one optional free channel. This scheme is different from that in DXY which always prioritize the crossing channel no matter it is free or busy. On the one hand, the select function could make efficient use of crossing channels to cut down the travelling hop counts under low load rate. On the other hand, when load rate is high, the resource competition is fierce, so the adaptivity provided by RDXY could efficiently balance channel utilization among regular links and crossing links. This balancing could directly be transferred to reduced average delay and enhanced throughput in the whole network.

The proposed RDXY provides some adaptivity for packets. For example, in an 8×8

DMesh, a packet originating from (0, 0) and designating to (3, 1) has 4 optional routing paths in RDXY, while only 1 in DXY. The RDXY algorithm allows packets to traverse the network along non-minimal paths. However, the total length of routing path is no more than that of the minimal routing in Mesh networks. Since non-minimal routing is introduced in RDXY, the livelock-freedom should be presented, and details about that are described in the next subsection.

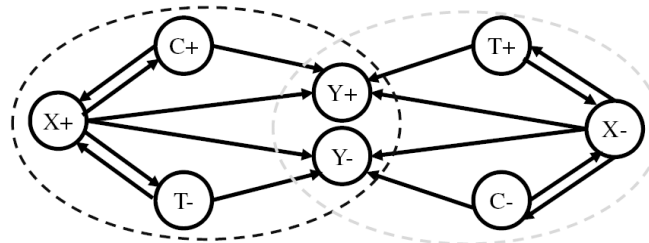


Figure 3. Possible Channel Dependencies in RDXY.

3.2. Deadlock and Livelock Freedom

Deadlock and livelock freedom are two fundamental requirements in design of routing schemes. Here in this subsection, we will prove that the proposed RDXY can fulfill them. In NoC, livelock occurs when a packet travels indefinitely in the network without ever reaching its destination. In some certain situation, this can happen if a packet is misrouted on an unproductive channel. Though misrouting is allowed in the proposed RDXY, packet (source: (x_s, y_s) and destination: (x_d, y_d)) will traverse no more than $(|x_d - x_s| + |y_d - y_s|)$ hops in the DMesh network, that is, packet will never wanders permanently in the network. Since packet will always reach its destination router in some definite time based on RDXY, to sum up, RDXY is free from livelock.

Lemma 1 *The RDXY algorithm is deadlock free.*

Proof

According to Algorithm 1, 16 different channel dependencies may occur in the network, as shown in Figure 3. Since XY routing in Mesh is deadlock free, cyclic channel dependency within X and Y channels will never occur, in the similar manner, RDXY will not introduce cyclic channel dependency with only X and Y channels. From Figure 3, no channel dependency forms from Y to others, therefore, we can divide the channel dependency graph into two parts with two ellipses, and now prove that no cyclic channel dependency occurs with only channels in black (gray) ellipse.

Suppose that there exists a cycle, packets involved in it can only hold and apply for channels in the black ellipse. On the one hand, Y channel will not appear in the cycle, or the cycle is broken since the packet hold Y channel will not apply for other type of channels. On the other hand, the X+, C+, T- channel all lead packets towards the positive position along dimension X, till now, the cycle is broken since no channel in the group could lead packets in the reverse direction. Therefore, it is clear that no deadlock occur with only channels in the black ellipse. In the similar manner, we could prove that no deadlock occur with only channels in the gray ellipse in Figure 3. Therefore, the proposed RDXY algorithm is deadlock free.

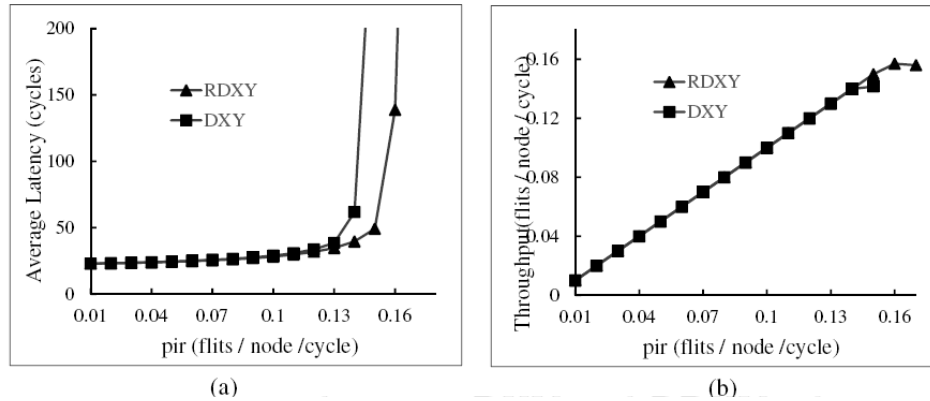


Figure 4. Performance Comparisons between DXY and RDXY Schemes with Bit Complement Traffic: (A) Latency-Pir Curve, (B) Throughput-Pir Curve

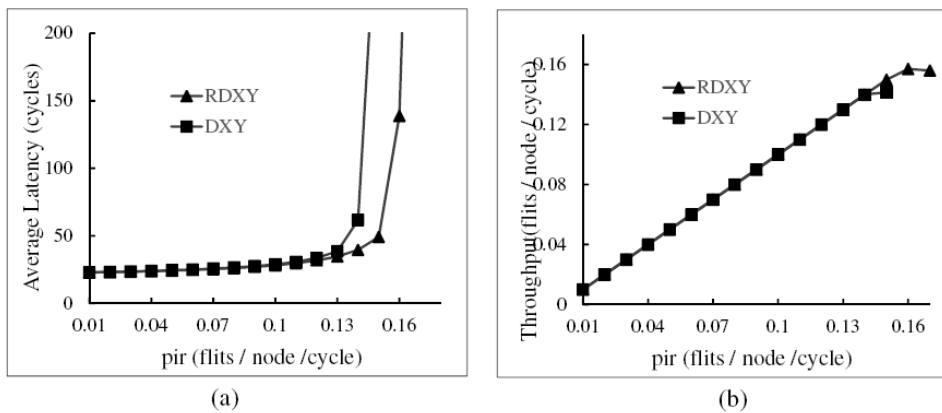


Figure 5. Performance Comparisons between DXY and RDXY Schemes with Transpose Traffic: (A) Latency-Pir Curve, (B) Throughput-Pir Curve

4. Evaluation and Discussion

4.1. Experimental Setup

Measurements are implemented in a cycle-accurate C++ network simulator. Simulations are performed on an 8×8 2D DMesh, and all network channels are 64 bits wide with a delay of one cycle. Each router is modeled input-queued with four pipeline stages including buffer write, routing computation, switch allocation, and switch traversal. Each input buffer has a total capacity of 4 flits. Each packet contains five flits with one head flit, three data flits, and one tail flit. In our simulation, 10; 000 cycles are used to warm up the network, and another 100; 000 cycles are used to capture the parameter of network performance.

4.2. Traffic Pattern and Evaluation Metrics

To verify the effectiveness of the proposed RDXY, we evaluate its performance by comparing with DXY under a range of synthetic traffic patterns of permutation (transpose, bit-complement) traffic. In [8], performance comparisons are done under bit complement traffic, and that is one of the reasons why we select it in our simulation. Details about the three permutation traffic patterns can be found in chapter three in [11]. As for performance metrics, we choose average latency (cycles) and throughput

(flits/node/cycle) with the varying of packet injection rate. We indicate with packet injection rate (pir) the rate at which packets are injected into the network.

4.3. Results Discussion

Figure 4 shows the latency-pir curves for the bit-complement traffic pattern for both DXY and RDXY algorithms in 8×8 DMesh. Under this traffic, the RDXY shows better performance than DXY. The saturation point of them are 0.145 (flits/node/cycle) and 0.16 (flits/node/cycle), respectively. The performance improvement of RDXY over DXY is about 10.3%. As for the aspect of throughput, the peak throughput of RDXY and DXY are 0.157 (flits/node/cycle) and 0.145 (flits/node/cycle), thus, RDXY gains 0.012 (flits/node/cycle) improvement. Here, the proposed RDXY offers better performance because it makes more balance traffic than DXY between the regular channels (X and Y) and the crossing channels (C and T).

Figure 5 shows the results obtained when the network has transpose traffic. This type of traffic is used in several simulation scenarios. As can be seen, the non-adaptivity of the DXY algorithm results in a lower saturation point, at about 0.13 (flits/node/cycle). However, the proposed routing scheme saturates at about 0.18 (flits/node/cycle), which performs much better (about 38.5% improvement) than DXY from the saturation viewpoint. For a pir value of 0.12 (flits/node/cycle), the average packet latency of DXY and RDXY are 20.55 and 26.58 (cycles), respectively. As for peak throughput, the RDXY provides 0.170 (flits/node/cycle) while DXY provides 0.127 (flits/node/cycle), thus, the RDXY still yields the lower average packet delay under non-saturated network conditions, and higher sustained throughput than DXY scheme.

5. Conclusions

To exploit advances in technology, high radix routers are adopted in order to convert pin bandwidth to reduced latency in the interconnection network. In DMesh network, the port number of routers is twice as many as that in mesh. In this paper, we have presented a new RDXY routing algorithm to make up for the non-adaptivity deficiency in DXY. The balanced use among different physical links in RDXY contributes to performance enhancement. Due to the special characteristics of DMesh network, the new routing mechanism is simple and easy to implement in routing computation component compared to DXY scheme. Also, we give a theoretical justification for RDXY in the aspect of deadlock-freedom and livelock-freedom. Simulation results show that the proposed RDXY can effectively enhance channel utilization, and bring $> 10\%$ improvement when compared to the original RXY routing algorithm.

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References

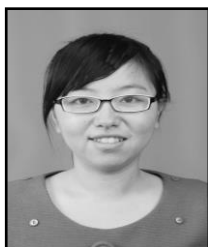
- [1] Y. Xu, B. Zhao, Y. Zhang and J. Yang, "Simple virtual channel allocation for high throughput and high frequency on-chip routers", In Proc. of IEEE International Symposium on High Performance Computer Architecture, (2010), January.
- [2] R. Marculescu, J. Hu and U. Ogras, "Key research problems in NoC design: a holistic perspective", In Proc. of IEEE/ACM International Conference on Hard-ware/Software Codesign and System Synthesis, (2005), September.
- [3] J. Balfour and W. Dally, "Design tradeoffs for tiled CMP networks", In Proc. of ACM International Conference on Supercomputing, (2006), June.

- [4] J. Wang, Y. Li and H. Li, "A performance analytical strategy for network-on-chip router with input buffer architecture", In J. of Advances in Electrical and Computer Engineering. vol. 12, no. 4, (2012).
- [5] J. Kim, W. Dally and D. Abts, "Adaptive routing in high-radix Clos network", In Proc. of International Conference for High Performance Computing, Networking, Storage, and Analysis, (2006), November.
- [6] J. Kim, W. Dally and D. Abts, "Flattened butterfly: a cost-efficient topology for high-radix networks", In Proc. of IEEE International Symposium on Computer Architecture, (2007). January.
- [7] M. Csernai, F. Ciucu and R. Braun, "Reducing cabling complexity in large flattened butterfly networks by an order of magnitude", In Proc. of Optical Fiber Communication Conference, (2014).
- [8] Y. Ouyang, B. Zhu, H. Liang and W. Feng, "Networks on chip based on diagonal interlinked mesh topology structure", In J. of Computer Engineering, vol. 35, no. 22, (2009).
- [9] J. Kim, W. Dally and S. Scott, "Technology-driven, highly-scalable dragonfly topology", In ACM SIGARCH Computer Architecture News, vol. 36, no. 3, (2008).
- [10] X. Wang, D. Xiang and Z. Yu, "TM: A new and simple topology for interconnection networks", In J. of Supercomputing, vol. 66, no. 1, (2013).
- [11] W. J. Dally and B. Towles, "Principles and practices of interconnection networks", Morgan Kaufmann, San Francisco, CA, (2004).
- [12] D. Becker, N. Jiang, G. Michelogiannakis and W. Dally, "Adaptive backpressure: efficient buffer management for on-chip networks", in Proc. of IEEE International Conference on Computer Design, (2012), September.
- [13] X. Y. Wang and N. Li, "DTDOR: an efficient routing algorithm for torus networks", In J. of Future Generation Communication and Networking, vol. 7, no. 4, (2014).

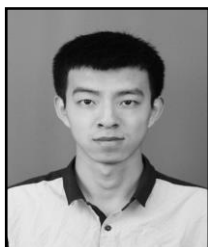
Authors



Xinyu Wang, Female, born in 1985, she received her doctoral degree from the Department of Computer Science and Technology in Tsinghua in July, 2013, and her research areas include parallel and distributed computing, and routing design in network on chip. Email address: Distribute_2008@163.com.



Tingting Han, Female, born in 1993, she is pursuing her bachelor degree in Dongbei University of Finance and Economics, and her research areas include parallel and distributed computing, and routing design in network on chip. Email address: tingtinghan_2015@163.com.



Haikuo Liu, Male, born in 1993, he is currently pursuing his bachelor degree in Dongbei University of Finance and Economics, and his research areas include parallel and distributed computing, and routing design in network on chip. Email address: haikism@hotmail.com.

