International Journal of Future Generation Communication and Networking
Vol. 8, No. 5 (2015), pp. 145-156
http://dx.doi.org/10.14257/ijfgcn.2015.8.5.15

Research on the Optimization of the Performance of CTL Loop Discriminator

Xu Ying[1], Yuan Hong[1], Luo Ruidan[1,2] and Xu Duo[3]

[1]Academy of Opto-Electronics, Chinese Academy of Science, Beijing, 100094, China
[2]University of Chinese Academy of Sciences, Beijing 100049, China
[3]Beijing Institute of Technology, Beijing, 100081, China
nadinexy@aoe.ac.cn

Abstract

Chip Tracking Loop (CTL) is the key to ensure the accuracy of regenerative pseudo-noise ranging in the deep space measurement and control communication system. However, due to the impact of the code imbalance, clock attenuation rate and noise, the loop locking time of CTL is prolonged and the ranging accuracy is degraded. In this paper, we proposed the discriminator optimization algorithm to address this problem. This algorithm is based on the loop discrimination performance of clock code and composite code, and the impact of the noise on the discrimination performance. In order to improve the tracking accuracy and shorten the loop locking time, this algorithm corrected the curve of discriminator's gain by compensating discriminator's gain. Both the theory analysis and simulation results illustrate that the algorithm can correct the discriminator's gain curve, reduce the loop locking time and ensure the significant tracking accuracy in low SNR.

Keywords: *Regenerative PN Ranging, CTL, Tracking Performance, Discriminator Gain, S Curve*

1. Introduction

Currently, owing to high independent ranging accuracy and can be combined with the carrier ranging, regenerative pseudo-noise ranging has become a generic solution of deep space exploration sophisticated inter-satellite ranging [1-2]. The Consultative Committee for Space Data Systems (CCSDS) is developing the pseudo-noise ranging standard, which focuses on the regenerative pseudo-noise ranging [3-4].

With respect to the regenerative pseudo-noise ranging approach, Chip Tracking Loop (CTL) is the key to ensure the accuracy of ranging accuracy. The greater loop detection gain, the stronger capacity to capture and track loop.

Literature [5] first proposed the concept of CTL and made a detailed analysis on the theoretical tracking performance of loop, drawn that the capture and tracking performance of CTL was independent of SNR (Signal to Noise Ratio). However, a number of subsequent researches have focused on the pseudo-noise ranging signal, and made a comparative analysis on the loop tracking performance of different regenerative ranging codes [6], pseudo-code signal waveform [7-9], data channel modulation mode [10], *etc.*, as well as analyzed comprehensively the relations between loop bandwidth, PN code chip rate, ranging SNR, data processing rate and regenerative code clock jitter of CTL [11].

In this paper, it focuses on the research of loop gain of CTL, and proposes to perform optimization and compensation on the discriminator gain through the analytical derivation of loop discriminator's characteristics and discrimination curve gain, and based on the difference in discrimination performance between clock code and composite code, and the

ISSN: 2233-7857 IJFGCN

impact of noise on the discrimination performance, as well as finally verifies the feasibility of this approach via simulations.

2. Discriminator Characteristics of CTL

The structure of CTL is shown in Figure 1, wherein the phase integrator, multiplier and integrate-dump together constitute the discriminator of CTL.

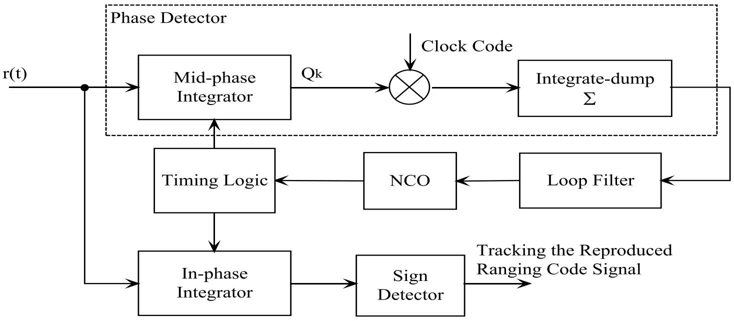

Figure 1. The Schematic Diagram of CTL's Structure

Assuming that the input signal of CTL $r(t)$ contains only the composite code information and noise:

$$r(t) = Q'_{ps}(t) = \sqrt{\frac{P}{2}} \cdot \theta_r \cdot R(t) + n(t) = s(t,\varepsilon) + n(t) = A\sum_{m=-\infty}^{\infty} c_m h_{sq}(t - mT_c - \varepsilon) + n(t) \tag{1}$$

Where, $s(t,\varepsilon)$ is the composite code signal, A denotes the signal amplitude, T_c denotes the chip period, cm denotes the polarity of the m-th chip, $h_{sq}(t)$ is the unit amplitude rectangular pulse in the range of $0 \le t \le T_c$, and ε denotes the composite code signal phase to be estimated, which is assumed to be uniformly distributed in the range of $-T_c/2 \le \varepsilon \le T_c/2$, $n(t)$ is an additive white Gaussian noise, the unilateral power spectral density of which is N_0. Then, the output of the phase integrate-dump in $\hat{\varepsilon}$ is expressed as:

$$Q_k = \int_{(K-\frac{\xi}{2})T_c+\varepsilon}^{(K+\frac{\xi}{2})T_c+\varepsilon} s(t,\varepsilon)dt + \int_{(K-\frac{\xi}{2})T_c+\varepsilon}^{(K+\frac{\xi}{2})T_c+\varepsilon} n(t)dt \, \square \, b_k + N_k \tag{2}$$

Where, b_k denotes the portion of the composite code signal, $\hat{\varepsilon}$ denotes clock phase of the estimated composite code, ξ denotes the window width of phase integral, N_k denotes the output noise of the phase integrate-dump, which is a random number with the mean value of zero variance of $\sigma^2_{Nk} = \xi N_0 T_c / 2$, and for $k \ne l$, N_k and N_l are mutually independent.

Taking a time-domain rectangular wave for example, assume that the window width of the Mid-phase Integrator is ξ=1, due to the symmetry of the signal waveform and it is considered that the polarity of the adjacent chips is opposite, thus it may simplify the interval of the phase integral filter, as shown in Figure 2. The theoretical start and end points of the mid-phase integral filter for those two chips are $\left(K - \frac{1}{2}\right)T_c + \varepsilon$ and $\left(K + \frac{1}{2}\right)T_c + \varepsilon$ respectively, while the actually outputted start and end points of the mid-phase integral filter by NCO are $\left(K - \frac{1}{2}\right)T_c + \hat{\varepsilon}$ and

$\left(K+\frac{1}{2}\right)T_c+\hat{\varepsilon}$ respectively. Due to the symmetry of the signal waveform and it is considered that the polarity of the adjacent chips is opposite, thus the integration result of the interval from $\left(K-\frac{1}{2}\right)T_c+\hat{\varepsilon}$ to $\left(K+\frac{1}{2}\right)T_c+\hat{\varepsilon}$ is zero, and the actually equivalent range of the integrate-dump is $\left(K+\frac{1}{2}\right)T_c+2\varepsilon-\hat{\varepsilon}$ □ $\left(K+\frac{1}{2}\right)T_c+\hat{\varepsilon}$.

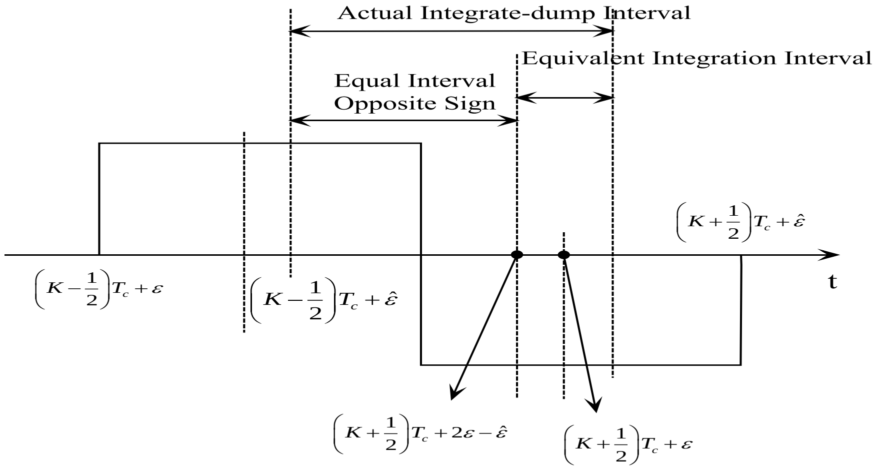

Figure 2. The Schematic Diagram of the Interval of the Mid-Phase Integrate-Dump

Then, the signal portion of the phase integrate-dump is:

$$\begin{aligned} b_k &= A\int_{(K-\frac{1}{2})T_c+\varepsilon}^{(K+\frac{1}{2})T_c+\varepsilon} c_k dt = A\int_{(K-\frac{1}{2})T_c+\varepsilon}^{KT_c+\varepsilon} c_k dt + \sqrt{2}A\int_{KT_c+\varepsilon}^{(K+\frac{1}{2})T_c+\varepsilon} c_{k+1} dt \\ &= a_k(\frac{AT_c}{2}+(\varepsilon-\varepsilon))+a_{k+1}(\frac{AT_c}{2}-(\varepsilon-\varepsilon)) = 2AT_c\cdot\frac{\varepsilon-\varepsilon}{T_c} = 2AT_c\lambda \end{aligned} \tag{3}$$

Where, $\lambda=(\varepsilon-\varepsilon)/T_c, -1/2\le\lambda\le 1/2$ represents the normalized estimation error of code clock, due to the discrimination curve (S curve) of CTL is an odd function, all simplified analysis are carried out in the range of $0\le\lambda\le 1/2$.

The overall error of CTL is the output result of the integrate-dump, that is

$$e(t)=e_i=\sum_{k=iK}^{(i+1)K-1}(Q_k\times D)=\sum_{k=iK}^{(i+1)K-1}[(b_k+N_k)\times D] \tag{4}$$

Where, K denotes the cumulative number of chips for the integrate-dump before the loop filter, $D=\pm 1$

The expected value of code clock estimation error is the S curve of the discriminator, expressed as:

$$g(\lambda)=E_{n,s}\{e(t)\}=E_{n,s}\left\{\sum_{k=iK}^{(i+1)K-1}[(b_k+N_k)\times D]\right\}=E_s\left\{\sum_{k=iK}^{(i+1)K-1}(b_k\times D)\right\} \tag{5}$$

Where, $E_{n,s}\{\cdot\}$ means to acquire the expectations of signal and noise, and $E_s\{\cdot\}$ means to acquire the expectations of signal. Substituting equation (4.3) into equation (4.5), average the received composite code signal, that is, the relational expression of S curve. Taking the +1/-1 alternating square wave signal for example, it is deemed that the code loop is in the tracking state (*i.e.*, $\lambda \rightarrow 0$), then it can be obtained

$$g(\lambda) = 2\lambda A T_K \qquad 0 \le \lambda \le 1/2 \tag{6}$$

Where, TK=KTc denotes the integrate-dump time of CTL.

$$K_s = \left.\frac{dg(\lambda)}{d\lambda}\right|_{\lambda=0} = 2AT_K \tag{7}$$

The S-curve of CTL is shown in Figure 3. It is visible that S-curve of CTL is a straight line with the gain of 1.

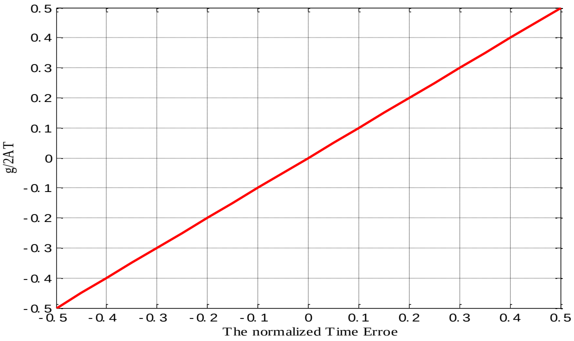

Figure 3. The Normalized S-Curve of CTL

3. Performance Optimization of CTL Discriminator

3.1. Discrimination Performance of Clock Code and Composite Code

In the theoretical derivation process, the composite code signal inputted into the loop is considered as a +1/-1 alternating code sequence (*i.e.*, clock code), but in fact, the composite code signal inputted is not completely +1/-1 alternately. The +1/-1 alternating characteristics of the composite code reflects the balance property and clock attenuation rate characteristics of the code, while the imbalance and clock attenuation rate characteristics of the code will affect the accuracy of ranging accuracy, therefore, in order to get a higher ranging accuracy in the deep space exploration communications system, it needs to conduct research and analysis on the loop discrimination performance of the clock code and composite code.

CTL will dynamically adjust NCO according to the output code clock error results of the discriminator, so as to achieve the synchronization between the estimated code clock and the actual code clock. In order to measure the discrimination phase difference on those two codes of the CTL discriminator, it has carried out CTL open-circuit simulation, namely, not updating the frequency words of NCO, but fixing its code rate identical with the input signal. The setting of simulation parameters is shown Table 1.

Table 1. Setting of Simulation Parameters for the Performance of CTL Loop Discriminator

Loop Simulation Times	Carrier to Noise Ratio (CNR)	Starting Code Chip	Number of Loop Integrate-Dump Chips K
100	No Noise	1	10000

The discrimination results of CTL discriminator on clock code and composite code are listed in Table 2, and it draws the discrimination curve of clock code and composite code according to the simulation results in Table 2, *i.e.*, S-curve, as shown in Figure 4. As mentioned above, earlier studies on the loop S-curve indicate that, the gain of CTL discriminator is 1, owing to assume that the inputted composite code signal is +1/-1 alternately in the theoretical derivation process. However, in accordance with the actual simulation analysis results, with respect to the code clock, the gain of CTL discriminator is 1, which is consistent with the theoretical analysis results; Nevertheless, in respect of the composite code, the gain of CTL discriminator is not 1, but approximate to 0.627106. This gain may be considered an existence of a fixed bias with the actual gain, which does not change with the changes in the signal to noise ratio, thus it may compensate the CTL discriminator's gain.

Table 2. Discrimination Results of Clock Code and Composite Code

Initial Code Phase Difference/chip	Clock Code Discrimination Results/chip	Composite Code Discrimination Results/chip
-1/2	-0.499793	-0.313552
-3/8	-0.374795	-0.235393
-1/4	-0.249794	-0.156974
-1/8	-0.124795	-0.078551
0	0.002051	-0.000133
1/8	0.125194	0.078290
1/4	0.250194	0.156709
3/8	0.375194	0.235127
1/2	0.499793	0.313553

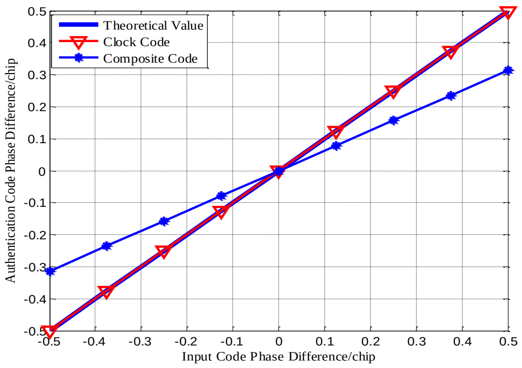

Figure 4. The Discrimination Curve of Clock Code and Composite Code

3.2. Impact of Noise on the Discrimination Performance

In the simulation process, it is revealed that noise has a great influence on the CTL discriminator, although the analysis on the loop discriminator in Section 2 has taken the noise into consideration, the influence of noise was offset during the process of acquiring expectations to signal and noise simultaneously. In practice, in case of extracting composite code signal from the carrier loop, due to the presence of noise, the composite code signal superimposed with noise may change the size of the original composite code signal, which may not be significantly affected if only the change in amplitude as the sign operation of the signal may ignore the impact. However, if the polarity is changed, the results of Mid-Phase Integrate-Dump will be subject to a significant change, as shown in Figure 5. Ideally, the Mid-Phase Integrate-Dump should contain accurate code clock estimation error. When the noise is severe, the estimation error contained in the Mid-Phase Integrate-Dump may become smaller, and the adjustment amount introduced into NCO after filtering will also become smaller, while CTL oscillation time will become longer, thereby affecting the tracking time and tracking accuracy of CTL.

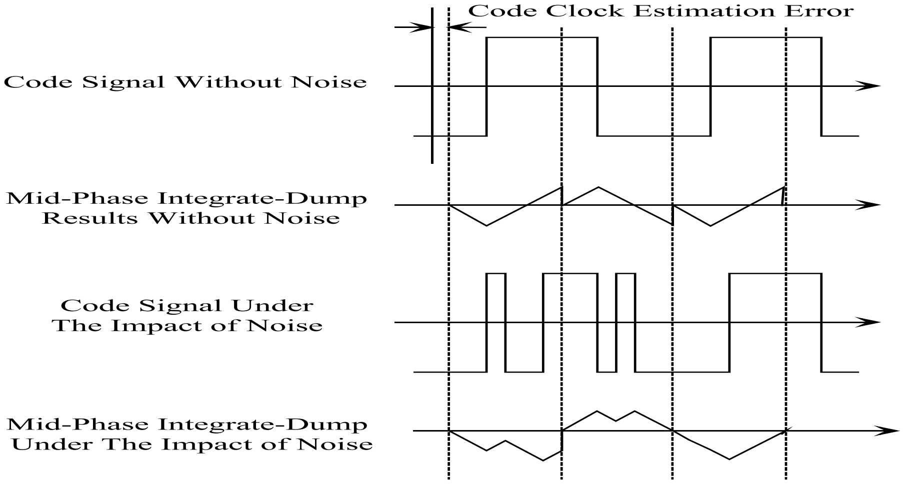

Figure 5. The Impact of Noise on Composite Code Signal

Table 3. The Impact of CNR on the Authentication Code Phase Difference

CNR/dB-Hz	Authentication Code Phase Difference/chip	Gain Adjustment Compensated To The Theoretical Value
No Noise	0.1567096	1
65	0.1567096	1
60	0.1562227	0.9968
58	0.1537017	0.9808
57	0.1509983	0.9635
56	0.1468327	0.9369
55	0.1414707	0.9027
54	0.1352330	0.8629
53	0.1274961	0.8135
52	0.1191995	0.7606
50	0.1016302	0.6485
45	0.0629896	0.4019
40	0.0366733	0.2340
38	0.0290874	0.1856
35	0.0207499	0.1324
32	0.0147882	0.0943
30	0.0116308	0.0742

Table 3 illustrates the output results of the discriminator under different CNRs when the input code phase difference is 1/4 chip. In accordance with the recommendations by CCSDS, CTL is able to operate at the lowest frequency environment of 30dBHz, thus the minimum CNR for simulation can be down to 30dBHz. In line with the simulation results illustrated in Table 3, it can be obtained that, when CNR decreases below 56dB-Hz, there will be beginning to present more differences between the code phase difference outputted by the discriminator and the ode phase difference discriminated under no noise conditions. As the increment of noise, the adjustment of NCO on the loop is gradually reduced, so that the loop oscillation time becomes longer. Therefore, it can correct the discrimination results to make the code phase difference discriminated to get closer to the actual code phase difference, so that the loop oscillation time becomes shorter.

3.3. Optimization and Simulation Analysis of Discriminator

When the input signal is a composite code, namely, which is not an entirely +1/-1 alternating code sequence, the gain of CTL discriminator is not 1, and it needs to be corrected. For T2B code, the gain can be corrected to 0.627.

When the noise is severe, the code phase difference outputted by the discriminator will be far less than the actual code phase difference, so that the regulation effects of NCO will be weaken, while the loop oscillation is great and long-term, affecting the tracking time, thus it may correct the discriminator appropriately in order to reduce the oscillation time. The compensation on the discrimination results can neither be too large nor too small, when the compensation is too small (compensated by high CNR), the improvement on the loop oscillation time is not significant; when the compensation is too large (compensated by low CNR), it is equivalent to increase the adjustment step of NCO, which may result in the loop always unable to lock. In this paper, it averages the gain adjustment under different CNRs, multiplying the mean value (0.646) and the gain adjustment of the composite code obtains a relatively reasonable gain adjustment -0.405.

In this paper, the optimization focuses on the low CNR scenarios. When the noise is severe, the adjustment introduced into NCO is small, making the loop locking time slow down, and the introduction of gain adjustment can solve the problem of slow adjustment of NCO in the beginning of tracking by CTL. However, when CTL achieves a relatively stable tracking, continuous introduction of gain compensation may affect the tracking accuracy of CTL, thus the compensation on the gain of the loop discriminator only acts on a period of time in the beginning of the simulation in order not to affect the tracking accuracy while reducing the loop locking time; after a period of time, the loop has been basically achieved a stable tracking, and it will not compensate the gain. The specific settings of simulation parameters are shown in Table 4.

Table 4. Settings of Optimization Simulation Parameters of the Loop Discriminator

Setting Variable	Settings
Sampling Clock	56MHz
Type of Composite Code	T2B
Rate of Composite Code	2.06859MHz
Waveform of Composite Code	Rectangular
Length of Loop Integrate-Dump	10000chip
Loop Bandwidth	10Hz
Compensation and Correction Time of Gain	1.5s

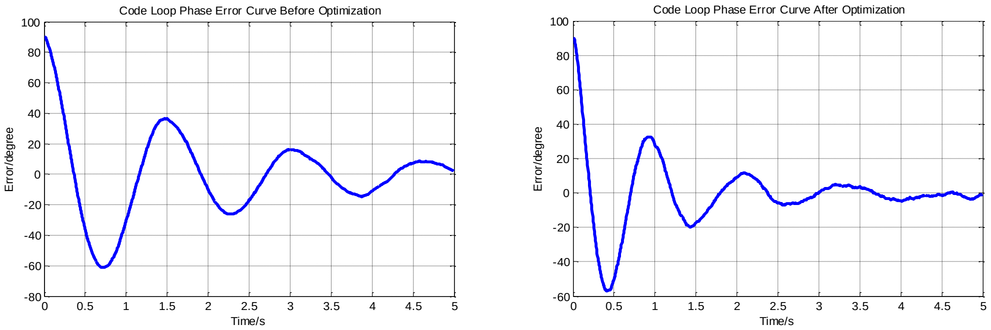

Figure 6. The Simulation Results for the Tracking Error of CTL before and after Optimization when CNR Is 30dbhz

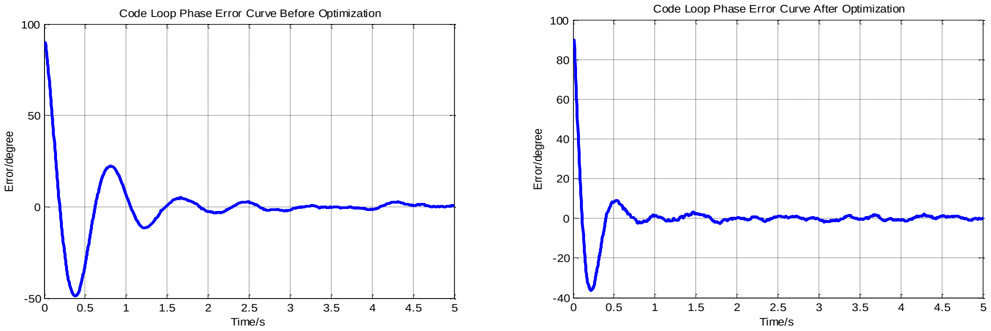

Figure 7. The Simulation Results for the Tracking Error of CTL before and after Optimization when CNR Is 40dbhz

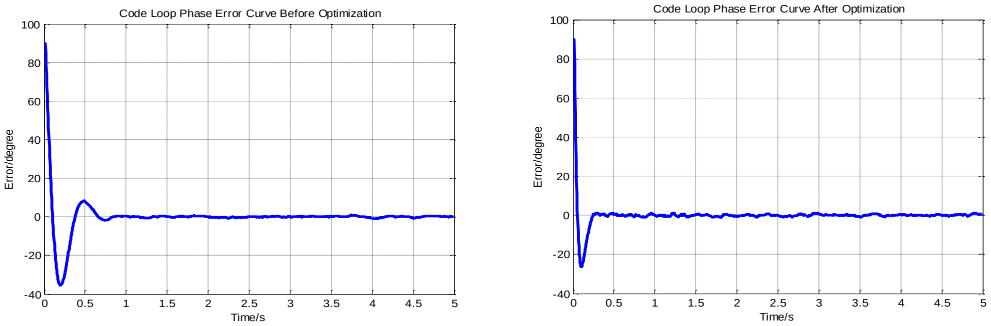

Figure 8. The Simulation Results for the Tracking Error of CTL before and after Optimization when CNR Is 50dbhz

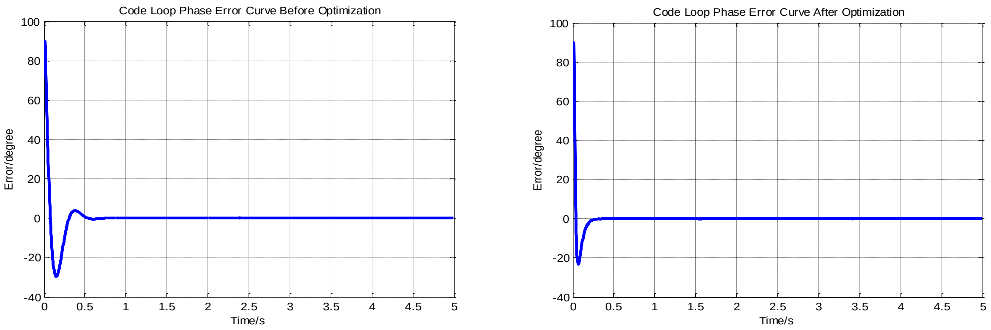

Figure 9. The Simulation Results for the Tracking Error of CTL before and after Optimization when CNR Is 60dbhz

Figure 6 - Figure 9 illustrate the simulation results for the tracking error of CTL before and after optimization under different CNRs. It is indicated that, the tracking error oscillation of CTL after optimization has been significantly reduced, and the improved performance is more obvious with the reduction in CNR. When CNR is greater than 60dBHz, the tracking error curve of CTL is substantially similar to that under 60dBHz. In this kind of simulation conditions, under the minimum CNR of 30dBHz, the optimized loop can be substantially locked with 2s, while the loop before optimization needs to achieve the efficiency after optimization with 4s.

Table 5. The Tracking Accuracy of CTL under Different CTLs

CNR/dBHz	The tracking accuracy before optimization/°	The tracking accuracy under fixed gain adjustment/°	The tracking accuracy under switching gain adjustment/°
No Noise	0.045555	0.055810	0.048328
60	0.052587	0.064160	0.052696
50	0.396801	0.589139	0.373153
40	1.316295	1.370087	0.869488
30	6.490832	4.368554	2.351053

Table 5 illustrates the tracking accuracy of the discriminator before and after optimization under different CNRs, and the tracking accuracy herein is the rms of the difference values between the reproducible code phase by CTL and the actual code phase, in degrees. As can be seen from Table 5, in the same time, the impact of discriminator optimization on the tracking accuracy under high CNR is relatively small. In the wake of the reduction in CNR, optimizing the discriminator will result in a certain improvement on the tracking accuracy. Although the improvement is not significant, it will not degrade the tracking accuracy.

4. Conclusions

In this paper, a theoretical derivation on the discriminator characteristics of CTL has been carried out, and the analysis results show that the S-curve of discriminator is a straight line with a gain of 1. Then, based on the differences between the clock code and the composite code, as well as the impact of noise on the discriminator, an optimizing approach for discriminator has been proposed - making compensa-tion for the gain of discriminator. The optimized discriminator can effectively shorten the loop locking time in the premise of ensuring that the tracking accuracy does not deteriorate, and the simulation results demonstrate the feasibility of this approach.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant Nos. 61102130) and the Innovative Program of the Academy of Opto-Electtronics, Chinese Academy of Science (Grant Nos. Y12414A01Y).

References

[1] J. L. Massey, G. Boscagli and E. Vassallo. “Regenerative Pseudo-Noise (PN) Ranging Sequences For Deep-Space Missions”, International Journal of Satellite Communications and Networking, vol. 25, no. 3, **(2007)**, pp. 285-304.

[2] E. Atricciani, “Best Design of Deep-Space Communication with A 2-Hop Downlink at 32 GHz”, IET Conference Publications, vol. 552, **(2009)**, pp. 554-558.

[3] G. Boscagli, P. Holsters and E. Vassallo, “PN Regenerative Ranging and Its Compatibility with Telecommand and Telemetry Signals”, Proceedings of the IEEE, vol. 95, no. 11, **(2007)**, pp. 2224-2234.

[4] S. S. Intille, J. Lester and J. F. Sallis, "New Horizons in Sensor Development", Medicine & Science in Sports & Exercise, vol. 44, no. 1S, **(2012)**.
[5] Z. Chaojie, J. Xiaojun and Y. Faxin, "Performance Analysis Of A Novel Chip Tracking Loop Used For Regenerative Pseudo-Noise Ranging Clock Recovery", Journal of Southeast University, vol. 32, no. 2, **(2007)**, pp. 185-189.
[6] J. Xiaojun, Y. Faxin and Z. Yangming, "Study on the Tracking Accuracy of Regenerative Ranging Codes Used in Micro-Satellite Transponder", Chinese Journal of Sensors and Actuators, vol. 20, no. 8, **(2007)**, pp. 1921-1925.
[7] J. Xiaojun, Y. Faxin and J. Zhonghe, "Design of Signal Waveform in Pseudo-Code Ranging", Journal of Astronautics, vol. 28, no. 1, **(2007)**, pp. 64-68.
[8] Y. Faxin, J. Xiaojun and S. Yuan, "Performance Analysis of CTL Used For MSK Waveform PN Code", Journal of Jilin University, vol. 32, no. 2, **(2007)**, pp. 464-468.
[9] Y. Faxin, Z. Chaojie and J. Jianwen, "Performance Analysis of Chip Tracking Loop Using TDRC Waveform Pseudo-Code", Journal of Zhejiang University, vol. 41, no. 8, **(2007)**, pp. 1316-1319.
[10] J. Xiaojun, Z. Chaojie and Y. Faxin, "Impact of Data Channel on Tracking Performance of Pseudo-Code Tracking Loop", Journal of Zhejiang University, vol. 42, no. 3, **(2008)**, pp. 465-470.
[11] Z. Chaojie, J. Xiaojun and J. Jianwen, "Effect of Processing Rate On Regenerative Clock Jitter Performance In Pseudo-Random Code Ranging", Journal of Astronautics, vol. 31, no. 7, **(2010)**, pp. 1805-1809.

Authors

Xu Ying, born in 1983, received the Ph. D degrees in signal processing from Beijing Institute of Technology, Beijing, China, in 2009. She is currently a vice researcher in Academy of Opto-Electronics, Chinese Academy of Science, Beijing. Her main research fields include signal processing and satellite navigation. *The corresponding author.

Yuan Hong, born in 1968, received the B.E. and M.S. degrees in electrical engineering from Xidian University, Xi'an, China, in 1988 and 1991 respectively, and received the Ph. D degree in astrometry from Shanxi Astronomical Observatory Chinese Academy of Sciences in 1995. He did his post-doctoral research in Wuhan Institute of Physics and Mathematics, Chinese Academy of Sciences during 1995-1997. He has been a researcher in Wuhan Institute of Physics and Mathematics since 2000. RSC Yuan was a visiting scholar to the University of Adelaide in Australia from 2001-2002. He is currently the deputy chief engineer of Satellite Navigation Special Overall Department, and the director of Navigation Overall Technical Department. He also is the export of Navigation Special Penal, and the editorial committee of Chinese Journal of Space Science. His major research interests include satellite navigation, ionospheric physics & detection and navigation theory & methods.

LUO Ruidan, born in 1987, received the M.S. degrees in electrical and communication engineering from University of Chinese Academy of Sciences in 2013. Now she is a Ph.D. candidate in University of Chinese Academy of Sciences. Her main research fields are weak signal processing and signal detection.

Xu Duo, born in 1987, received the master degree from School of Information and Electronics, Beijing Institute of Technology, China, in 2013. Her research interests are spaceflight TT&C and telecommunication technology. She mainly focuses on tracking technique of direct sequence spectrum signal and telecommunication between satellite and ground.