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The Design of LDPC Encoder Based on the WIMAX Standard

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Abstract

To meet the higher data rate requirement of encoder, an encoder structure suitable for both two rates(1/2,2/3B) in WIMAX standard is proposed, combined with the method of Design Space Exploration. According to the quasi cyclic characteristics of sparse parity check matrix, the traditional RU algorithm is simplified and optimized to reduce the complexity of the system. Simultaneously we introduce a barrel shifter, and use the method that two rows of the base matrix be restored in one ROM to reduce resource consumption. The simulation results show that the encoder for two rates not only runs successfully, but also reduces the utilization of hardware resources. The encoder architecture has broad application prospects with high flexibility.

Keywords: *WIMAX standard, high flexibility, Design Space Exploration, encoder*

1. Introduction

As channel coding, more and more researchers have been attracted by QC-LDPC [1] because of its high error correction performance. Currently, QC-LDPC has been adopted by a lot of standards, such as WIMAX, DTMB, DVB and so on. How to achieve high efficiency coding in large circuit board is one of hotspots of modern science need to solve. The shift register accumulator (SRAA) in literature [2] is the commonly used encoding m-ethod for general matrices. Literature [3] applies the left loop accumulator for high density matrix multiplication of DTMB standard. In our design making use of WIMAX standard with dual-diagonal structure check matrix, we design an efficient encoder structure through simplifying and optimizing RU algorithm.

2. Encoder Architecture Analysis of Design Space Exploration (DSE)

How to efficiently find methods to meet the hardware structure design of large-space constraints is an important challenge. The micro-encoder is designed based on Design Space Exploration [4] method. The main process is that we must consider resources consumption of the system on a chip (the chip area and storage resources) before loading programmer into the target board. The overall design of the frame is shown in Figure 1.

2.1. Memory Exploration (ME)

The system memory includes A, C matrix memory, information bits memory *etc*. The constrained storage resource determines the maximum number of reused data saved on the chip. In order to achieve resource sharing, the best way is to store reused data among inter-layers on chip memory system. Take 1/2 rate in WIMAX standard for example, we store the sub-matrix $(A, C)^T$ line by line which is obtained after blocking model matrix, reducing the number of storage into half. Specific design detail is shown in Part IV.

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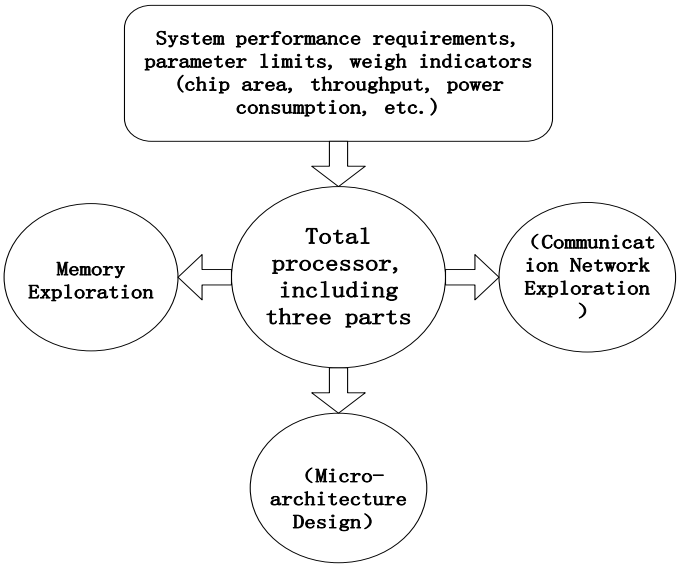

Figure 1. DSE Overall Design Diagram

2.2. Micro-architecture Design (MD)

The Design Space Exploration method includes two levels, Micro-architecture Design and Macro-architecture Design. The Macro-architecture design idea is to adopt multi-pro-cessor parallel process codes. Through the analysis of digital instantiation, we only consider serial input codewords. Micro-architecture design is relatively simple, feasible and resource-saving, and in the case the performance is not affected. The architecture can be realized by inputting data concurrently or sharing ROM modules. Spe-cifically designed micro-architecture will also be given in detail in Part *IV.*

2.3. Communication Network Exploration (CNE)

WIMAX is the Worldwide Interoperability for Microwave Access based on IEEE802. 16e WMAN (Wireless metropolitan area network) technology, in which quasi cyclic LDPC codes is adopted. The standards were defined by 1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6, 6 different LDPC code rates in total. LDPC codes for each bit rate have a total of 19 different kinds of code length. With the satisfying constraint between the lines, we can design encoders only if we change the ROM blocks number and *r* parameter.

3. Encoder Algorithm and Optimization

3.1. Encoder Algorithm Principle

In WIMAX the fundamental matrix determines the parity check matrix. In the matrix -1 represents the whole zero matrix, 0 is the identity matrix, and positive z stands for cyclic shift permutation matrix. In this design expansion factor *z* is 96. The double diagonal structure of matrix *T is* also applicable in other WIMAX standard rates.

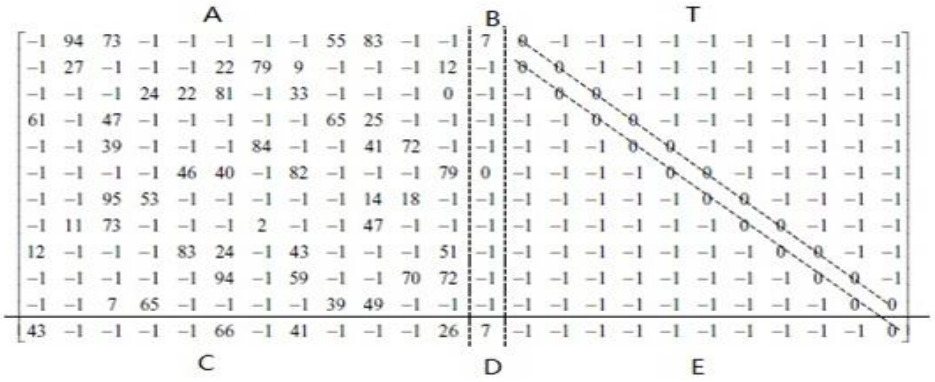

Figure 2. IEEE802.16e Standard's Parity-check Matrix

As shown in Figure 2, RU algorithm [5] will decompose the parity check matrix into *A, B, T, C, D* and *E*. According to the equation $H(s, p_1, p_2) = 0$, the first part p_1 and the second part p_2 can be obtained. *s* represents an information sequence (12*96 bits), p_1 is 96 bits ,and p_2 is 11*96 bits.

$$p_1 = (D + ET^{-1}B)^{-1}(C + ET^{-1}A)s = (C + ET^{-1}A)sl \quad (1)$$

$$p_2 = T^{-1}(As + Bp_1). \quad (2)$$

Every code rate meets $\phi = D + ET^{-1}B = I$, which is the identity matrix in the WIMAX standard, except 3/4B.

3.2. Combining WIMAX Standard Algorithm to Simplify

3.2.1. Simplification of Processes

p_1**:** Encoder's resource consumption often converges on large inverse matrix calculations, so simplifying inverse matrix can make the encoder more simple and the operation more efficient. WIMAX matrices have dual-diagonal structure, so simplification also applies for other rate. Take rate of 1/2 as an example.

Set $T^{-1}As(i) = D(i)$, making the equation left multiplies *T* then transforms into $As(i) = TD(i)$ (Note: *i* represents the matrix rows). According to the particularity of *T* we can get $As(i) = D(i-1) + D(i)$ (and $As(0) = D(0)$). Then we can obtain $p_0(i)$ as follows:

$$D(0) = As(0);$$

$$D(1) = As(1) - D(0) = As(1) - As(0);$$

……

$$D(10) = As(10) - D(9) = As(10) - As(9) - \ldots\ldots\ldots - As(0),$$

$E = (-1,-1,-1,-1,-1,-1,-1,-1,-1,0)$, according to the identity matrix substitution principle, the result of $T^{-1}As$ multiplied by *E* is the last line of $T^{-1}As$.

$$ET^{-1}As = \sum_{i=1}^{11} As(i) \quad (3)$$

$$p_1 = Cs + \sum_{i=1}^{11} As(i) \quad . \quad (4)$$

Finally we get that p_1 equals sum of *Cs* and *As (i)*.

3.2.2. Simplification of Processes

p_2 **:** Through (2) we can obtain that computation of p_2 needs T^{-1} . Assuming $W = As + Bp_1, P = p_2$, we can obtain that $P = T^{-1}W$. To avoid the inverse matrix calculation, transform equation *into* $TP = W$ .The *P* and *W* is decomposed according to the number of rows of *T*, getting that $P = (P_1, P_2, \ldots\ldots, P_{11}), W = (W_1, W_2, \ldots\ldots, W_{11})$. $TP = W$ is expanded into a series of equations :

$$P_1 = W_1;$$
$$\cdots\cdots$$
$$P_{10} + P_{11} = W_{11}.$$

These equations will be written in an iterative formula: $P_i = W_i - P_{i-1}$. (5)

Because of modulo-2 addition, finally get the equation: $P_i = W_i + P_{i-1}$. (6)

Finally, p_2 is simplified to accumulation of the current time value of W ($As + Bp_1$) and previous cycle value of p_2 .

4. Design and Analysis of the Encoder Structure

The proposed encoder is mainly composed of three parts: Intermediate Vector Calculation Module (IVCM), Checksum1 Calculation Module (C1CM) and Checksum2 Calculation Module (C2CM), as shown in the dashed box. The Intermediate vectors *As* (Product of matrix A and information bits s) and *Cs* (Product of matrix C and information bits *s*) are outputted grouped by 96 bits, while C1CM outputs p_1 and C2CM outputs p_2. Eventually they will be written to *Chk* ROM in the form of 96 bits per clock cycle. In successive sections we will give the descriptions in detail.

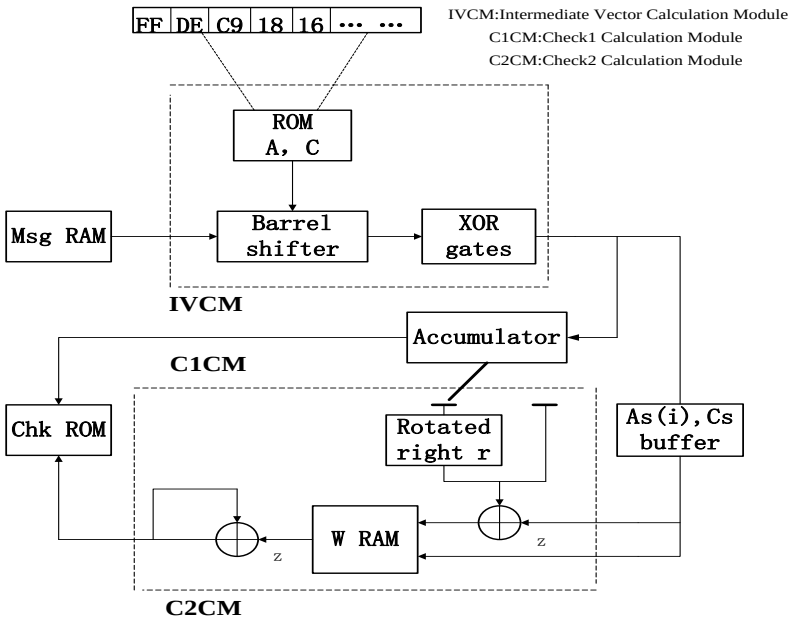

Figure 3. The Proposed Encoder Structure

4.1. Resource Sharing ROM for Matrix *A*, *C*

From (1) and (2), we know that *D* is not needed during the calculation, and *T*'s dual-diagonal structure is simple. Thus most of the values stored in ROMs is from matrix *A* and *C* of the parity check matrix. According to the grouping principle that non-negative values of two rows are not in the same column, we put the 1st and 3rd row, 2nd and 11th row, 4th and 6th row, 5th and 12th row, 7th and 9th row, 8th and 10th row stored in six ROMs respectively, in order to meet the need of resource-saving encoder. ROM is designed in depth of 12, corresponding to the column number in the matrix. Figure 3 shows one ROM for storing the first row and the third row. The maximum shift value is not more than 96, so we need 7 bits to store non-negative value, and another bit as a flag bit. When the flag bit is 1, it represents the value is from the first row; if not, it represents the third row. For example, we fill *FF* as the value in the first column of the first row and the third row is -1. Since the second column value in the first row is 94, with the appending of 1 in the *MSB* we store it as a hexadecimal value '*DE*'. The storage content of six ROMs is shown in Table 1.

Table 1. Storage Content of 6 ROMs

Address	1	2	3	4	5	6	7	8	9	10	11	12
ROM1	FF	DE	C9	18	16	51	FF	21	B7	D3	FF	00
ROM2	FF	9B	07	41	FF	96	CF	89	27	31	FF	8C
ROM3	BD	FF	AF	FF	2E	28	FF	52	C1	99	FF	4F
ROM4	2B	FF	A7	FF	FF	42	D4	29	FF	A9	C8	1A
ROM5	0C	FF	DF	B5	53	18	FF	2B	FF	8E	92	33
ROM6	FF	8B	C9	FF	FF	5E	82	3B	FF	AF	46	48

4.2. Barrel Shifter

Cyclic shift permutation matrix is multiplied with the column vectors, which is equivalent to the shift operation of the column vector. In this design, the multiplication is accomplished by the barrel shifter and XOR gates. We use 96 XOR gates corresponding to the spreading factor. One conventional shift register accumulator SRAA circuit needs 192 flip-flops, 96 XOR gates, and 96 AND gates. 1/2 rate requires 12 SRAA, in other words 2304 flip-flops, 1152 XOR gates, and 1152 AND gates. The barrel shifter requires $(\log_2 z - 1)z$ flip-flops [6], so the intermediate vector calculation module needs 672 flip-flops and 96 XOR gates in all. Barrel shifter is more conducive to resource-saving encoder design.

4.3. Checksum Calculation Modules

Ultimately from (4), p_1 can be obtained by the modulo-2 operation of *As(i)* and a set of 96-bit data of *Cs*. It is calculated by an accumulator, which mainly consists of 96 XOR gates. After calculation p_1 will be stored in *Chk* ROM. The calculation of *W* is detailed as follows. $B = (7,-1,-1,-1,0-1,-1,-1,-1,-1)^T$ We need the nonzero value in matrix *B* for XOR operation with p_1, only in the first cycle and sixth clock cycle, so in the rest of the clock cycles we restore *As (i)* in the *W* RAM. The shifting value *'r'* is determined by the non-negative element in matrix *B*. In the first clock cycle, *r* has the value of 7. So p_1 is shifted right 7 bits, whose XOR operation with the first set of 96-bit data *As (1)* will be written in *W* RAM. In the sixth cycle, the modulo-2 operation of p_1 and *As (6)* is written in *W* RAM (the rotation is completed by a key switch).

After all the data is stored in *W* RAM, open the read enable port. Add the current value of *W* to the last p_2, and then we will obtain p_2.

4.4. Applicability of the Encoder

The proposed encoder is not only suitable for 1/2 rate, but also applicable to 2 / 3B rate. Because the dual-diagonal structure exists in all rates under WIMAX standard, the design of C2CM is universal. But the rate containing some non-negative elements in the same column can not use this encoder structure. In 2 / 3B rate, we need 4 ROM while in 1/2 rate, the amount is 6. What's more, *r* has the value of '7' and '95', in 1/2 rate and 2/3B rate respectively. The design is expected to make significance for the prospect of the universal encoder.

5 .Simulation Results

Based on the above micro-architecture design and improvement, the encoder of LDPC codes is compiled and simulated in two rates using Verilog HDL language and Cyclone II P2C70F896C6 chips, and the simulation results are given in Table 2. It shows the resource consumption of 1/2 rate and 2/3B rate with code length 2304. From the usage elements and the resource utilization, we see the proposed encoder is efficient and resource-saving. The availability of resources facilitates the enhancement and expansion of the entire system.

Table 2. Resource Usage Summary of Two Rates

Resource Usage Summary	1/2 rate(utilization)	2/3B rate(utilization)
Total logic elements	8,329(11%)	4999(7%)
Total combinational functions	7,849(11%)	4997(7%)
Total registers	5007(7%)	3212(5%)
Total pins	303(47%)	291(47%)
Total memory bits	6,240(<1%)	1152(<1%)

Meanwhile, based on the Modelsim simulation platform, coding waveforms are output successively, which verifies the correctness of the results compared with coding on MATLAB platform.

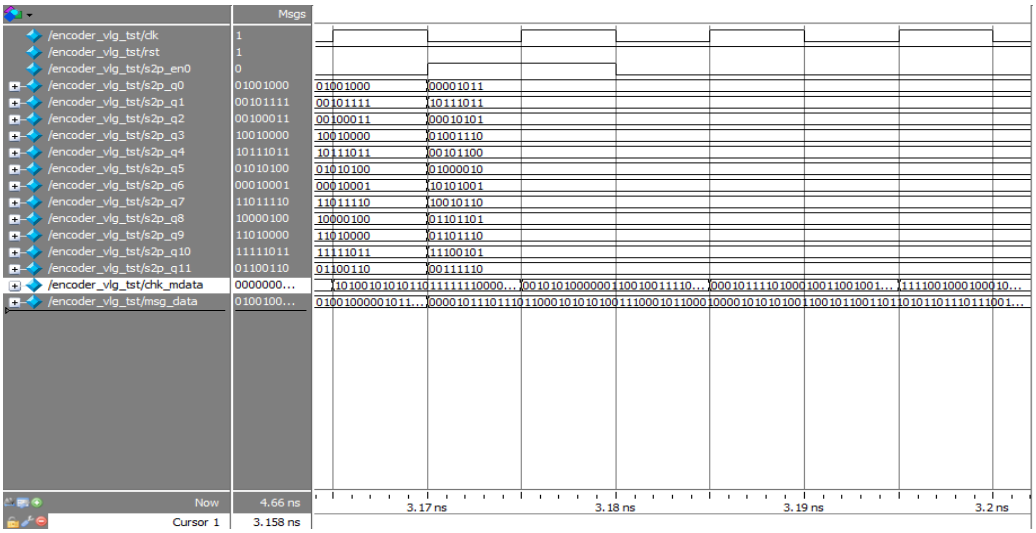

Figure 4. Simulation Waveforms of 1/2 Rate

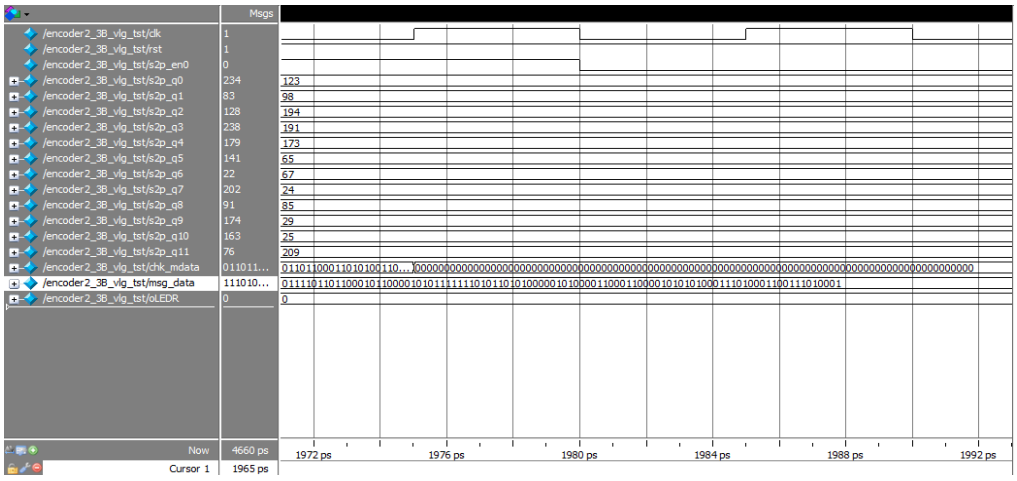

Figure 5. Simulation Waveforms of 2/3B Rate

Figures 4 and 5 depict 1/2 rate and 2 / 3B rate of LDPC codes in Modelsim SE 10.0 respectively. *S2p-q0 ~ s2p-q11* are inputted with the length of 96 bits, 8 bits every word. Input them when *s2p_en0*=1, and output *'msg-data'* and *'chk-mdata'* in final. The information bits *'msg-data'* includes 12 groups of *s2p-q0 ~ s2p-q11* and *'chk-mdata'* presents all the parity bits, 12*96 bits in length.

6. Conclusions

Based on the methodology of encoder design exploration and aiming to reduce hardware consumption, an efficient encoder architecture suitable for both 1/2 rate and 2/3B rate under WIMAX standard was proposed.

In the exploration of the memory design, we adopt the idea of storing two lines of data in one ROM to achieve the sharing of resources, and the amount of memory is reduced to half of the original. Combined with specific analysis using the WIMAX standard, we further simplify the RU algorithm, thus greatly simplifying the structure of the encoder. The final design can be applied to two rates by summarizing the similarities and differences in the structural characteristics of each base matrix. We expect that the proposed encoder will make certain significance for the future design of multi-rate encoder.

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