Design of a Two Stage Low Noise System in the Frequency Band 1.8-2.2GHz for Wireless System

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Abstract

In first stage of each microwave receiver there is Low Noise Amplifier (LNA) circuit, and this stage has important rule in quality factor of the receiver. This paper presents the design of LNA and development of low bias (VD=3V, ID=20mA), the LNA operating in frequency range 1.8-2.2GHz using a feedback circuit. Design System (ADS) 2012 tool was used for design and simulation, and each design was tuned to get the optimum value for NF, power gain (S21), input return loss (S11) and reverse isolation (S12). Simulation results have indicated that the S21 achieves 33.2515±0.4475dB over the wide frequency band of 1.8-2.2 GHz, the gain was almost flat over the whole band. Noise figure (NF) maintains is 0.4945±0.0565 dB, S12 < -47.089 dB and S11 < -16.126 dB in the entire band.

Keywords: Low noise amplifier, HEMT, Feedback, Noise Figure, ADS

1. Introduction

In the era of wireless communications, devices that are able to exchange information through modulated radio frequency waves acquire more and more importance. Wireless communication and its applications have travelled through rapid growth in recent years. Cellular systems, WLANS, Bluetooth as well as WPANs have undergone numerous generations of evolution in the swift development in wireless communication [1].

LNA are used at receiver's side in all communications systems in order to offer the first amplification to the received signal with the addition of the minimum noise. Although LNAs are parts of the receivers only, their design should take into account the general features of the whole communications system [2]. Since the incoming signal from an antenna is usually weak, the unavoidable noise generated in the amplifier must be as low as possible, to obtain an acceptable "signal to noise" at the output of the amplifier. Therefore, one of the key design goals for the LNA is a low noise contribution to the input signal, together with a good impedance matching to the signal source, a sufficiently large output signal dynamic range and a low power consumption.

Most of the single stage LNA device in the review could only around 20 dB gain. It was proposed that the low noise amplifier should have a gain of at least 30 dB. So the proposed LNA will be designed by two stage.

2. LNA Design

The design of LNAs, there are several common goals. These contain minimizing the NF of the amplifiers, providing gain with sufficient linearity, and supporting stable input impedance are all-important considerations [3].

In order to make an LNA, the choice of transistor is critical. This is one of the most important steps in designing a low-noise-amplifier (LNA). Different types of transistors

are available for LNA applications. According to specifications, appropriate transistor should be selected for low-noise-amplifier due to its low NF and high gain [4]. The numbers of transistors are limited at the interested frequency. In this work, ATF54143 is chosen.

2.1 Bias Circuit Design

The S-parameters of the transistor are fixed and do not change as the correct bias current is maintained. In order to meet the design goals for NF, intercept point and gain, the drain source current (ID) was chosen to be 40mA. FET in the amplifier is biased at a Vds of 3V and Id of 20mA, giving a total current of 40mA. As indicated by the characterization data shown in the device data sheet, 20mA gives the best NF. Also shown in the data sheet, a 3V drain to source voltage (Vds) gives a slightly higher gain and is also preferred since it easily allows the use of a 5 V regulated supply.
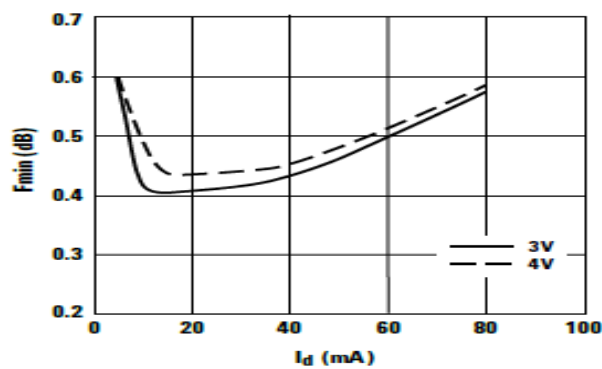

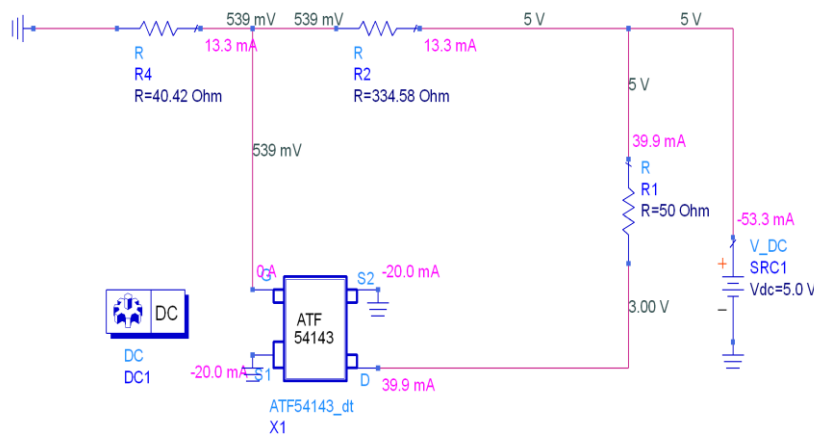**Figure 1. Fmin vs. Ids Tuned for Max OIP3 and Fmin at 2GHz**

Figure 2. Actual Bias Circuit is Designed in ADS

The DC analysis is used to calculate the power consumption. First to set the power consumption requirement, we have to adjust the DC bias resistor, transistor sizes and source degenerated inductor. The DC current was found with the help of DC simulations.

After processing of ADS simulation Data, we can obtain the actual bias circuit. The actual bias circuit is shown in Figure 2, the actual electricity current and voltage can be seen in the Figure. The resistors are calculated to be R1=50 ohm, R2=334.56ohm, R4=40.42ohm. Conduction a DC analysis in the ADS circuit simulator produces

ID=20mA, Ids=39.9mA and VD=3.0V, which are very close to our original goal (minimum NF).

2.2 Stability Analysis

An important part of amplifier design is stability. In the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. The "Stability Factor and Measure" parameters are real functions of frequency and are available for 2-port networks only. These parameters aid in determining the stability of the 2-port network. If S12 of a device is not zero, a signal path will exist from the output to the input. This feedback path creates an opportunity for oscillation.

The stability factor is given as

$$K = \frac{1- \mid S_{11} \mid^2 - \mid S_{22} \mid^2 + \mid \Delta \mid^2}{2 \mid S_{12}S_{21} \mid} > 1 \quad (1)$$

And

$$\Delta = S_{11}S_{22} - S_{12}S_{21} {}_{<1} \qquad (2)$$

When the K>1, the circuit will be unconditionally stable for any combination of source and load impedance. When K<1 then circuit is potentially unstable and oscillation may occur with a certain combination of source and /or load impedance presented to the transistor. The K factor represents a quick check for stability at given frequency and given bias condition.

The length of these microstrips is determined from the knowledge of the wave length which in turn depends on the effective dielectric constant ε_{eff}. For this design, we intend to deploy for simplicity microstrips with Z0=50Ω . Using equation (3) with a substrate of ε_r =3.48, we obtain for the microstrip a width-to-height ratio of w/h=2.266, corresponding to a strip width of 45.3mil on a 20mil substrate. Compensating for 1.4 mil strip thickness using equation (4), the final strip width is 43.835433 mil. The effective dielectric constant is found to be ε_{eff} =2.734 according to equation (5). This determines the wavelength at f=2GHz (the center frequency) to be $\lambda = c / (f / \sqrt{\varepsilon_{eff}})$ =3571.56 mil. The λ /4 bias stubs are thus 893 mil long [5].

$$\frac{w}{h} = \frac{2}{\pi} \left(B - 1 - \ln(2B - 1) + \frac{\varepsilon_r - 1}{2\varepsilon_r} \left[\ln(B - 1) + 0.39 - \frac{0.61}{\varepsilon_r} \right] \right) \quad (3)$$

$$w_{eff} = w + \frac{t}{\pi} \left(1 + \ln \frac{2X}{t} \right) \qquad (4)$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left(1 + 12 \frac{h}{w} \right)^{-\frac{1}{2}} \qquad (5)$$

The schematic diagram of simulating stability factor is shown in the Figure 3, Here, the DC source of 5V supplies DC bias. C1, C2 are bypass capacitors, respectively. where C1=C2=C3=C4=270pF. Actual models of capacitor in the above circuit were adopted from the Murata Components Library for Agilent ADS. The accuracy and efficiency of simulations have been improved, since physical effects of the layout components were taken into account. C1 and C2 can improve the stability of low frequency. In order to get unconditionally stable circuit, we can add negative feedback inductor to the source of the transistor.
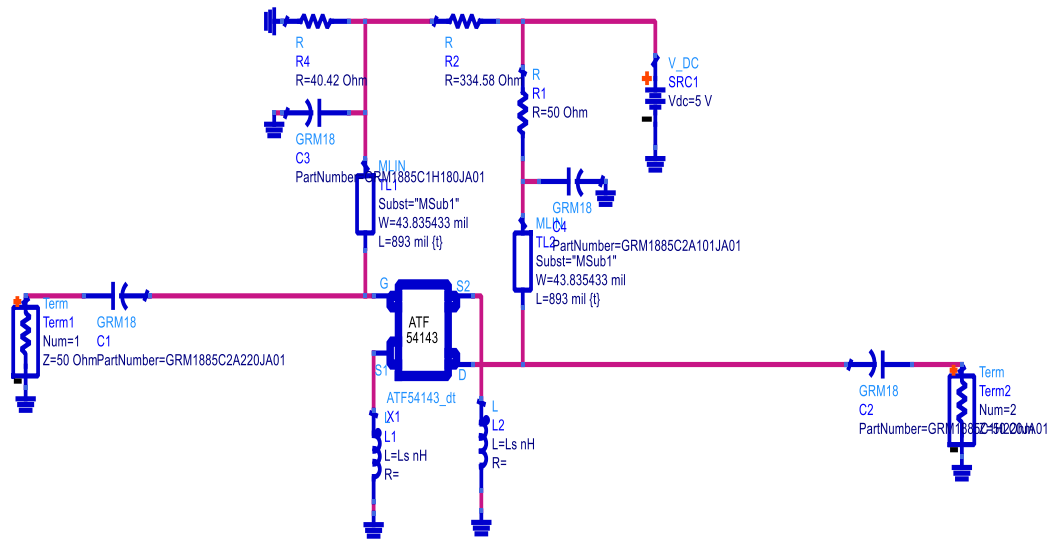
Figure 3. The Schematic Diagram of Simulating Stability Factor, when the Feedback Inductor Adds to the FET's Source
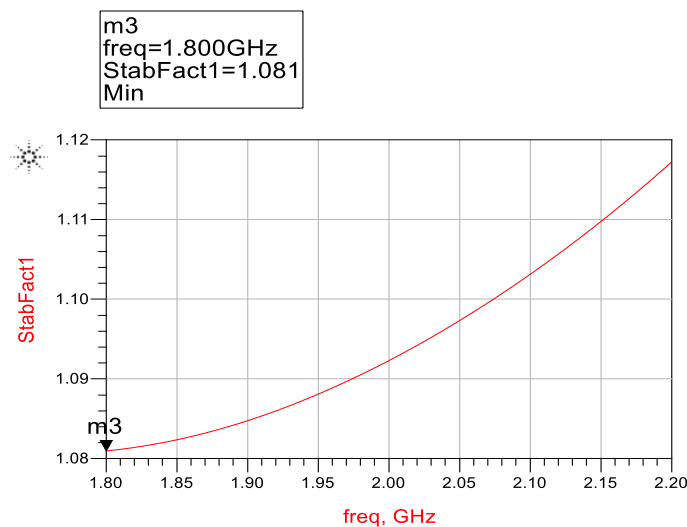

Figure 4. The Stability Factor of Single LNA

When we add feedback inductor in the FET's source, the maximum stability is achieved for L1=L2=0.8nH. In Figure 4, we can know the K>1 over the frequency band of 1.8-2.2GHz.

2.3 Noise in Amplifiers

At this point, it is worthwhile to examine the notion of noise, and modeling of noise in fundamental circuits. Amplifiers are being used to enhance the signal that is generated by a weak signal source. LNAs are being used to receive and amplify weak signals transmitted by distant transmitters, which may be fixed or mobile, or installed on board a satellite. The total signal received at the input of the amplifier does not only consist of the signal sent by the transmitter, but in addition, it includes the unavoidable noise signal originating from the internal resistance of the antenna. To obtain a sufficiently high level

of signal power with a reasonable signal-to-noise ratio (S/N) at the output of the LNA, the noise inherently generated in the amplifier must be kept as low as possible.

NF is one of the most important parameters to evaluate the radio performance of communication system. It is a measurement of degradation of signal-to-noise ratio (SNR) between the input and output of the component

The NF can be calculated using the following mathematical equation [6]:

$$NF(dB) = 10 \log F \tag{6}$$

Where

$$F = \frac{(S/N)_{input}}{(S/N)_{output}} \tag{7}$$

We can characterize the performance of a particular receiver element by its NF, which is the ratio of actual output noise of the element to that which would remain if the element itself did not introduce noise. The total NF of a receiver system (a chain of stages) can be calculated using the Friss formula as follows:

$$NF = NF_1 + \frac{(NF_2 - 1)}{G_1} + \frac{(NF_3 - 1)}{G_1 G_2} + \ldots + \frac{(NF_n - 1)}{G_1 \cdots G_{n-1}} \tag{8}$$

The total system NF equals the sum of the NF of the first stage (NF1) plus that of the second stage (NF2) minus 1 divided by the total gain of the previous stage (G1) and so on. This result suggests that the noise contributed by each stage decreases as the total gain preceding that stage increases, implying that the first few stages in a cascade are the most critical. It is understandable that the total NF is dominated by the NF1, which is the NF of the LNA.

In receiver applications, it is often required to have a preamplifier with as low a NF as possible, as the first stage of a receiver front end has the dominant effect on the noise performance of the overall system.

Note that in a cascaded system, the NF1 of the first-stage is directly added to the overall system NF but noise contribution from any stage except the first stage is reduced by the gain of its preceding stage or stages. Therefore, for better noise performance of a cascaded system, along with a high gain the first stage should have the minimum possible NF.

2.4 Input Matching

Low-noise-amplifier (LNA) is one of the most important key components of the communication system. It is used in the input stage of the receiver. It deals with two important parameters such as gain (in dB) and the NF. In a few words, the purpose of the LNA is to amplify the received signal to acceptable levels while minimizing the noise which is added from the channel. According to Friss equation (equation 8), it is very important for RF and microwave engineers to design RF receiver with low noise at the input stage. Once the signal is received by the antenna, passing through LNA, it is not possible to get the high gain and low noise at the same time. That's why, it is important to consider a trade-off between gain and NF.

Matching networks is one of the important steps to design LNA. Impedance matching is used to minimize the reflections and obtain an acceptable amount of NF and maximum gain by making the load impedance equal to the source impedance. To get an optimal value of input reflection coefficient, gain and NF; input matching network is tuned and for output reflection coefficient; output matching network (OMN) is tuned.
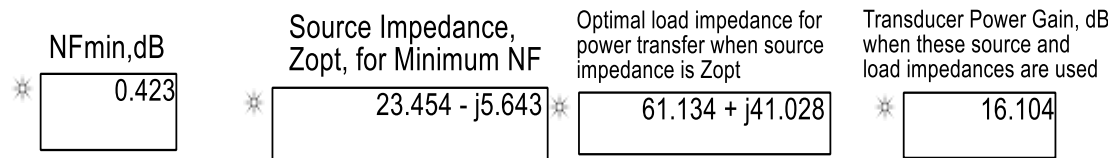
NFmin,dB	Source Impedance, Zopt, for Minimum NF	Optimal load impedance for power transfer when source impedance is Zopt	Transducer Power Gain, dB when these source and load impedances are used
❈ 0.423	❈ 23.454 - j5.643	❈ 61.134 + j41.028	❈ 16.104

Figure 5. Gain and Noise Circles and Optimal Source and Load Impedances for Minimum NF

Generally it is not possible to obtain both minimum NF and maximum gain for an amplifier. So, some sort of compromise must be made. This can be done by using constant gain circles and circle of constant NF to select a usable trade-off (check it from book, trade off: up-down or compromise: linear) between NF and gain.
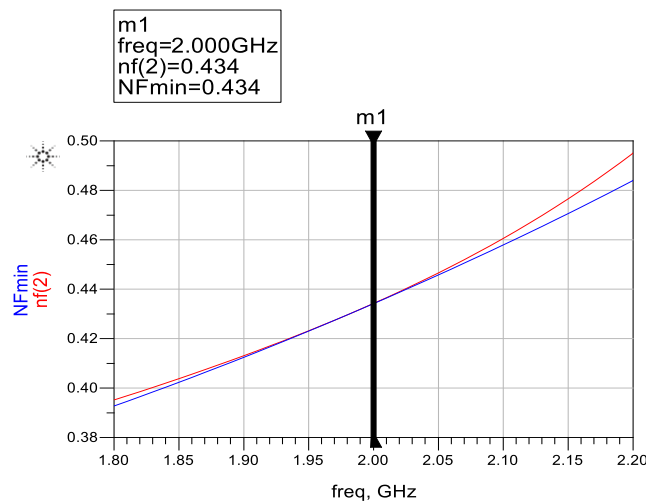

Figure 6. Simulation Result of NF and NFmin, when Noise Circles and Optimal Source and Load Impedances for Minimum NF

In our LNA design, Noise is more important than gain, then a source impedance to minimize Noise could be chosen, so the first stage of the LNA is designed to drive the NF and the second stage of the LNA offers necessary gain. Determine the optimal source and load impedances to present to the stabilized FET, via S-parameter and NF simulations, using the SP_NF_GainMatchK schematic from the Amplifier DesignGuide. The data display, shown in Figure 10, shows that with a source impedance of 23.454-j*5.643 ohm, the NF is about 0.423dB.

S-parameter analysis was also used to generate the NF of the LNA. The minimum and actual NF of the LNA was simulated using scattering parameters. Figure 6 shows that the LNA has a NFmin and NF are of approximately 0.472 and 0.472 at 3 V supply voltage which is very close to its minimum NF at 2 GHz operating frequency.

2.5 Analytical and Circuit Simulation Results

The schematic of the proposed LNA is shown in Figure 7, the feedback inductor is replaced by Microstrip lines, because the inductor is too small which is difficultly designed. The input, interstage and output matching networks are composed of microstrip lines. The LNA is composed of two stages. The designed circuit of Figure 10 is simulated with ADS 2012 tools. TL1, TL2, TL4, TL5 and TL6 sizes art set to L1=405.035433mil, L2=359.019291mil, L4=334.064493715mil, L5=115mil and L6=26mil.
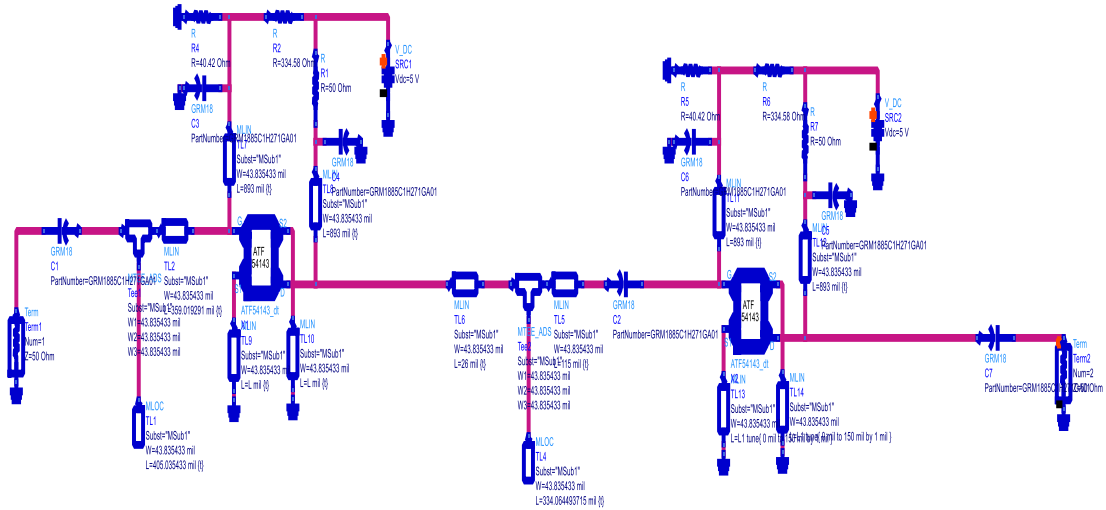
Figure. 7. Two Stage LNA Schematic Diagram

The simulation results are shown in Figure 8, Figure 9, Figure 10, Figure 11, Figure 12. In Figure 8, NF between 0.438 and 0.55dB, we can know nf(2)=0.485 dB and NFmin=0.484dB, which is very close to its minimum NF at 2 GHz operating frequency, when the Two Stage LNA operating in 2.0GHz.
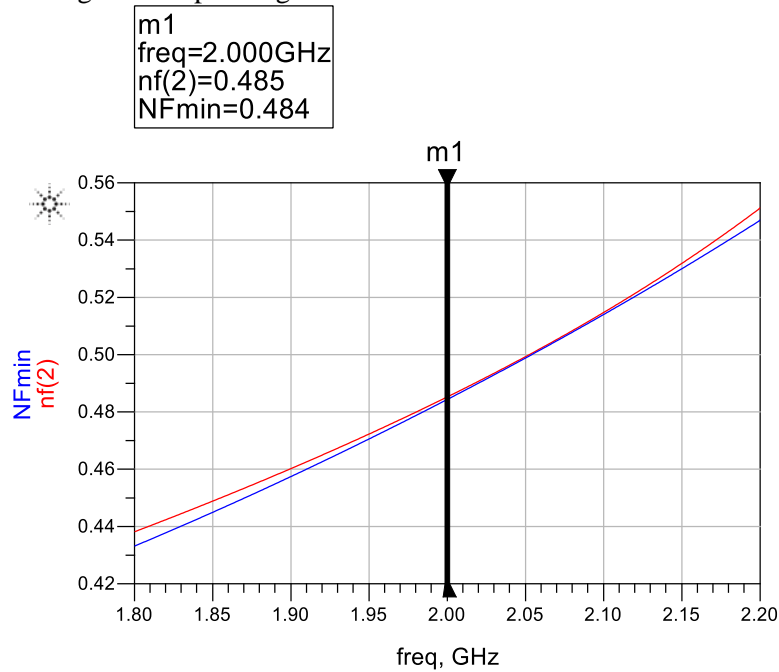

Figure 8. Simulation Result of NF and NFmin

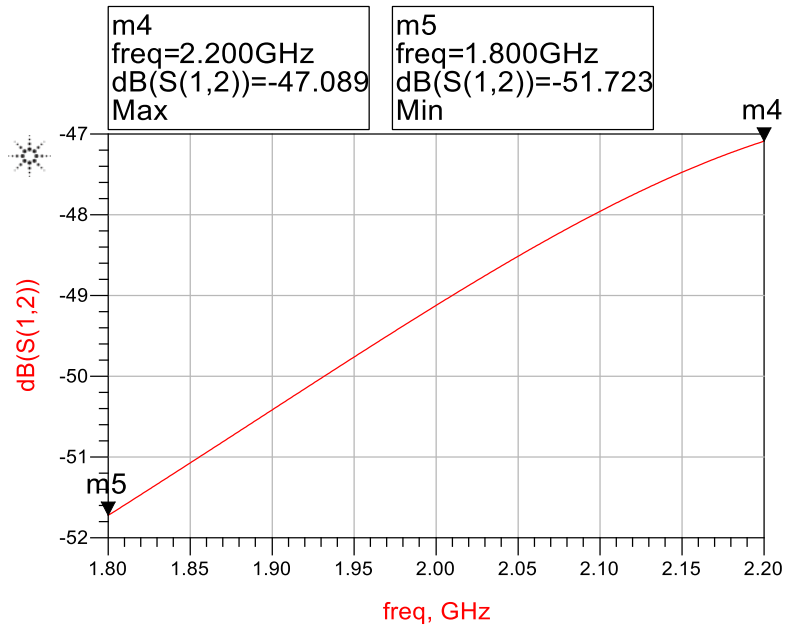In Figure 9, The reverse power gain S12 is simulated to is less than -47.089dB throughout the operating band.

m4
freq=2.200GHz
dB(S(1,2))=-47.089
Max

m5
freq=1.800GHz
dB(S(1,2))=-51.723
Min

Figure 9. Simulation Result of S12

In Figure 10, we can know S11 is below -16.126 dB in the entire band, which shows the perfectly matched.

m1
freq=2.051GHz
dB(S(1,1))=-32.050
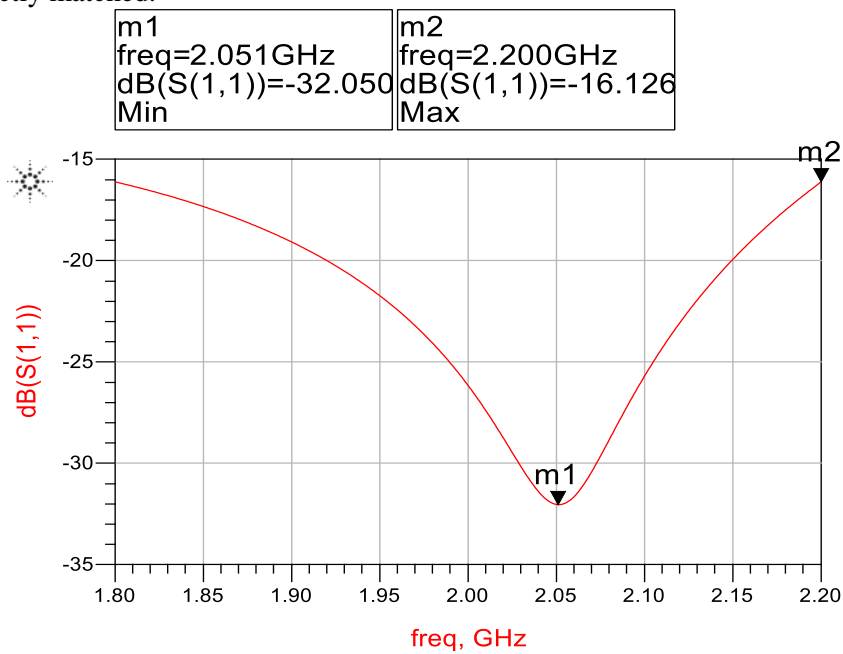Min

m2
freq=2.200GHz
dB(S(1,1))=-16.126
Max

Figure 10. Simulation Result of S11

In Figure 11, we can know Stability Factor is more than 1 dB in the entire band, the proposed circuit will be unconditionally stable.
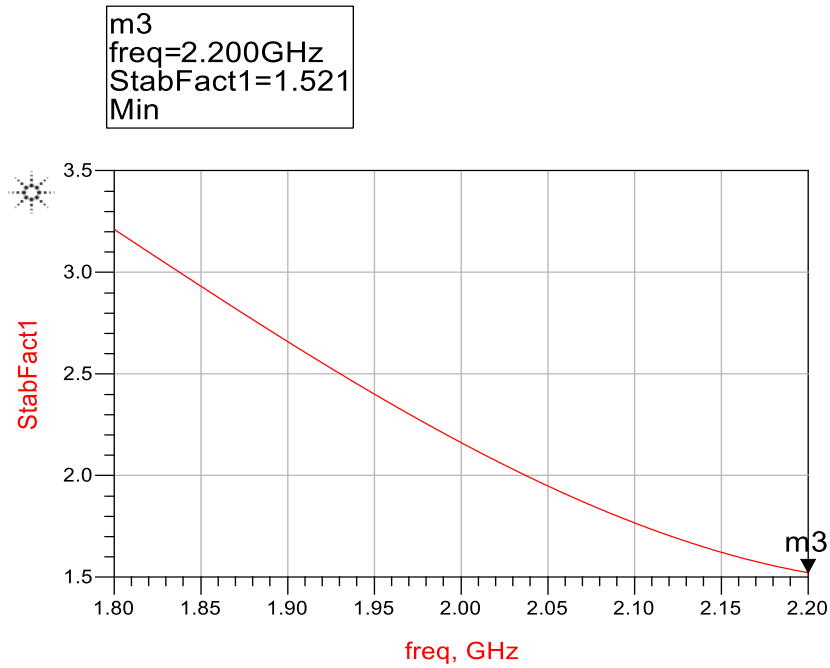
m3
freq=2.200GHz
StabFact1=1.521
Min

Figure 11. Simulation Result of the Stability Factor

In Figure 12, we can know S21 is more than 32.84 dB in the entire band, the simulation result reveal a relatively flat gain from 1.8 to 2.2 GHz.
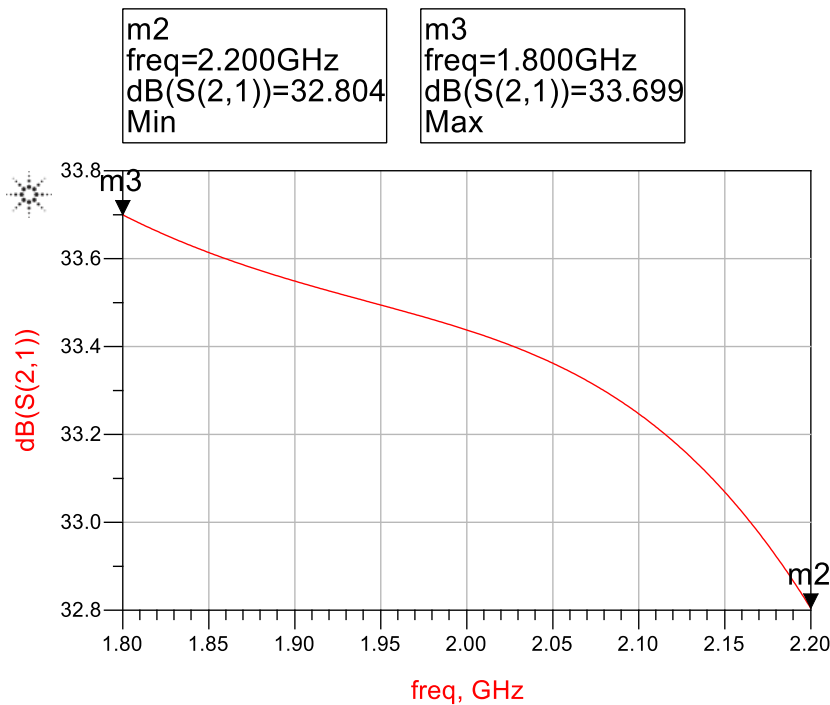
m2
freq=2.200GHz
dB(S(2,1))=32.804
Min

m3
freq=1.800GHz
dB(S(2,1))=33.699
Max

Figure 12. Simulation Result of S21

A comparison of our work with other previous LNAs is listed in Table 1.

Table 1. Performance Comparison of the Proposed LNA with Other Previous LNAs

	BW(GHz)	S11(dB)(Min)	S21(dB)(Min)	S12(dB)(max)	NF(dB)(max)
This work	1.8-2.2	-32.05	30.952	-44.976	0.571
[7]	1.8-2.2	-28.92	16.68	NA	1.25
[8]	1.85-2.48	<-5.5	16	NA	1.77
[9]	1.9	-9.34	29.13	-43.02	0.44
[10]	1-2	<-12	15	NA	<0.8
[11]	2	-9.842	15.87	-42.86	3.775

3. Conclusion

In this work, the final Two Stage LNA operating from 1.8GHz to 2.2 GHz had been designed. In this work, the LNA operating from 1.8 GHz to 2.2 GHz had been designed. Feedback technique has been employed in the LNA design in order to meet the design specification over the wide frequency ranges. The matching and biasing circuits are also carefully designed so that the design specifications are met with lowest count parts. Tuning and optimization of the circuit is very crucial to make sure that the LNA gives the best performance. The final Two Stage LNA with Murata components and microstrip lines are designed with ATF-54143. The simulation results show S11 below -16.126dB, flat gain S21 of 33.2515±0.4475 dB, the gain was almost flat over the whole band, S12 below -47.089dB, and flat NF of 0.4945±0.0565dB over the whole band.

The proposed Two Stage LNA is good candidate for wireless applications due to its low NF and high gain. Furthermore, throughout the whole design, transistor was stable. The level of satisfaction of this thesis work is satisfactory. Though the responses are satisfactory, but still there are scopes to improve the performances. Some of the circuits can be improved in design and with more proper optimization to have better responses. This thesis work gives a closer and wide view of all the relevant background theories and design technologies to the designer.

Acknowledgment

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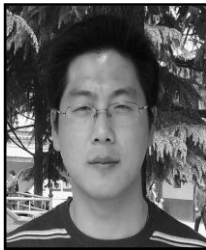
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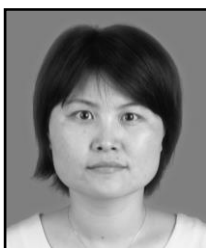
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