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Design and Implementation of the Packets Transceiver System of Ethernet MAC Layer

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Abstract

As we all know, Network communication is essential in network transmission, while the transmission delay of Ethernet's MAC (Media Access Control) layer will affect the quality of communication networks with the continuous progress and development of Ethernet technology. In this paper, we design and implement the correct receiving and sending of Ethernet MAC protocol layer's packets with FPGA, through the in-depth analysis of Ethernet MAC packets transceiver. The simulation results of the transceiver module system level were given through the simulation test plat form we built, which shows that Ethernet MAC layer's packets designed on the FPGA-based platform can receive and send faster, and the low system occupancy rate can meet the requirements of system throughput for real-time communication environment system, which can provide the technical support for the development of Gigabit Ethernet.

Keywords: *Ethernet, MAC protocol layer, FPGA, ASIC*

1. Introduction

Ethernet technology was born in the Palo Alto Research Center in 1975, Ethernet is a broadcast network used the CSMA / CD protocol mechanisms, and is essential in the enterprise, science and technology, military research and other fields with the advantages of high flexibility, mass media information, easy to expand and update and the like, as a LAN media access technology [1].Currently, the vast majority of networks are using the Ethernet technology, and the new research programs of global "wisdom of the Earth" and "smart city" proposed make the research of Gigabit Ethernet get an unprecedented development, and which has become the mainstream of network technology.

According to OSI (Open System Interconnection, Open Systems Interconnection) seven-layer network model, the key of Ethernet technology is the physical layer and the data link layer, where data link layer includes the media access control MAC (Medium Access Control) sub-layer and logical link control LLC (Logical Link Control) sub-layer [2], MAC sub-layer mainly contains the access content related to the transmission media, and which is independent in the actual network transmission. Therefore, it has important significance for the study of Ethernet MAC layer protocol.

The traditional ASIC products have high mask costs in the research and development of Ethernet products, which has limited the continuous development of the integrated circuit [3-4], and Gigabit Ethernet network requires a higher throughput, lower congestion, and lower transmission latency, which provides a good development opportunity for FPGA.

FPGA (Field Programmable Gata Array) is a programmable logic device, and is the mainstream technology in the field of electronic design currently. It configures a complete set of system design automation software including design, simulation, and test, with the

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features of high speed, high precision, reconfigurable, and the short development cycle and low-cost, and the perfect combination of the standardized programming structure of VHDL hardware description language [5-6], which makes it rapidly become the first choice of low-end products. Paper [7] took the combination of ARM and FPGA into consideration, designed an NC System. Paper [8] implemented the design of high-speed serial transmission interface based on FPGA. Poure *et. al.,* [9-10] achieved some applications of FPGA-based reconfigurable control. Xie *et. al.,* [11] designed a remote control system for intelligent instruments based on FPGA. Therefore, the design and implementation of Ethernet MAC protocol based on FPGA, and applying it to Ethernet-related applications, have certain practical significance and application value.

2. Design of the Packets Transceiver of Ethernet MAC protocol Layer Based on FPGA

After in-depth analysis of Ethernet MAC protocol, the Ethernet MAC protocol is divided into three modules (data reception, data transmission, control and management) according to its overall function in this paper. The encapsulation and encapsulation of Ethernet packets are mainly through the data reception and transmission module, while the control and management module is mainly used to achieve the communication with external PHY chip. The overall structure design frame diagram of Ethernet MAC sub layer protocol is shown in Figure 1.

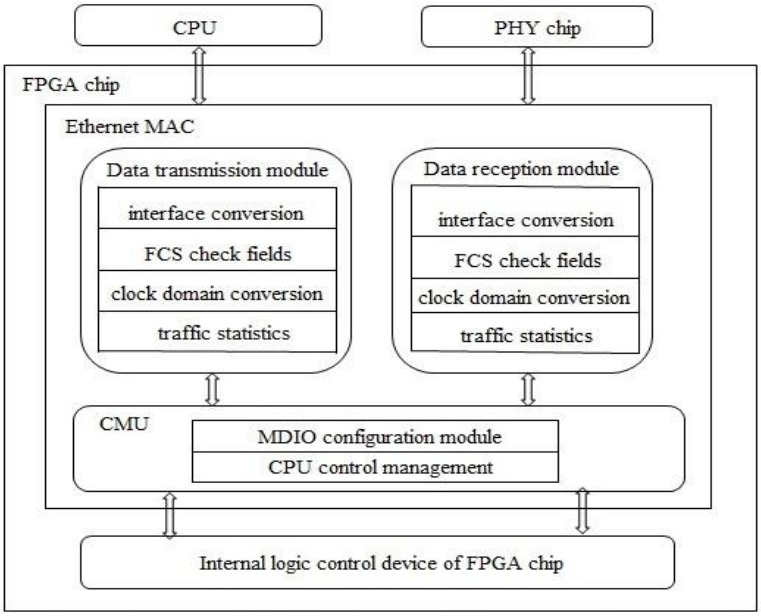

Figure 1. Overall Structure Design Frame Diagram of Ethernet MAC Sub Layer Protocol

Through the analysis of the system's overall design structure, the hardware structure block diagram of Ethernet MAC sub layer protocol is shown in Figure 2, which consists of the control module, the transmission module and the reception module. In the design of communication mode, half-duplex communication mode is chosen, which makes the system have low network load, small communication delay, and simple hardware design structure.

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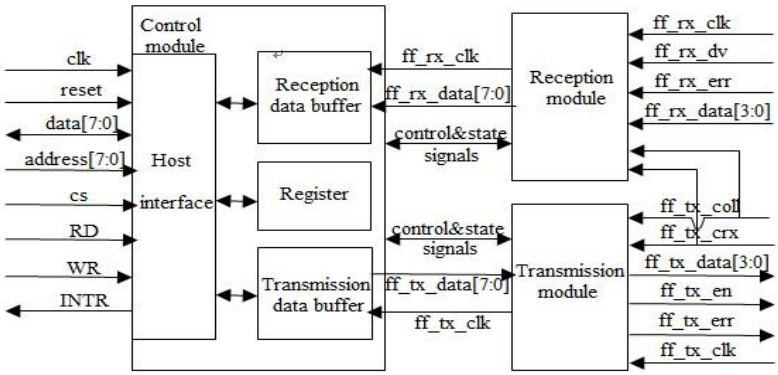

Figure 2. Hardware Structure Block Diagram of Ethernet MAC Sub Layer Protocol

2.1. Design of the Data Reception Module Based on FPGA

Data reception module is mainly responsible for receiving data packets from PHY chips of external physical layer, which achieves data packets reception by setting the Ethernet 10/100/1000 IP cores in this paper, mainly including the functions of Ethernet data frame delimitation, frame synchronization, data FCS checksum, the identification and elimination of data packets' padding field, and the statistics of data packets received and the like. The composition frame diagram and processing flow chart of data reception module are shown in Figure 3 and Figure 4 respectively.

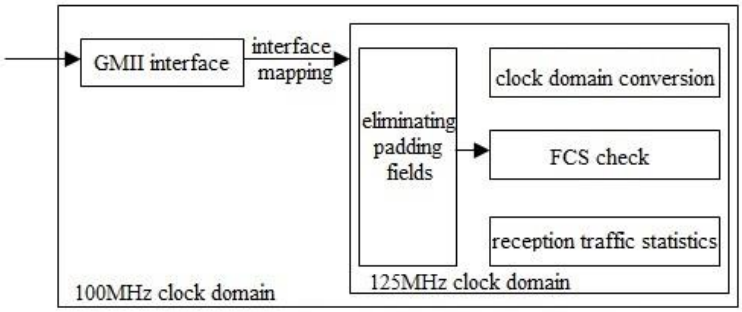

Figure 3. Composition Frame Diagram of Data Reception Module

Data reception module consists of GMII interface data conversion module [12], MAC clock domain to System clock domain conversion module, FCS check module, removing redundant padding bytes module, and receiving traffic statistics module. This module will detect the change of the input signals at the PHY chips' interface, and carry on different operations according to the input signals. If the input signal indicates the data frame is invalid, the module does not perform any operations and discard the data frame; while the input signal indicates the data frame is valid, the module will receive the inputted data packets, analyze and inspect the received data, and scan the data packets to determine whether the packet has been filled at the same time, if yes, the padding bytes will be removed, otherwise, will be no operation. While receiving data packets, Ethernet 10/100/1000 IP cores will call the relevant module to calculate data packets' FCS, it doesn't stop calculating until the scan reaches to the end of the packets, if the calculation result is zero, which indicates the packets are transmitted correctly.

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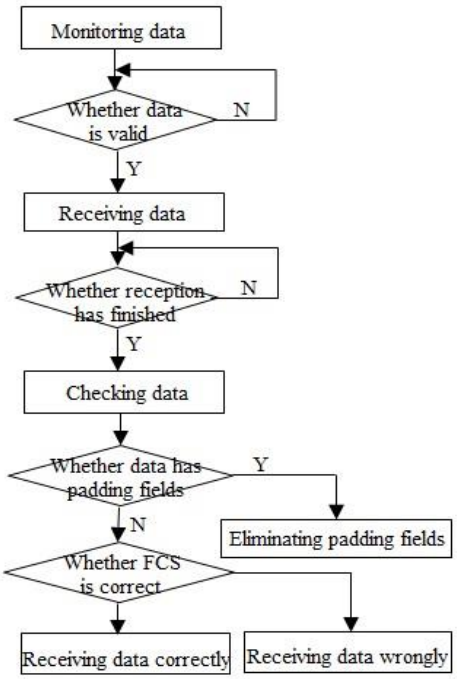

Figure 4. Processing Flow Chart of Data Reception Module

MAC Clock Domain to System Clock Domain Conversion Module: In this paper, the operating frequency of MAC controller is 100MHz, and the frequency of system end is 125MHz, so it is necessary to convert the MAC clock domains. We use double latches method to process the data signal of clock domain crossing, which is the signal of the source clock domain will latch twice using latches on the purpose clock domain. Phase-locked loop structure diagram is shown in Figure 5.

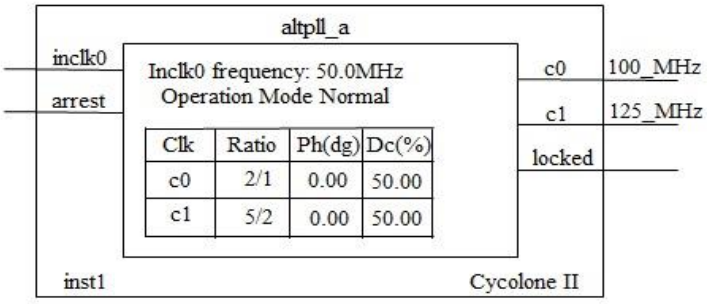

Figure 5. Phase-Locked Loop Structure Diagram

Where the system clock provided for inclk0 is 50MHz, the output are:c0, 100MHz; c1,125MHz. c0 provides clock for theff_tx_clk and ff_rx_clk of three-speed Ethernet(Ethernet 10/100/1000); c1 providesclock for thetx_clk and rx_clkof three-speed Ethernet.

2.2. Design of the Data Transmission Module Based on FPGA

Data transmission module is designed to transmit data packets to PHY chips of external physical layer, mainly including the functions of the generation of Ethernet MAC data frame, adding data packets FCS, padding data packets, and the statistics of data packets received and the like. The data needed to be written into ff_tx_data sequentially when

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sending packets, Ethernet 10/100/1000 IP core will process the data (add local MAC, calculate the checksum, *etc.*), and be sent out through GMII interface. In fact, data transmission is the reverse process of data reception.

The overall processing flow chart of data transmission module is shown in Figure 6.

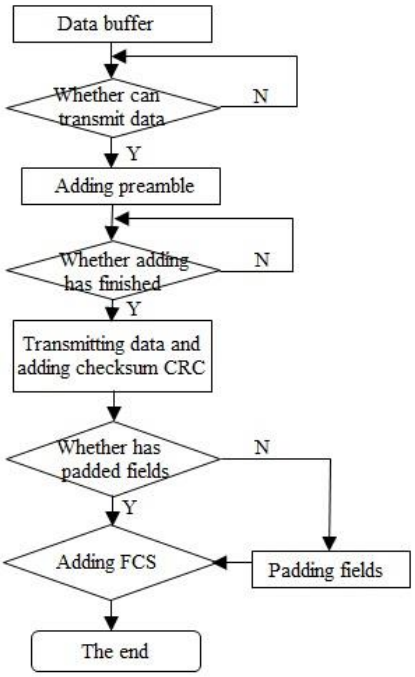

Figure 6. Processing Flow Chart of Data Transmission Module

Data transmission module is designed to transmit packet as a unit, when the module in this system is ready to send a data packet, it will encapsulate these packets, and the packets sent to PHY chips of external physical layer need to add MAC leading frame before the valid data. At same time, the frame sequence FCS of packets is detected according to the CRC-32 checksum algorithm, and finally these valid data sent will be checked whether beyond the effective length of Ethernet data frames or not, if which is less than 60 bytes, it needs to fill with zero bytes. The transmission process of the entire data packets is just completed in this way.

2.3. Design of the Control Management Module Based on FPGA

This module is mainly responsible for achieving external control, interfaces configuration, and including the configuration of data packets' sending interval, and the external PHY chips through MDIO interface, and the load s of system traffic statistics information and the like. While carrying on the logic design using FPGA, the module achieves its control function through Ethernet 10/100/1000IP core provided by Alter.

3. System Simulation and Test

The design and implementation of Ethernet MAC protocol use the Cyclone II FPGA of Algerian this paper. Through simulation and test, we know this system can achieve the basic functions of data transceiver of Ethernet MAC protocol layer, and the transmission rate can be up to 1Gbps. In addition, the simulation test platform of our system is mainly Quartos II, we choose it to create the Ethernet 10/100/1000 IP core, which belongs to the data link layer in the entire network layer, and is mainly responsible for adding up packet header of the data which users need to send,

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sending it out after checking; and accepting the data packets from the physical lines, then sending the data to users after separating it out.

3.1. Initialization Test

The initialization of this experiment is mainly aimed at Ethernet 10/100/1000IP core, writing the required data onto the corresponding register of IP core. The diagram of the data's write-in and the corresponding address register's read-out in the initialization process is shown in Figure 7, we give an example for the register whose address is 0x02.

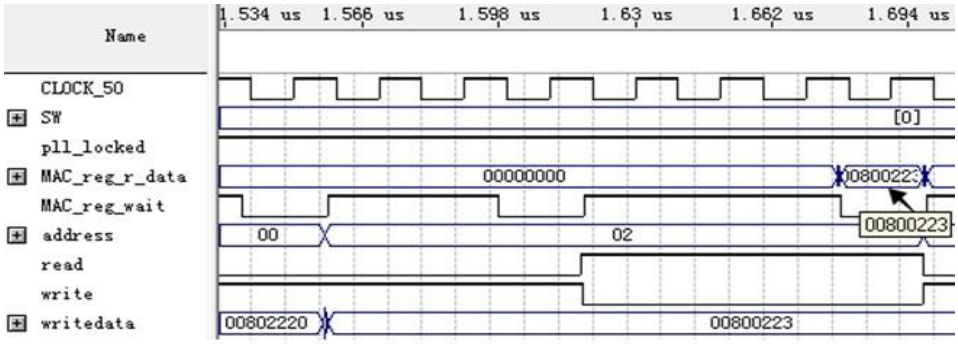

Figure 7. Initialization Test Result

As we can see in Figure 7, the write signal is set to 1 at the beginning, and then we write data into the register whose address is 0x02 data after address becoming 0x02, and the data written into register's data lines becoming 0x00800223. Then we set the write signal to 0, and the read signal to 1, and read the address register, the value read will be displayed on the MAC_reg_r_data signal. The value is consistent with we written at the beginning, so the simulation results show that the initialization process is correct.

3.2. Transmission Data Packets Test

According to the design structure of system, the transmission of data packets can be divided into two steps. The simulation diagram of transmitting data is shown in Figure 8.

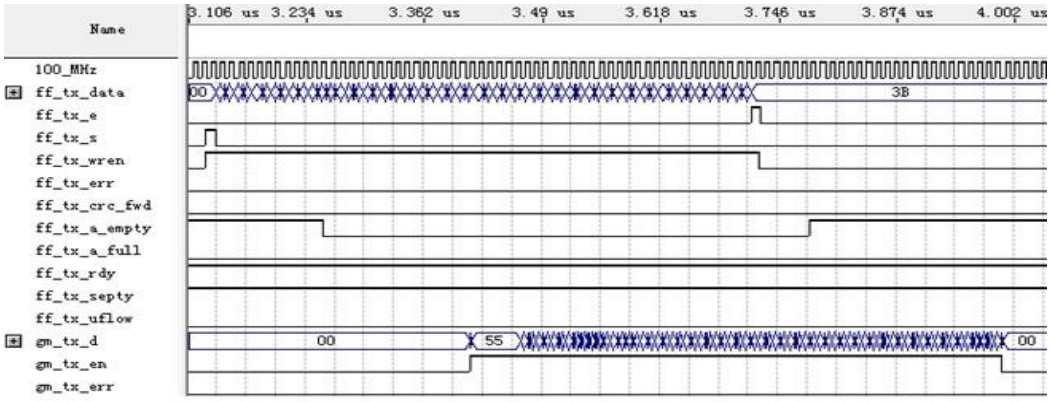

Figure 8. Simulation Diagram of Transmitting Data

As we can see in Figure 8, ff_tx_sand ff_tx_egenerated a pulse respectively at the beginning and the end of the data packets after the data is written into the FIFO sequentially by user, and the ff_tx_wrenwas setto 1 in the whole process of write-in, while other signals (*e.g.*: ff_tx_a_empty, *etc.)* are in normal states.

Before GMII transmitting data, Ethernet 10/100/1000IP core will automatically add

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packet header(7-byte 0x55, 1-byte 0xD5, in total: 8 bytes)for user's data packet, and the IP core will automatically add CRC checksum (4 bytes) of entire packet at the end of packetsto continue to transmit after finishing the transmission of the former packet. The schematic diagrams of adding packet header of the data frames and checksum are shown in Figure 9 and Figure 10 respectively.

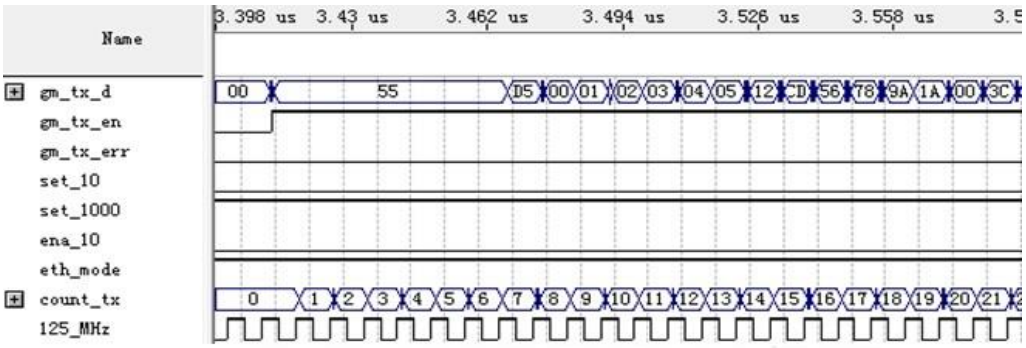

Figure 9. Schematic Diagrams of Adding Packet Header of the Data Frames

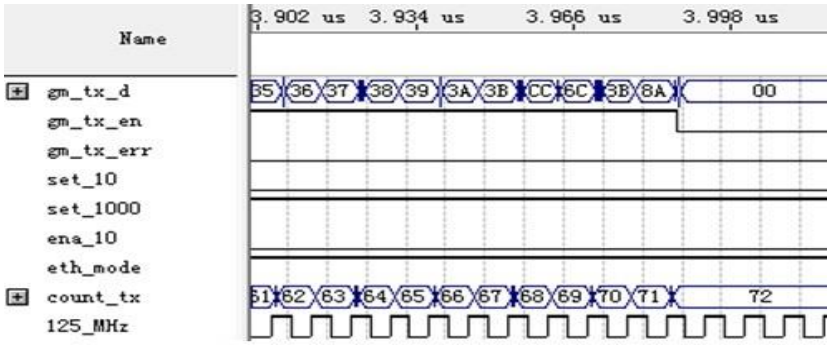

Figure 10. Schematic Diagrams of Adding Checksum

In Figure 10, we can see the clock signal sent by GMII is 125MHz, while in Figure 9, the source MAC fields of transmission data packets have been modified for the local MAC address written in the process of the initialization mentioned above automatically: 12-CD-56-78-9A-1A. The simulation test results above show that the transmitting process of data in our paper is correct.

3.3. Reception Data Packets Test

The reception of data packets are also divided into two steps, the overall simulation diagram of receiving data is shown in Figure 11.

Two steps in Figure 11 can be described as: GMII received data packets, including 8-byte packet header and 4-byte CRC checksum; Then FIFO transferred data to user. While FIFO transmitted data, ff_rx_sop andff_rx_eop generated a pulse respectively at the beginning and the end of the data packets. The packet length field of received data packets was 0x0014 in the process of test, which is 20 bytes, while the minimum length of the packets in data link layer is 60 bytes, so they needed to fill with zero bytes untilff_rx_eop displayed 60 bytes.

The data given was a packet of CRC checksum error in reception data simulation diagram Figure 11, while ff_rx_eop gave an end signal, rx_err gave an error code B000101 of reception error correspondingly, which means CRC error.

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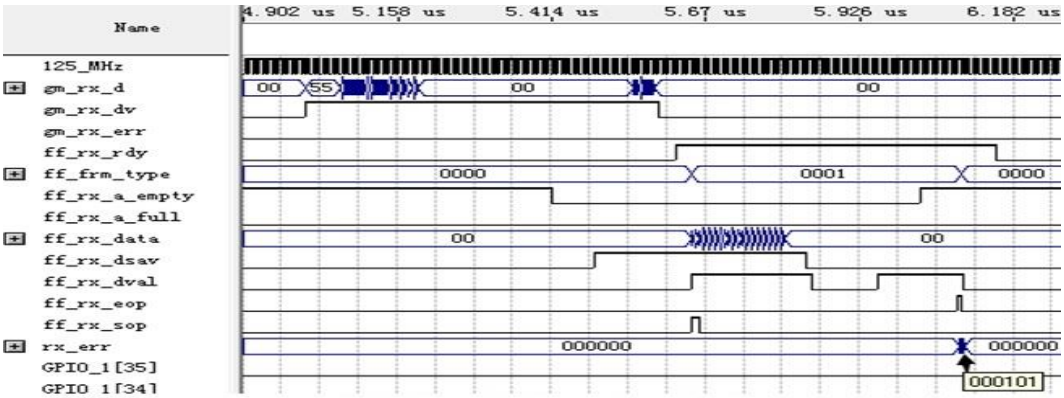

Figure 11. Simulation Diagram of Receiving Data

We compiled through the simulation design built on Quartos II, and got the compilation report of our experiment shown in Figure 12.

Flow Status	Successful
Quartus II Version	8.0 Build 215 05/29/2008 SJ Full Version
Revision Name	tcpip
Top-level Entity Name	topenet_block
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	No
Total logic elements	3,043 / 33,216 (9 %)
Total combinational functions	2,370 / 33,216 (7 %)
Dedicated logic registers	1,971 / 33,216 (6 %)
Total registers	1971
Total pins	237 / 475 (50 %)
Total virtual pins	0
Total memory bits	51,728 / 483,840 (11 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	1 / 4 (25 %)

Figure 12. Compilation Result of our Experiment Built on Quartos II

As can be seen from the compilation results, the development platform of FPGA selected for this experiment is EP2C35F672C6 of DE2, the number of logic gate units this experiment shared is 3043, occupying 9% of total resources; the number of registers used is 1971; the total of RAM consumption is 51728bits, occupying 11% of RAM resources; the number of phase-locked loop is 1. The results compiled are consistent with that of simulation tests, which shows that our system is correct, while the Ethernet data packets transceiver module based on FPGA has a low system occupancy rate, and a high transfer rate compared with existing general system currently.

4. Summary

This paper successfully implemented Ethernet MAC packets transceiver module based on FPGA, and the logic control functions of Ethernet through Ethernet 10/100/1000IP core. The experiment results show that the transceiver module we designed can meet the requirements of high-speed transmission in real-time environmental conditions, and this system takes up less resources. However, there is something need to improve in the process of system design, such as the usage of FPGA resource, and richer functions, which will be our further research contents in future.

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