International Journal of Future Generation Communication and Networking
Vol.7, No.1 (2014), pp.81-88
http://dx.doi.org/10.14257/ijfgcn.2014.7.1.08

Design and Realization of Baseband Signal Downsampling in LTE System

Li-hua Wu[1], Xiu-li Zhang[1] and Yang Yang[1]

[1]*The higher educational key laboratory for Measuring & Control Technology and Instrumentations of Heilongjiang Province, Harbin University of Science and Technology, Harbin 150080, China*
wulihuasc@126.com

Abstract

During the random access process of LTE system, PRACH needs to perform significant amount of computations (e.g. IFFT, FFT) on received signals. Therefore conducting downsampling on received signals is necessary to decrease the complexity of the subsequent signal processing work. Downsampling usually employs a multi-stage filter which consists of a CIC filter, a compensation filter and a half-band filter. This paper introduced a new donwsampling method using a multi-stage half-band filter with three half-band decimation filters. Compared with the traditional one, the new method showed a great increase in computing efficiency. The new filter was designed and a plan of implementing this filter on FPGA was suggested. MATLAB simulation was performed and the simulating results showed that the method proposed in this paper is capable of conducting downsampling on received signals, especially in the random access channel.

Keywords: *Decimation; Half-band filter; Downsampling; FPGA; LTE*

1. Introduction

In LTE-FDD system, the sampling rate is 30.72MHz on transmitter [1]. PRACH receiving process needs to perform significant amount of computations (*e.g.*, IFFT, FFT) on received signals [2], therefore conducting downsampling on received signals is necessary to decrease the complexity of the subsequent signal processing work [3]. Downsampling usually employs a multi-stage filter which consists of a CIC filter, a compensation filter and a half-band filter. How to improve the computational efficiency of the downsampling is what to be solved at present.

2. Determination of LTE System Downsampling Plan

As shown in Figure 1, LTE system consists of two parts, an uplink and a downlink [4], One certain user device can only be scheduled after the unlink transmission time is synchronized. Therefore PRACH plays a key role in uplink wireless access.

ISSN: 2233-7857 IJFGCN

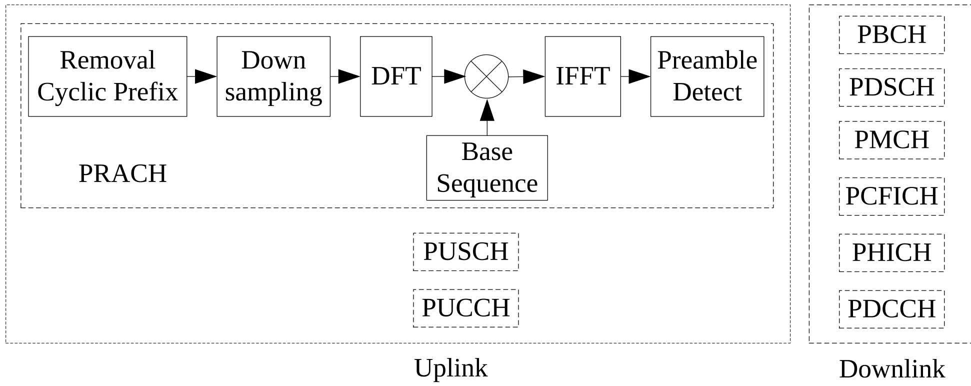


Figure 1. Schematic of PRACH receiver in LTE System

Downsampling plays an important role in the process of receiving PRACH signal [5]. In the premise that no aliasing sampling in the downsampling process occurs, process can greatly reduce the complexity of the any follow up task of signal processing [6]. Since CIC filter requires small bandwidth scale factor which LTE system does not has, it is not applicable in LTE system. Another problem is that CIC filter has a rather large pass-band fluctuation. If using CIC filter in LTE system, a CIC compensation filter would be needed to compensate the pass-band ripple. As a result, both design complexity and system consumption will be increased [7]. On the other hand, half-band filter, due to its unique time domain characteristics (*i.e.*, half its tap coefficients are zero), saves half of the calculation cost compared to other filters during downsampling process. In this way it provides better computational efficiency and real-time performance. Also, PRACH needs to transform its received signal with FFT and IFFT, whose factors are both integer power of 2, while half-band filter is a kind of filter with a decimation factor of 2. With the above consideration, this paper uses half-band filter to realize PRACH signal downsampling.

3. Design of PRACH Downsampling Module

Downsampling module consists of a multi-stage half-band filter in this design. On one hand it can improve the computational efficiency. It can also achieve efficient decimation on the signal.

3.1. Filter Design

3.1.1. Overview of Half-Band Filter: There are many effective methods of designing FIR filters. Half-band filter, a FIR filter based on the principle of decimation and interpolation, is a decimation filter with a decimation factor of 2. Half-band filter's pass-band and stop-band are symmetrical in the Nyquist frequency, so half of the filter coefficients are 0 [8]. These 0 coefficients do not ask for computational consumption in the process, which leads to greatly reduced computation cost in the actual filtering process. Due to its high calculation efficiency and good real time performance, half-band filter becomes particularly important in multi-rate signal processing.

Features of half band filter:

a) Pass-band ripples and stop-band ripples are equal (*i.e.*, $\delta_p = \delta_s$)

b) Pass-band frequency F_p and stop-band frequency F_s are symmetrical about $f_s/4$, (*i.e.*, $F_p+F_s = f_s/2$). For digital frequency it is expressed as: $\omega_p + \omega_s = \pi$[9].

3.1.2. Design Method of Low-pass Filter: Based on the features of the half-band filter, it is especially suitable for realizing decimation or interpolation with $I=2^M$ (where I is multiple of decimation; M is filter series) [10]. At the same time, it has very high computing efficiency and good real-time performance.

Methods such as Equal-ripple and Window may be used for designing half-band filter. Due to the complexity of Equal-ripple method, this paper uses the method of Window.

In the design of half-band filter with Window method [11], an ideal characteristic of half-band filter frequency response $H_d(e^{-j\omega})$ is assumed and its equation is shown as follows:

$$H_d(e^{-j\omega}) = \begin{cases} e^{-j\omega} & |\omega| \le \frac{\pi}{2} \\ 0 & \frac{\pi}{2} < |\omega| < \pi \end{cases} \quad (1)$$

Where $\omega = 2\pi F / f_s$ is digital frequency. So half-band filter time-domain response $h_d(n)$ is:

$$h_d(n) = \frac{1}{2\pi} \int_{-\pi/2}^{\pi/2} e^{-ja\omega} e^{j\omega n} d_\omega = \frac{\sin\left[\frac{\pi}{2}(n-a)\right]}{\pi(n-a)} \quad (2)$$

where $a=(N-1)/2$, N is filter order.

Shift $h_d(n)$ to a to make its range same with the Window function.

The next thing is to choose the proper Window function. Available choices include Rectangular Window, Bentley Window, Hamming Window and the Kaiser Window. In order to satisfy the half-band filter's requirements for F_p, F_s and $\delta_p = \delta_s$, function $h_d(n)$ should be combined with the Kaiser Window. Design steps are listed as follows:

The relative transition zone $\Delta\omega$ can be calculated using the following equation:

$$\Delta\omega = \frac{\omega_s - \omega_p}{2\pi} = \frac{\pi - 2\omega_p}{2\pi} \quad (3)$$

Where ω_s is stop-band digital frequency, ω_p is pass-band digital frequency.

The filter order number N is determined by:

$$N \ge \left\lceil \frac{-20\lg\delta - 7.95}{14.36\Delta\omega} \right\rceil + 1 \qquad N \text{ is odd} \quad (4)$$

Where $\delta = \delta_p = \delta_s$ is pass-band ripple.

The time-domain response $\omega_k(n)$ of Kaiser Window can be calculated using the following equation:

$$\omega_k(n) = \frac{I_0(\beta\sqrt{1-[1-2n/(N-1)]^2})}{I_0(\beta)} \tag{5}$$

Where $I_0(x) = 1 + \sum_{k=1}^{\infty}\left[\frac{(x/2)^k}{k!}\right]^2$ is the first kind zeroth order Modified Bessel function; k is an integer greater than 1, β is an empirical coefficient shown as in the equation below;

$$\beta = \begin{cases} 0.1102(A_s - 8.7) & A_s > 50 \\ 0.5842(A_s - 21)^{0.4} + 0.07886(A_s - 21) & 50 \geq A_s \geq 21 \\ 0 & A_s < 21 \end{cases} \tag{6}$$

Where $A_s = -20\lg\delta$ is the minimum attenuation of stop-band;

The filter coefficients is determined by

$$h(n) = h_d(n)w_k(n) \qquad 0 \leq n \leq N-1 \tag{7}$$

3.2. Design of PRACH Half-band Filter

The decimation factor of the filter must be 8 because when random access signal has a bandwidth of 1.08MHz and system has bandwidth of 20MHz, sampling frequency f_s=30.72MHz.

A half-band filter can only support a two time decimation or interpolation. When I is 2^M, an M-level cascade is needed. Therefore, this paper uses three half-band filters in series to achieve the downsampling process of PRACH signal. After the original signal *x(n)* is processed three times by the half-band filter with decimation factor of 2, the sampling rate drops to 1/8 of the original value. The realization diagram is shown in Figure 2.

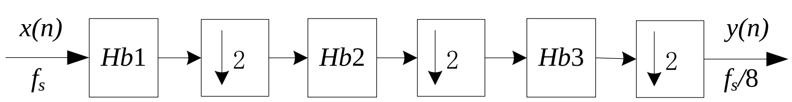


Figure 2. Downsampling Cascading Realization Block Diagram

Since each cascade requires a half-band filter, the order and coefficients of filter of each stage need to be analyzed. As the input decimation rate of each stage filter is different, the cut-off frequency ω_p of each digital filter is different. According to Equation (3), it can be seen that the relative transition bandwidth is changing. Thus the order of filter of each level is different. And in the case of decimation, the order of filter will raise with the increase of series. The following is the analysis of specific values of factors.

According to the previous steps to calculate the value of N, the stop-band attenuation *As* is 60dB.

Pass-band frequency of first level signal F_P=1.08M and the sampling frequency f_s= 30.72MHz, so the digital frequency ω_p = 0.2207. Bring ω_p into the Equation (3) and get the relative transition zone $\Delta\omega$ = 0.4294; As it is known that $A_s = -20\lg\delta$ =60db and value of $\Delta\omega$, it can compute the order N of first filter which is 9 by Equation (4).The order of the various stages can be computed by repeating the above steps. The three stages are 9, 11, 15.

As shown in Table 1, according to the known parameter N, the filter coefficient can be obtained with the analysis of MATLAB software.

Table 1. Half-band Filter Coefficient

half-band filter	filter coefficient
First level filter	-0.0024,-0.0323,0,0.2823,0.5000,0.2823,0, -0.0323, -0.0024,
Second level filter	0.0074,0,-0.0530,0,0.2956,0.5000, 0.2956,0,-0.0530,0,0.0074
Third level filter	-0.0045,0.0088,0.0226,-0.0180, -0.0747,0.0268,0.3066,0.4689,0.3066, 0.0268,-0.0747,-0.0180,0.0226,0.0088, -0.0045

4. PRACH Downsampling Module on FPGA

A downsampling module was designed in Verilog HDL on FPGA, and then implemented under QUARTUSII environment. The module consists of four parts including a delay module, a control module, a storage module and a calculation module. The schematic of the PRACH downsampling module is shown in Figure 3.

The delay module achieves the latch of the input data and delays the input of the signal. The main function of the control module is to produce control signals for delay module and storage module to implement the decimation filtering; Storage module stores the corresponding filter coefficients. It also distributes data, under the control of control module, to the calculation module. The process of downsampling is completed after the calculation module finishes the calculations using the coefficients from the storage module and the input data.

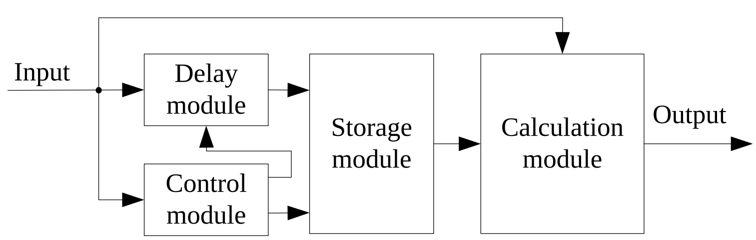
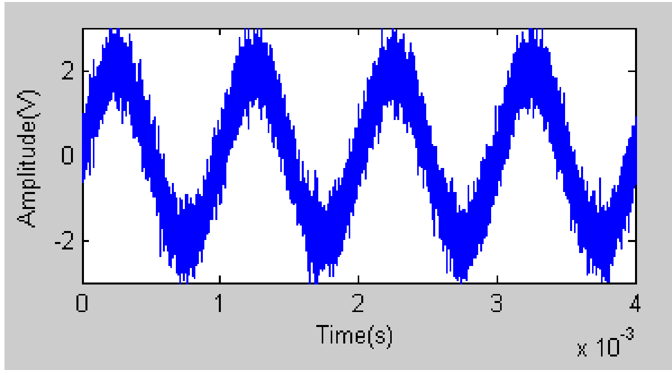
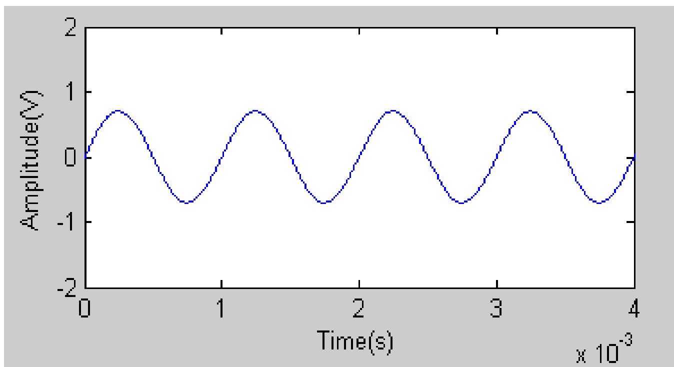


Figure 3. Schematic of PRACH Downsampling Module based on FPGA

MATLAB was used for input signal simulation. The sine signal which has a bandwidth of 10 kHz was superposed with the Gaussian White Noise as shown in Figure 4(a). After FPGA decimation filtering the signal graphics is shown in Figure 4(b). As it can be seen from the figure, output signal realizes the uniform decimation of the input signal, and has filtered out the interference of the noise in the input signal with just small energy attenuation.



(a)The Input Signal with Gaussian White Noise



(b) The output signal by downsampling

Figure 4. Input and Output Signals

It can be seen from the experimental result that the output has realized the effective decimation of the input signal. MATLAB simulation shows that the performance of downsampling method is consistent with the theoretical analysis. As the downsampling filter is implemented as a cascade of three half-band filters and the zero parts of half-band filter coefficient do not need to be computed, therefore it reduces the amount of computation and improves the computational efficiency.

5. Conclusion

Considering the uplink random access channel in LTE system, the paper uses the method of half-band filter cascade which is computationally efficient and can be easily realized to take the signal downsampling. The simulation results of MATLAB and Quartus II show that this design can be applied to the signal downsampling, and it is suitable for the downsampling process of the random access channel.

Acknowledgements

This research was funded by the Scientific and Technological Project of Education Department of Heilongjiang Province with Grant Number (12531113), and Postdoctoral Science-research Developmental Foundation of Heilongjiang province Under Grant Number (LBH-Q12070).

References

[1] L. Milic, “Multi-rate filtering for digital signal processing: MATLAB applications”, New York: IGI Global, **(2009)**.
[2] B. Farhang-Boroujeny and R. Kempter, “Multicarrier communication techniques for spectrum sensing and communication in cognitive radios”, IEEE Communications Magazine, **(2008)**.
[3] J. M. De Haan, N. Gribe and I. Claesson, “Filter Bank Design for Sub-band Adaptive Microphone Arrays”, IEEE Trans. Speech Audio Processing, **(2003)**.
[4] 3GPP R1-063044. Motorola.Non-Synchronized Radom Access Physical Layer Procedure.3GPP TSG RAN WG1 Meeting #47, Japan, **(2006)**.
[5] E. Galija Allpass, “Based Near Perfect Reconstruction Filter Banks”, Ph. D. thesis, Christian-Albrechts University, Kiel, Germany, **(2002)**.
[6] Z. Ying, “Random access preamble based on LTE up links”, WASE International Conference on Information Engineering, **(2009)**.
[7] X-N. Yang, C.-Y. Lou and J.-L. Yu, “Software Radio Principles and Applications”, Electronic Industry, **(2001)**.
[8] S. Sesia, I. Toufik and M. Baker, “LTE: The UMTS Long Term Evolution from Theory to Practice”, London: John Wiley&Sons Ltd., **(2009)**.
[9] W.-L. Tong, “Faster design of IIR digital filter based on FPGA”, Electronic Component Applications, **(2007)**.
[10] A. N. Willson, “Desensitized Half-band Filters”, IEEE Transactions on Circuits and Systems, **(2010)**.
[11] S. Maruyama, “Mobile Terminals Toward LTE and Requirements on Decive Technologies”, IEEE Symposium on VLSI Circuits, **(2007)**.