Line Topology Estimation of Indoor power Lines Using Multipoint Single Ended Loop Testing

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Abstract

Quality of broadband connectivity over a residential power line is dependent on its topology; which is very different from twisted pair copper used in telephony. In this paper methods to estimate the topology of a power line are investigated. A two step procedure comprising of a set of correlation time domain Reflectometry (CTDR) measurements based on Single Ended Loop Testing (SELT) and an initial topology estimate as a first step, followed by a comparison with frequency domain Reflectometry (FDR) measurement as a second step to finally ascertain the power line topology. A set of codes with complementary autocorrelation property is used for probing the line. The number of bridge taps (BTs) in a power line is large and spaced closely; hence multiple applications of CTDR from different sockets are carried out to understand tap positions close to the measuring socket. An analysis of the measurements from multiple CTDR applications is then used to generate a first estimate of the complete power line topology. In the second step a FDR signature of the loop is computed and compared with the frequency domain Reflectometry (FDR) measurement in a mean squared sense to validate the findings. The CTDR and FDR use existing functional blocks of any DSL modem and do not need any additional equipment for measurement. This method is tested for a wide range of power line topologies with multiple bridge taps. The transfer characteristic of the estimated power line loop topology is derived using transmission matrix method and the channel capacity estimated.

Keywords*: Power Line Communication, Digital subscriber line (DSL), Single Ended Loop Testing (SELT), Frequency Domain Reflectometry (FDR), Time Domain Reflectometry (TDR)*

1. Introduction

A power line communication (PLC) system is one in which data is carried on conductors used for the transmission of electric power and have been utilized for low bandwidth application in the past. Though the use of power lines for broadband applications in the home/office environment was proposed to be feasible, it was not fully utilized because of the line noise and hostile channel characteristics [1] for high frequency signal propagation. Transmission Modelling of power line channel is crucial in understanding the quality of data transmission. PLC modeling is done either by top down approach or by using bottom up approach [2]. In top down approach [3] the modeling parameters are determined by measurements and the transfer function is calculated. This is easy to implement and computationally efficient, but is prone to measurement errors [1]. The more versatile bottom up approach treats the network as a composition of many cascaded sections. The parameters of each line section are derived from theoretical concepts [2, 4]. The bottom up approach needs more computational efforts and the network topology is a vital input that has to be ascertained by a loop estimation process.

Network topology can be estimated either by Double Ended Loop Testing (DELT) or by SELT. SELT is far less expensive as the measurement is done from one end only. SELT using TDR [5-9] and FDR [10-12] for telephone lines are well discussed in the literatures. In [5] TDR is implemented by probing the line under test with a pulse. The reflected signal has peaks and the shape of the peak depends on the type of the discontinuity and this is analysed to estimate the loop topology [6, 7]. In [10] the one port scattering parameter is measured and FDR is used to estimate the topology [11, 12]. In these methods measurement is done off line using additional equipment.

However, literature on application of SELT methods for power line topology estimation is scarce. Power lines are different from telephone lines as they are built with thicker conductors, far shorter in lengths, consist of larger number of bridge taps (BTs) and more importantly have assorted variety of bridge tap terminal impedances that are largely inductive and time varying. These terminal impedances are always mismatched with the characteristic impedance of the transmission line.

Application of SELT for a power line environment is investigated in this paper. The SELT estimation process basically contains two phases, a measurement phase and an Interpretation phase. The proposed method aims at using the blocks of existing DSL modem; thus eliminating need of any external equipment for measurement. The measurement phase is completed in two steps; one when CTDR measurements are carried out at different sockets (due to large number of BTs) and a second step when a FDR measurement is performed for the whole Power line loop. Interpretation of measured data is again a twostep procedure that involves computation and can be executed either in the modem itself or offline where more resources are available. The first step in interpretation involves extraction of an approximate loop topology from CTDR measurements and creation of a FDR signature of the CTDR estimated loop. In the second step the computed FDR is compared with the FDR measurement in a mean squared sense to arrive at a most probable estimate of the power line network. Results have been presented for a number of test loops of varying complexity in terms of bridge taps.

The outline of the remaining paper is organized as follows: Section II provides the mathematical model for the received echo signal in time domain which is used to simulate the time domain reflection. Section III deals with the estimation of power line topology using multipoint CTDR. FDR based verification process is presented in Section IV. In section V, results of topology estimation using the proposed method are presented for a variety of loops. The data rate of the network is investigated in section VI along with the capacity estimation for the defined test loops.

2. Mathematical Model for the Received Signal in Time Domain

Junctions are created in power lines due to bridge taps as indicated in Figure 1. Echo will be generated due to every discontinuity. The amount of signal reflected back depends on the reflection coefficient (ρ) [16] and is given by

$$\rho(f) = \frac{Za - Zb}{Za + Zb} \tag{1}$$

Where, *Za* and *Zb* are the frequency dependant characteristic impedances before and after the discontinuity. Similarly the transmission coefficient τ is given by [16]

$$\tau(f) = \frac{2Za}{Za + Zb} \tag{2}$$

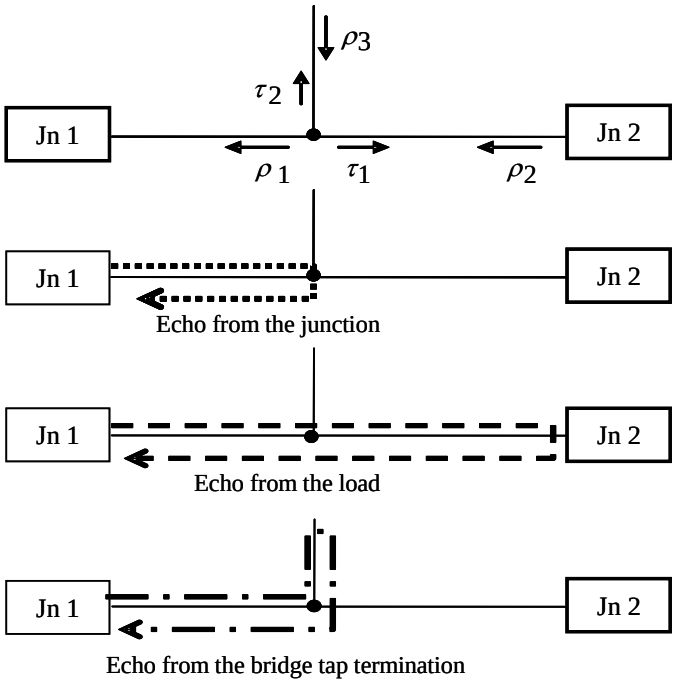


Figure 1. Representation of a Single Tap Loop with Possible Echo Paths

The characteristic impedance is a function of frequency and is given by [19],

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{3}$$

The frequency dependant RLGC parameters are empirically obtained from [17] and used in our computation for deriving the echo transfer function of the power line as,

$$R = \frac{2}{a}\sqrt{\frac{\mu f}{\pi\sigma}} \tag{4}$$

$$L = \frac{\mu}{\pi}\cosh^{-1}\frac{d}{a} + \frac{R}{2\pi f} \tag{5}$$

$$C = \frac{\pi\varepsilon}{\cosh^{-1}\left(\frac{d}{a}\right)} \tag{6}$$

$$G = 2\pi f C \tan\delta \tag{7}$$

Where, 'a' and 'd' are diameter and separation distance of power line conductors respectively, μ and ε are permeability and permittivity in free space and δ is the skin

depth factor. The transmitted signal is a Discrete Multitone signal with 'N' tones conforming to the tone spacing and bandwidths as detailed in the DSL standards [18, 19].

The received echo signal, for a probe signal $p(t)$ is given as

$$r(t) = \sum_{i=1}^{M} E_r^{(i)}(t) \tag{8}$$

Where, $E_r^{(i)}(t)$ is the echo generated by the i[th] discontinuity and M is the total number of discontinuities in the loop. Now

$$E_r^{(i)}(t) = p(t) * h_{echo}^{(i)}(t) \tag{9}$$

where $h_{echo}^{(i)}(t)$ is the impulse response of the i[th] discontinuity. Noting that

$$h_{echo}^{(i)}(t) = F^{-1}(H_{echo}^{(i)}(f)) \tag{10}$$

$H_{echo}^{(i)}(f)$ is the transfer function of the i[th] echo path given by

$$Hecho^{(i)}(f) = F(\tau^{(1)}, \tau^{(2)}, ...\tau^{(i-1)}) H^{(i)}(f) \rho^{(i)}(f) \tag{11}$$

Here $F(\tau^{(1)}, \tau^{(2)}, \cdots \tau^{(i-1)})$ is a frequency dependant function that includes the transmission coefficients of all the discontinuities preceding the i[th] tone and $\rho^{(i)}(f)$ is the reflection coefficient of the i[th] discontinuity. $H^{(i)}(f)$ is the transfer function of the round trip path.

3. Loop Topology Estimation using Correlation Time Domain Reflectometry

In pulse time domain reflectometry, pulse is used as a probe signal and the echo response is collected. The received signal power $r(t)$ for a given probe signal $p(t)$ is expressed as

$$r(t) = k.p(t) * h(t) \qquad (Convolution) \tag{12}$$

Where, $h(t)$ is the impulse response of the echo path, k is the proportionality constant and operator * denotes convolution operation. The received signal strength is proportional to the energy of the probe signal viz; product of peak power of the signal and the pulse width. The peak power has a set limitation to the maximum PSD on the line. So to increase the pulse energy its width has to be increased. This causes the echo to be overlapped with the signal itself causing loss of resolution. High resolution requires that the probe pulse width to be as small as possible. Hence we need to trade resolution with SNR.

Spread spectrum [SS] techniques afford a possibility of providing measurements with improved SNR but without sacrificing response resolution. A spread spectrum signal $p(t)$ used as a probe signal and the received signal $r(t)$ is correlated with the input to obtain the correlated signal $w(t)$.

$$w(t) = p(t) \otimes r(t) = p(t) \otimes (k.p(t) * h(t)) \tag{13}$$

$$w(t) = k.\{(p(t) \otimes p(t)) * h(t)\} \quad (14)$$

Here, $\otimes$ represents correlation operation. If the auto correlation of probe signal is a delta function then the received signal is,

$$w(t) = k.\{(L.\delta(t)) * h(t)\} \quad (15)$$

Where, L is the length of the probe signal. Correlation TDR uses the DMT modulation blocks already available in the line modem along with its tone loading support algorithms. In DMT the available bandwidth is divided into multiple sub channels (bins) and the data is QAM modulated in these bins and transmitted over the channel.

The correlation process with the received echo yields a correlation peak with time shift that is an indication of the line discontinuity. The location of discontinuity (d) is given by [12]

$$d = \frac{v.t_{\max}}{2} \quad (16)$$

Where, v is the velocity of propagation in the twisted pair and $t_{\max}$ is the peak position. Due to the good autocorrelation property of complementary codes, it is used as a probe signal in this paper.

3.1. Use of Complementary Codes in CTDR

Complementary codes are set of codes whose out of phase autocorrelation sums to zero. So the sum of the auto correlation of the two member sequence is a delta function [21].

$$A_k \otimes A_k + B_k \otimes B_k = 2L\delta_k \quad (17)$$

Where, δ_k is the delta function and A_k, B_k are the complementary code pairs of length L. A $2L$ complementary code is generated from its corresponding L element code by appending as shown in equation 18 [21]. Starting with a one element Golay code A=1 and B=1 the higher order Golay codes are derived as

$$\begin{Bmatrix} 1 \\ 1 \end{Bmatrix} \rightarrow \begin{Bmatrix} 1 & 1 \\ 1 & -1 \end{Bmatrix} \rightarrow \begin{Bmatrix} 1 & 1 & 1 & -1 \\ 1 & 1 & -1 & 1 \end{Bmatrix} \quad (18)$$

In this paper we use complementary codes of length $L = 2^K$ with K=13. The choice of K is a compromise between peak value and resolution. Unipolar version of each of the complementary codes (A_{uni}, B_{uni}) [21] and its one's complementary form (A'_{uni}, B'_{uni}) are generated and these four codes are used to probe the line.

The steps involved in using complementary codes for loop topology estimation is shown in Fig.2.

1. Generate complementary codes A_k and B_k.
2. Generate the unipolar version and its one's complemented form for A_k and B_k.

3. For A_{uni}, simulate the reflected signal ($A_{uni} * h(t)$) where, $h(t)$ is the impulse response of the channel.
4. For A'_{uni}, simulate the reflected signal ($A'_{uni} * h(t)$).
5. Obtain the received signal for the sequence A_k, $r^A = A_{uni} * h(t) - A'_{un\ i} * h(t)$
6. Obtain the correlated signal $W^A = r^A \otimes A_k$
7. Repeat steps 3-6 for the second Golay sequence to obtain W^B.
8. Sum $W = W^A + W^B$.

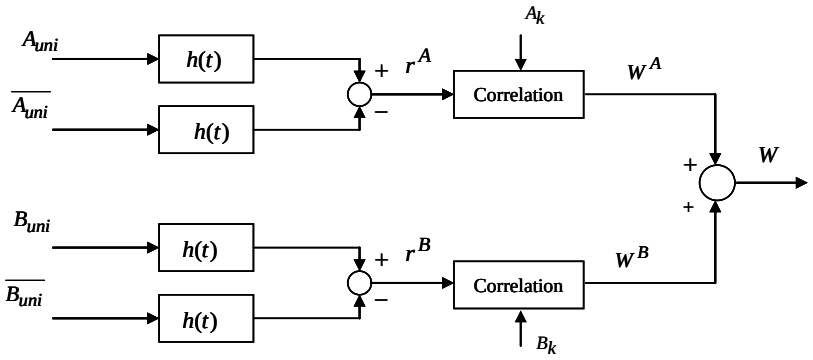


Figure 2. Functional Diagram of Complementary CTDR for Loop Testing

The auto correlation of the Golay code used in our simulation (K=13) is shown in the Figure 3. Ideally the auto correlation of the individual sequences (A_k, B_k) has side lobes but gets cancelled when added together. The peak of added signal will be 2L, where L is the length of the sequence. For a non ideal system finite side lobes will be always present. Fig 3 also shows that at zero phase shifts the peak amplitude doubles and the inner figure shows a decaying out of phase auto correlation of the sum.

From the correlated signal *W*, the locations of the bridge taps are identified using equation 16. Due to the low strength of the received signal from the higher order discontinuities, there is a significant variation in the order of magnitude of the reflections resulting in all the cross correlation peaks being not visible. To a limited amount this problem is overcome using successive decomposition. However when the numbers of bridge taps are more as in the case of typical power lines a better way is to apply CTDR at every socket to know the bridge taps close to that socket. With the repeated applications of CTDR at different sockets we get an overall loop topology. The accuracy of the predicted loop topology at each socket is limited by the length of the probe signal and also due to the variation in the propagation velocity. The topology learning from every socket is then combined suitably (discussed in section V) to arrive at the overall topology.

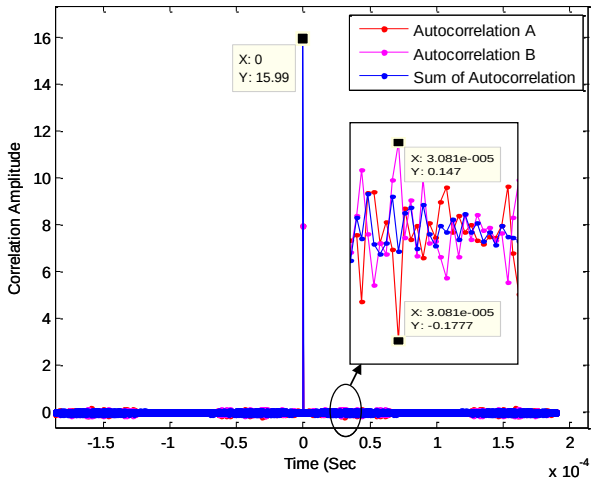


Figure 3. Autocorrelation of the Complementary Codes

4. Verification using Frequency Domain Reflectometry

A The CTDR predicted complete topology is verified by comparing its computed FDR response with a measured target FDR. The total received FDR signal is the sum of the received signal [13] over all the tones and is given by,

$$R(f) = \sum_{n} R(f_n) \tag{19}$$

Where, $R(f_n)$ is the sum of the received signal from all the discontinuities when nth tone is sounded.

$$R(f_n) = \sum_{i=1}^{M} \left(R^{(i)}(f_n) \right) \tag{20}$$

Here $R^{(i)}(f_n)$ is the received signal from the ith echo path when the nth bin is sounded. M is the total number of discontinuities.

CTDR estimated loop Φ is used to generate the FDR data ($R(\Phi, f_n)$) using equation 19. The received signal for Φ is the sum of received signal over all the tones when the line is sounded using DMT with one active tone per symbol. This is compared with the measured FDR data ($\hat{R}(f_n)$) in Mean Square Error (MSE) sense as shown in equation 21.

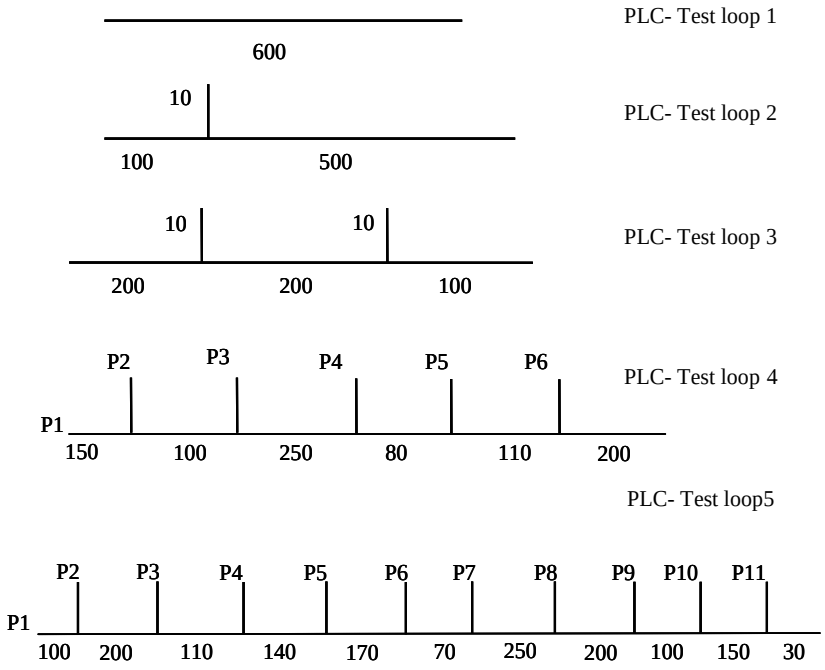
$$MSE = \left(\sum_{n=1}^{N} \left| R(\Phi, fn) - \hat{R}(f_n) \right|^2 \right) \tag{21}$$

A mean square error function optimization methodology is used to find the accurate length in the vicinity of the above predicted topology. This optimization works by comparing the time domain reflected signal of the predicted and actual loop. For FDR measurement and comparison tone numbers 6 -110 are sounded in the DMT with two

bits per tone. This happens to be an upstream standard test signal as generated by central office modems. The lower frequency tones offer lower attenuation and hence better range. The most probable loop topology is estimated by reconstructing Φ till the MSE converges below a set threshold (0.01) limit.

5. Simulation Results and Discussion

Test loops shown in Figure 4 are used to demonstrate the applicability of this method. All the test loops are assumed to be 14 AWG as used for power line. The proposed topology estimation method is tested assuming a -140 dbm/Hz AWGN. The loads at the BT ends correspond to that of a home appliance is found to be typically inductive in nature of about 600 mH. The frequency range employed in SELT for PLC is higher in the order of kHz, and therefore for typical inductances of 600mH the impedances are high enough to be considered as open bridge tap terminations. Tones up to 4000 (17 MHz VDSL2 profile) have been employed for this purpose in CTDR application.



All the lengths are in meters. The length of the bridge tap is 10 meters

Figure 4. PLC Test Loops

Test loop 1 - The variation of correlation amplitude with distance for test loop 1 is shown in Figure 5. Single peak indicates the end of line that in this case is a plain line without any bridge tap. It may be noted that these type of lines are rare in power line network but is considered as a hypothetical test loop for verification of this algorithm. CTDR Predicted line length of 602 m is further improved by the iterative method employing FDR to a final estimate of 599.99m as shown in Figure 6. The converged RMS error between the actual and estimated FDR reflected signal is 0.0077 which confirms the accuracy of prediction.

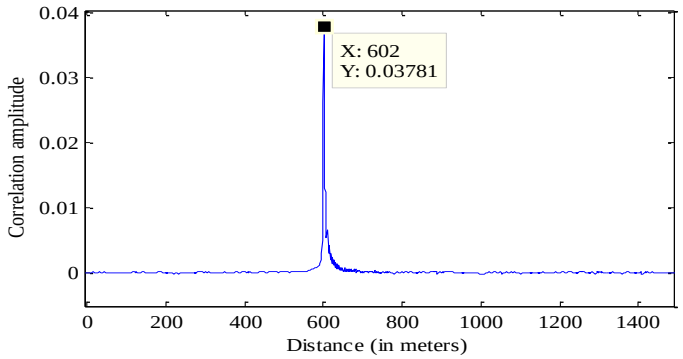


Figure 5. Correlated Signal (CTDR) for Test Loop 1

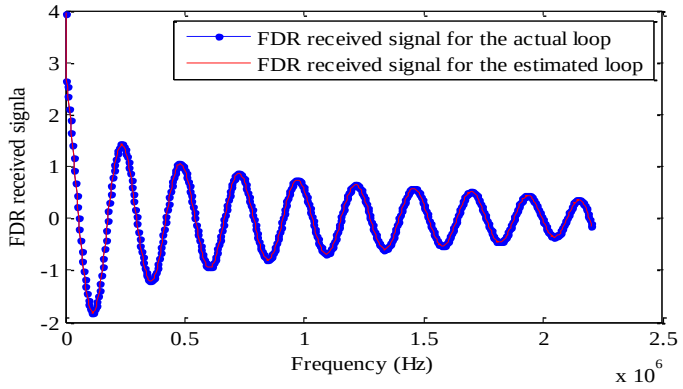


Figure 6. FDR Verification for Test Loop1

Test loops 2 & 3 - As the number of discontinuities are less in the test loops 2 & 3, single point CTDR method has predicted the topology with good accuracy as summarized in Table 2.

Test loops 4 & 5 - For test loops 4 and 5 single point CTDR does not reveal all the discontinuities, as the reflections from the distant discontinuities do not show up clearly on the overall received signal, due to multiple reflections and transmissions from the previous closer discontinuities merging and smearing the desired correlation peaks. Estimation of these discontinuities from a one point CTDR measurement is not possible. So a CTDR - SELT is carried out at all the sockets and the overall loop constructed as described below.

Correlation amplitude variation with distance is plotted for all sockets of test loop 4 in Figure 7 (P1-P6). The accuracy of the distance predicted from the peak position is limited as the propagation factor varies with frequency. Predicted topology after mean square error function optimization methodology, from each socket is tabulated in Table 1. As a convention, the smaller line segment is shown in the left to the point of measurement.

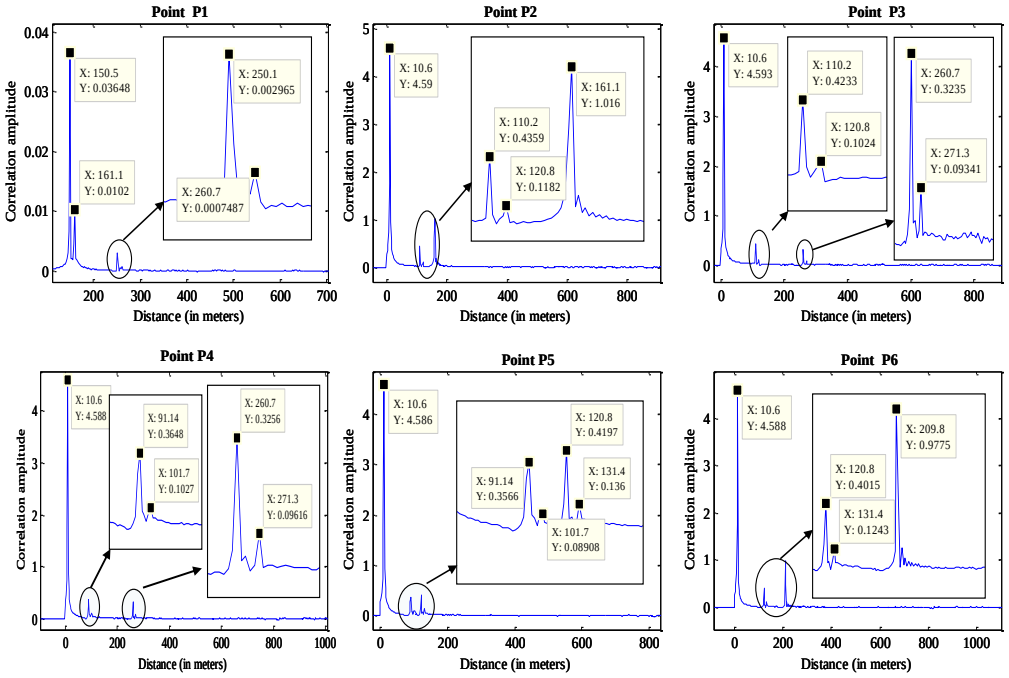
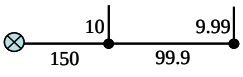
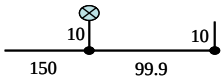
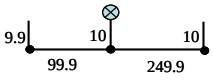
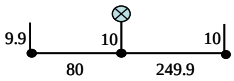
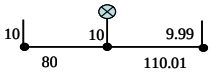
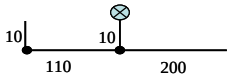


Figure 7.The Cross Correlation Obtained at Different Points of Loop 4 (P1: P6)

Table 1. Estimation Result using CTDR &FDR

Measurement point	Estimated topology(⊗ indicates measurement point)
P1	
P2	
P3	
P4	
P5	
P6	

Estimated line segments from P1 to P6 are analysed to arrive at the construction of the complete loop. Following guidelines are used in this construction.

1. Reflection at the start point will have multiple pairs of peak (from junction and the end of bridge tap).
2. Reflection at the intermediate sockets will have single peak (due to the bridge joint to the main line) followed by pairs of peak.
3. Reflection at the end of the loop will have an additional single peak due to the end of loop in addition to the characteristics of intermediate sockets.
4. At the start point (P1), identified bridge taps are in sequence.
5. At the last socket the end of loop is identified from the reflection coefficient. Reflection from the end of loop will be much higher amplitude as the reflection coefficient of the open end (1) is higher than that of the bridge tap (0.33).
6. For the rest of the points (P2 to P5), estimated segments lengths are verified with the start point and end point predictions to finalize the immediate next segments.

The predicted topology for test loop 4 is shown in Figure 8 and its FDR verification is shown in Figure 9.

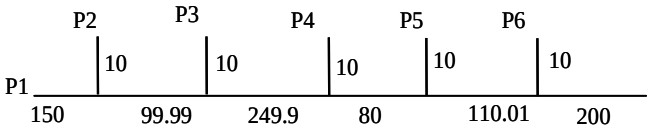


Figure 8. The Predicted Topology for Test Loop 4

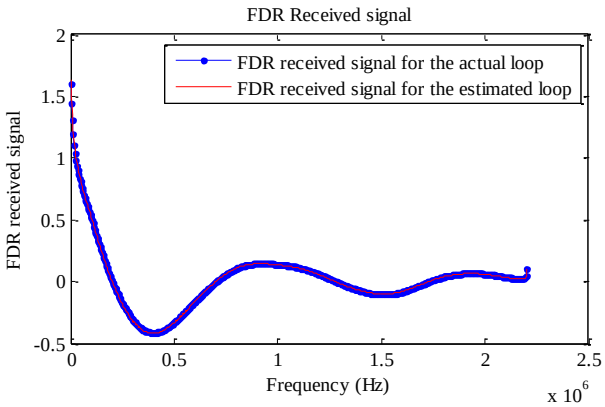


Figure 9. FDR Validation for PLC-test Loop 4

For test loop 5 SELT is applied at points P1-P11 and the similar construction is carried out. The predicted loop topology for all the test loops are tabulated in Table 2. For the test loops 4 & 5, FDR validation is observed to be insensitive to the accuracy of the last few segments. As this FDR validation method depends on the reflected signal from the initial point alone, contribution of the last segments on the total reflection is lesser compared to the initial segments. At each discontinuity, the transmitted signal

strength is reduced to 30% of incident value. This reduction when cumulated at each discontinuity results in too weak an echo and hence becomes insensitive beyond the 3rd tap. It is recommended that if the number of taps is higher than three, every CTDR measurement be followed by FDR measurement based verification for that socket as this would significantly improve the accuracy of estimation. This is easily accomplished since at the time of measurement both CTDR and FDR are performed and echo signals recorded at each socket. The offline analysis can then choose to perform estimation either as a multipoint CTDR and a single point FDR or multipoint CTDR and multipoint FDR verification. The same code can do both tasks.

Table 2. Estimation Result using CTDR &FDR

Test Loop	**Estimated line length (in meters)** (length)* refers to BT	**MSE between the measured and FDR of the predicted Loop**
1	599.99	0.007
2	99.9–(10)*-500	0.0035
3	200–(9.99)*-199.99–(9.99)*-200	0.0015
4	150–(10)*-99.99–(10)*-249.9–(10)*-80–(10)*-110.01– (10)*-200	0.001
5	100-(10)*-199.99-(10)*-110-(10)*-140-(10)*-170-(10)*-70-(10)*-249.9-(10)*-200-(10)*-100-(10)*-150-(10)*-30.	0.002

6. Capacity Estimation

With the loop topology determined, the next step is to ascertain the capacity of the line. From the primary power line parameters, the propagation constant γ is calculated from its RLCG parameters [17] as

$$\gamma = \frac{R}{2}\sqrt{\frac{C}{L}}\left(1-\frac{R^2}{8\omega^2L^2}\right)+j\omega\sqrt{LC}\left(1-\frac{R^2}{8\omega^2L^2}\right) \quad (22)$$

The transmission matrix of a two port network (Fig.10.) gives the relationship between output voltages /current and input voltage/current.

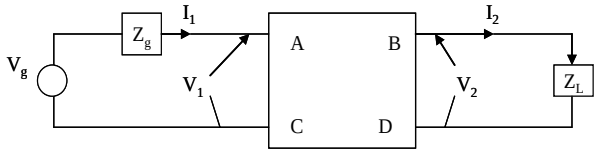


Figure 10. Two-port Model of Power Line

Indoor power line is composed of main propagation path and several distributed branches. Each part has its own transmission matrix and the cascade of these paths gives the overall transmission matrix [11, 16]. The transmission matrix of the main line is calculated as

$$T = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma L) & Z_O \sinh(\gamma L) \\ \frac{\sinh(\gamma L)}{Z_O} & \cosh(\gamma L) \end{bmatrix} \tag{23}$$

Transmission matrix of the cascaded path is given by

$$T_{tap} = ABCD_{tap} = \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_{0,tap} \coth(\gamma L_{tap})} & 1 \end{bmatrix} \tag{24}$$

Overall ABCD matrix is given by

$$T = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = T_1 \times T_2 \times \ldots T_N = \prod_{i=1}^{N} \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} \tag{25}$$

The transfer function of the network is given by

$$H(f) = \frac{V_2}{V_1} = \frac{Z_L}{AZ_L + B} \tag{26}$$

Presence of bridge tap results in a steep dip (null) in the transfer function at a frequency that depends on the length of the tap (d). The phase of the signal reflected from the end of the BT has an effect on the transfer function [22]. The first null occurs at $f_N = Vop/(4 \times d)$, where VoP is velocity of propagation of the signal in the copper medium. The null repeats at odd multiples of f_N. Depth of the null is a strong function of tap length and the number of taps. For smaller length taps, the attenuation of the signal through the tap is less and results in a deeper null depth and consequently increases the propagation loss.

Test loops 1-3 are defined with a constant total length of 600 m and their transfer function are plotted in Figure 11 using the RLCG values given in equation 4 -7. The dips for test loop 2, 3 are at the same location because the bridge tap length is same in both the loops, even though the location of the bridge tap is different. However the depth of the null in loop 3 is more due to the higher number of taps. Transfer function for loop 4 and 5 are shown in Figure 12. As the number of taps increases the null depth also increases.

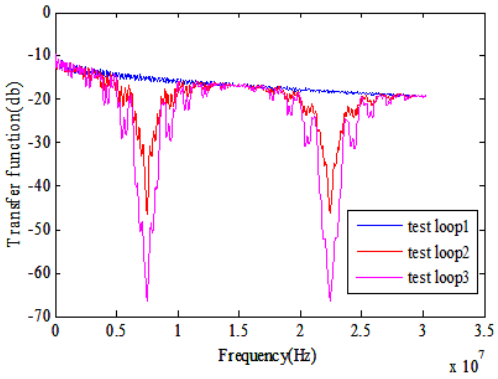


Figure 11. Transfer Function of Test Loops 1-3

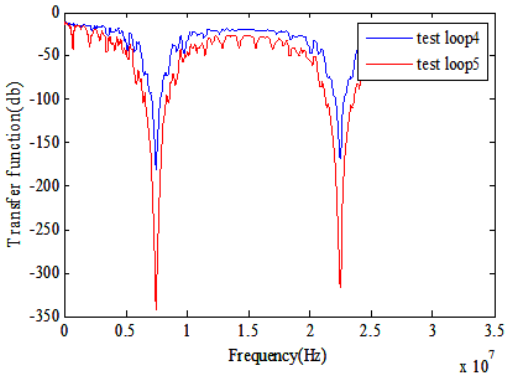


Figure 12. Transfer Function of Test Loops 4-5

SNR which is used to calculate bit rate is derived from the transfer function as [15]

$$SNR_n = \frac{E_n |H(f)|^2}{\sigma_n{}^2} \tag{27}$$

Where, E_n is the energy assigned to nth sub-channel calculated from water-filling algorithm and $\sigma_n{}^2$ is the noise power in nth sub-channel considering an AWGN of -140dbm/Hz. The band plan of VDSL 2 (up to 30 MHz) [18] for upstream and downstream data transmission is used for the data rate calculation. Unlike telephone lines, cross talk noise is not present in the power line as the power lines are not bundled and also has thicker insulation. There is no standard on the limit of power spectral density (PSD mask) defined for power lines, so in this paper the PSD mask of the 'All digital mode' in VDSL2 is assumed, as this helps in comparing the data rate of power lines with VDSL2 over telephone lines. In the computation of data rates in this paper, we do not consider the effect of random impulse noise in power lines which is significant requires a separate study and beyond the scope of the primary objective of this paper viz; loop topology estimation.

The number of bits loaded in each channel is calculated considering the AWGN noise of -140dBm/Hz using [15,20]

$$b_n = \frac{1}{2}\log_2\left(1 + \frac{SNR_n}{\Gamma}\right) \tag{28}$$

Γ is the SNR gap which is a function of probability of symbol error and the line encoding system. For a symbol error probability of 10e-7 the SNR gap is 15.8 db including a margin of 6 db and zero coding gain.

The integer bit loading using equation 26 above for the test loops is calculated. The data rate is easily computed by multiplying the symbol rate (4Ksps) and the sum of bits over all tones. The downstream bit loading profile for test loops 1-3 is shown in Figure 13. Nulls are present in the downstream transmission band of VDSL2 and the effect on the bit loading is clearly visible in this figure. The downstream bit loading profile for test loops 4, 5 is shown in Figure 14. Figures 15 and 16 show the upstream bit profiles for test loops 1-3 and 4-5 respectively. It may be noted that for the first 3 test cases the

total length of the loop is constant but for test case 4 and 5 the total length is different. The summary of the data rate is tabulated in Table 3.

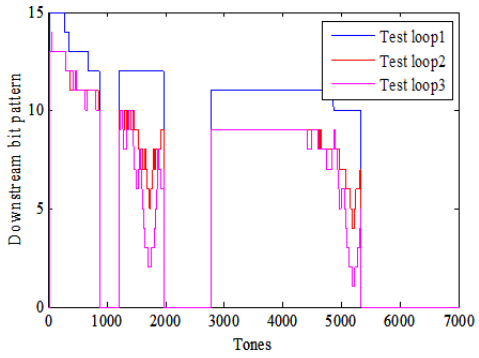


Figure 13. Downstream Bit Profile for Test Loops 1-3

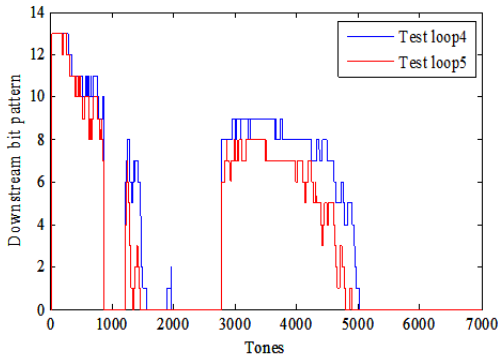


Figure 14. Downstream Bit Profile for Test Loops 4-5

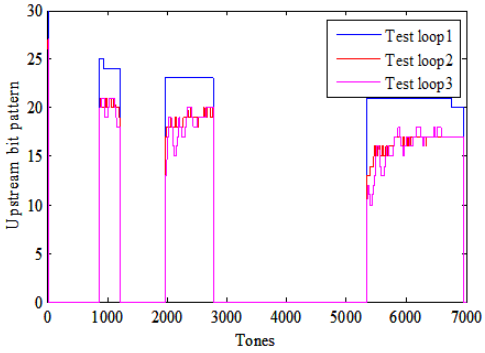


Figure 15. Upstream Bit Profile for Test Loops 1-3

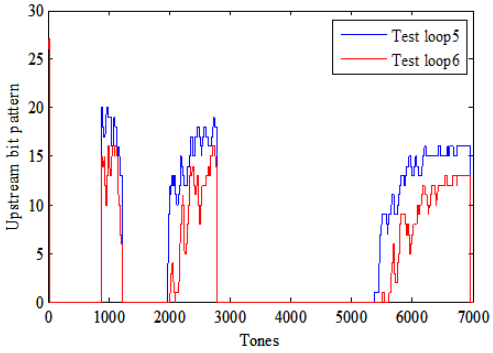


Figure 16. Upstream Bit Profile for Test Loops 4-5

Table 3. Capacity Estimation for Various Loops

Test loop	Downstream capacity (Mbits)	Upstream capacity(Mbps)
1	192.02	246.55
2	150.50	198.08
3	138.78	193.93
4	112.04	156.64
5	89.06	104.3

7. Conclusion

SELT for unravelling the PLC loop topology using CTDR and FDR has been presented. This study indicates that PLC bridge taps being too close to each other, needs CTDR to be utilized multiple times at all the sockets to unravel the loop topology. The predicted individual segments from individual CTDR are combined to form an approximate estimate of the complete topology. This estimate is refined by a MSE optimization employing a computed FDR (of an estimate from CTDR) and an actual FDR measurement. This error function optimization may be done once for the entire loop if the numbers of BTs are less than say three. When the numbers of BTs are more than three, the error function optimization may be performed for each CTDR application, followed by a reconstruction of the entire loop. Finally the data rates of the estimated loops are computed. This SELT tool is easily used by any power line communications equipment provider to advise the residence owner of the rates possible over their power lines. A wider application of this totally non-invasive tool is its ability to detect faults in well concealed power lines laid in industrial plants, submarines and ships. This work could also be extended to include discontinuity due to gauge changes and other types of load impedances at the BT ends.

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