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EFFECT OF VARIATION OF GATE WORK-FUNCTION ON ELECTRICAL CHARACTERISTICS OF LIGHTLY DOPED PMOSFET

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***Abstract*— Miniaturization of the dimensions of Metal Oxide Semiconductor field effect (MOSFET) transistors is very requisite nowadays for the enhanced enactment and integrated circuit compactness but this step of scaling arises to complications such as increased gate resistance and high leakage current. The utilization of integrated circuits in high-performance electronic gadgets is increasing day by day. As more and more complex functions are required in various fields like data/image processing and wired/wireless communication, the need to incorporate these functions in a compact package is also increasing. The reduction of channel length and other reduced parameters blemishes the device performance. The initial design can be designed and virtually fabricated in Computer-aided design (CAD) tool and the complexities of the design can be analysed at the early stage before the actual fabrication is done in fabrication laboratories. The scaling down of device dimensions results in a drastic increase in the sub-threshold leakage current of the device. There are various ways to reduce the leakage current of the device by increasing the work-function of the gate, variation of poly doping; halo doping and threshold implant concentration to reduce the leakage current of the device. To diminish these problems in Nano-scale transistors; there is massive interest in the variation of transistor's gate work-function. The experimental observations show that the devices with high gate work-function material have low leakage current as compared to low gate work-function devices. In this paper, 45nm P-MOSFET is virtually fabricated in ATHENA and simulated in ATLAS SILVACO. The work-function of the gate of PMOS is varied from 5.05eV to 5.32eV to estimate the leakage current of the device. The simulation result shows that the 9.35 nA/μm is achieved at gate work-function of 5.25eV.**

***Keywords*—** PMOS, Athena, Atlas, Silvaco, CAD

1. INTRODUCTION

Down-scaling of feature size of field-effect transistor (FET) has provided a continued enhancement in rapid performance, package density and cost per transistor over the past few decades. While performing scaling, the transistor gate length becomes in Nano-meter

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scale, problems related to MOS gate depletion and bigger gate resistance become more remarkable [1]. The depletion layer of the gate increases the equivalent gate oxide thickness and reduces the gate capacitance in the inversion regime [2]. There is a compromise between device performance due to a lesser inversion charge density and a lesser gate voltage. To reduce the problems of MOS gate depletion and bigger gate resistance, the active dopant density in the Poly gate material must be increased [3]. This can be done by increasing the gate work-function of the poly gate; by using the silicide material over the poly gates; by using the material with high work-function as the gate material [4, 5].

In this paper, work-function of gate material is set at different values to analyse the leakage current of the PMOS device. The MOS gate work-function is a very important consideration in the selection of gate materials for device integration because it directly affects the threshold voltage and performance of a transistor [6]. For bulk MOS transistors, the required gate work-functions for NMOS and PMOS transistors are close to the conduction and valence bands of silicon, respectively, to achieve low and symmetrical threshold voltages for optimal MOS performance [7]. The simulation results show that the raise of work-function of the gate of PMOS, the leakage current in the sub-threshold region of the MOS reduces [8].

2. DESIGN SPECIFICATIONS

By allowing the use of a lightly doped channel, significant benefits such as enhanced mobility and immunity to statistical dopant fluctuation can be achieved. Due to the low depletion charge density, work function engineering is utilized to adjust the performance metrics of the transistor. The operative work function of a gate material in a conductive–dielectric system is typically extracted from the flat-band voltage deduced from the capacitance-voltage characteristics of a metal-dielectric semiconductor capacitor[9].

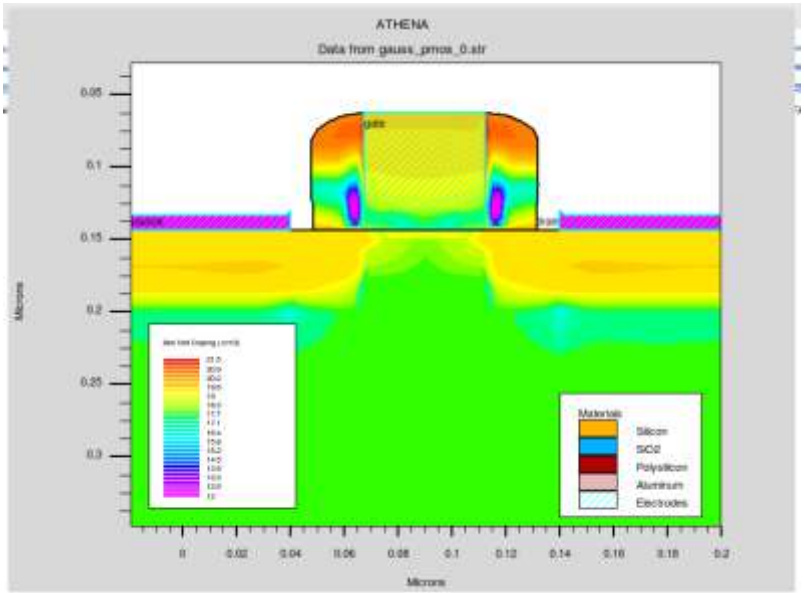

Fig. 1 Device Structure of PMOS in Contour Mode

A 45nm PMOS has been virtually fabricated in ATHENA package of SILVACO tool and simulated to analyze the current-voltage characteristics of the device in ATLAS package of SILVACO software. The fabrication is done by considering the optimum values of threshold implant concentration, halo implant concentration, and source/ drain

doping concentration. The fabricated structure of a 45nm PMOS is shown in Figure 1 above.

The effective gate length of 45nm PMOS is 40nm with an oxide thickness of 1nm. The N-type substrate is considered having 1e15 cm^{-3} concentration and the supply voltage varies from 0.05V to 1.2V.

Table I. Specifications of 45nm P type MOS

Parameters	**Value Assumed**
Effective Gate Length, Lg	40nm
Oxide thickness	1nm
Substrate	1e15 cm^{-3}
Pwell implant	7e13 cm^{-3}
Threshold implant	2e12 cm^{-3}
Halo Implant	4e13 cm^{-3}
S/D doping	1.6e15 cm^{-3}

Table I shown above specifies the parameters considered for the virtual fabrication of P-type device in ATHENA and by altering the concentrations of various parameters with different levels of dose in the ATHENA. ATLAS device simulator is incorporated to extract the current-voltage characteristics of the P-type device [10].

3. OUTPUT CHARACTERISTICS

The output drain current is plotted w.r.t gate voltage at various work-functions. The poly gate work function has been varied from 5.05 to 5.32 eV. The transfer characteristics of PMOSFET have been shown in TONYPLOT of SILVACO in Figure 2 and Figure 3.

During the simulation, the gate voltage, V_G is varied from 0.05V to 1.2V at constant drain voltage to achieve the I_{DS}-V_G curve. Afterward, the extracted parameters such as threshold voltage, ON current, OFF current, sub-threshold slopethe and DIBL has been extracted. To obtain I_DV_{DS} curve, the drain voltage, V_D was set to 0.1V to 1.2V at constant gate voltage. TONYPLOT of SILVACO is used to view the results in a graphical manner.

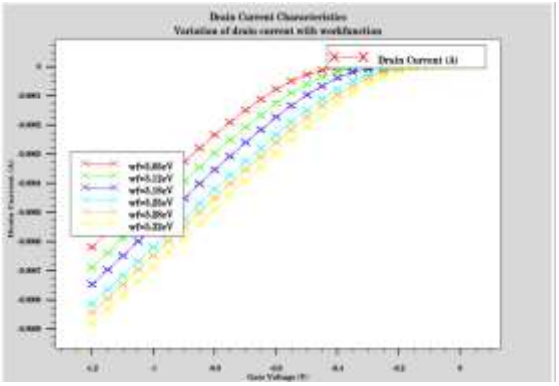

Fig. 2 I_D-V_G Curves in Linear Scale for multiple work-functions

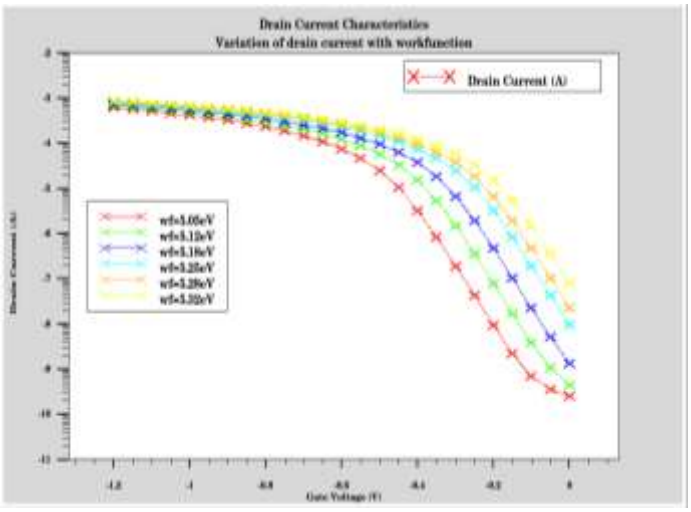

Fig 3 I_D-V_G Curves in Log Scale for multiple work-functions

The sub-threshold characteristics of the device are efficiently improving by enhancing the work-function of the device. This is due to the fact that as the threshold voltage is increased by increasing the work-function, hence the leakage current in sub-threshold state decreases due to the increase of threshold voltage. The high threshold voltage is always required for fewer leakage currents in sub-threshold behavior mode [11].

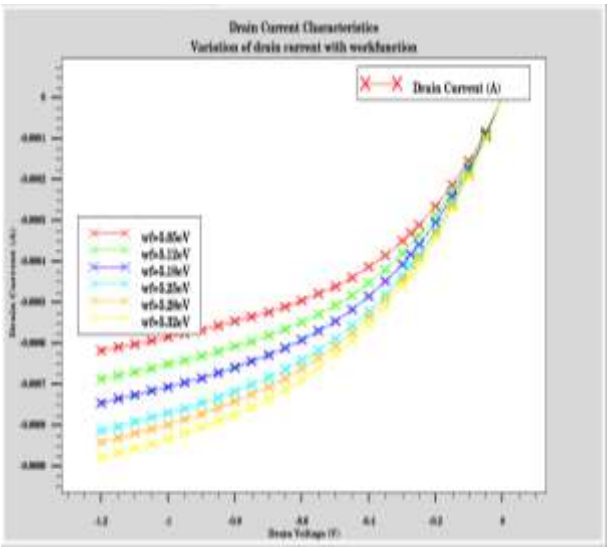

Fig. 4 I_D-V_D Curves for multiple work-functions

Figure 4 shows the deviation of drain current with drain voltage at different transistor's work-functions range. As the transistor's work-function increases, drain current of P-type MOS decreases.

4. INFLUENCE OF GATE WORK-FUNCTION ON VARIOUS PARAMETERS

There are various device and process parameters i.e threshold voltage, gate current, sub-threshold leakage current, drain current, mobility, trans-conductance, conductance, oxide thickness, etc. Among these parameters, the threshold voltage is an important parameter in MOSFETs.

4.1. INFLUENCE OF GATE WORK-FUNCTION ON THRESHOLD VOLTAGE

The threshold voltage is the voltage required to turn on the MOS. It should be not altered in any conditions. Any change in it can alter the performance of the device. [12] It is directly proportional to the flat-band voltage, twice the bulk potential, and the voltage across the gate oxide due to the depletion charge and inversely proportional to the oxide capacitance expressed as in equation 1 below:

$$V_T = V_{FB} - |2\phi_F| - \sqrt{\frac{2\varepsilon_S q N_d (|2\phi_F| - V_{SB})}{C_{OX}}} \quad \ldots\ldots\ldots(1)$$

where, the flat-band voltage, V_{FB}, is given in:

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{OX}} \int_0^{t_{ox}} \frac{x}{x_{ox}} \rho_{ox}(x) dx \quad \ldots\ldots\ldots(2)$$

ϕ_F is the fermi potential, q is the charge of electron, C_{OX} is the oxide capacitance, V_{SB} is the source to bulk potential, N_d is the substrate doping, T_{ox} is the oxide thickness and ρ_{ox} is the charge density. The Fermi energy varies with the doping type and concentration. This gate's work-function is directly proportional to the electron affinity in the semiconductor and the difference between the conduction band energy and the intrinsic energy divided by the electronic charge The changes due to gate work-function is represented by equation 3 below:

$$\phi_{MS} = \phi_M - \phi_S = \phi_M - \left(\chi + \frac{E_g}{2q} - |\phi_F| \right) \quad \ldots\ldots(3)$$

and

$$|\phi_F| = V_t \ln \frac{N_d}{n_i} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4)$$

E_g is the energy band-gap, n_i is intrinsic concentration and χ is the electron affinity. The work-function is the amount of energy required to move from its Fermi level to free space. Due to difficulty defined in modeling, it is very challenging to theoretically predict the work function with accuracy. [13] The threshold voltage for gate work function ranging from 5.05eV to 5.32eV increases in the present simulation study. It has been analyzed that by enhancing the work function of MOSFET, the corresponding threshold voltage of the MOSFET will increase to the desired value. The threshold voltage for a PMOSFET device is negative.

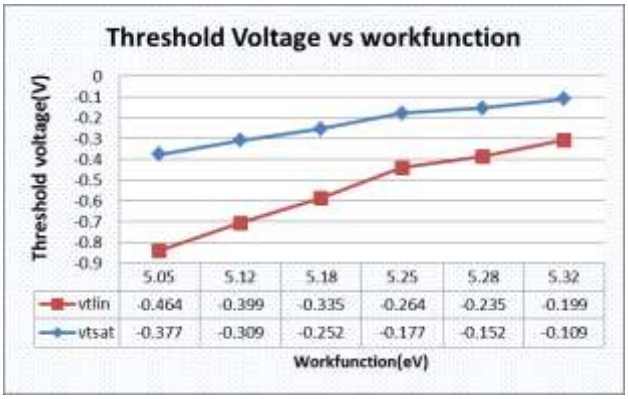

Fig. 5 Threshold voltage Indicative curve

Figure 5 depicts the threshold voltage at two different drain voltages equals to 1.2V and 0.05V, rises with the rise of work-function of the gate of FET.[14] The Poly gate work function addiction of threshold voltage comes out to be linear relation, which can be verified through the equation (1). The result as depicted in this figure has been obtained for a P-type device having L_G =40nm, EOT=1nm and V_{DD}=1.2V maintaining greater threshold voltage is a key requirement for low power devices and hence can be attained more proficiently by enhancing work function the gate material of PMOSFET device.

4.2. INFLUENCE OF TRANSISTOR'S WORK-FUNCTION ON DRAIN CURRENT AND SUB-THRESHOLD CURRENT

Both the drain current and subthreshold current cannot be achieved simultaneously in any device. So to achieve one best value of current among them should be foregone to achieve the best value of another current. The drain current varation of P-type MOSFET is shown as a function of the gate work function in Figure 6.

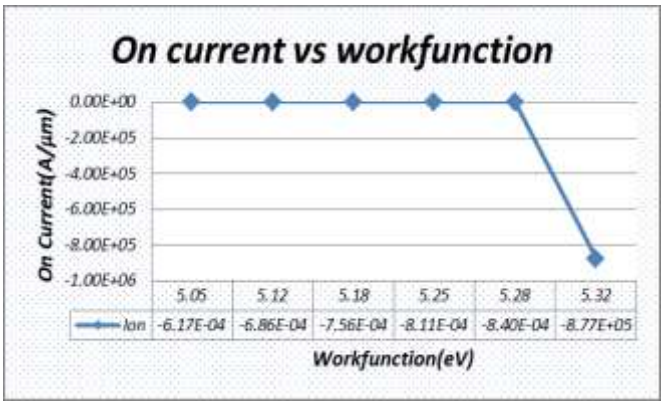

Fig. 6 Drain Current Indicative Curve

Figure 6 indicates the decrease of drain current with gate work-function parameter.

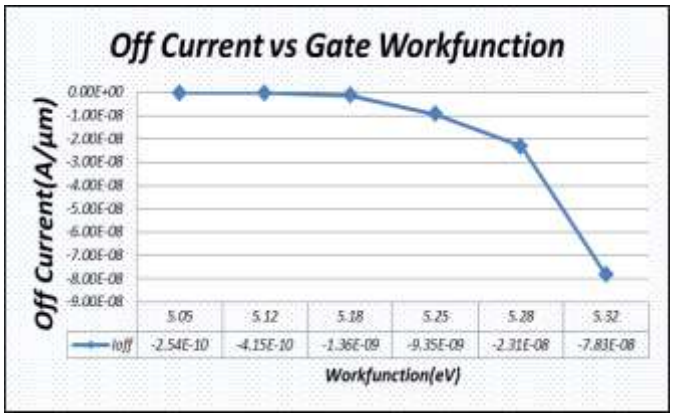

Fig. 7 Leakage Current Indicative Curve

The sub-threshold current characteristics showed that the best value is achieved at 5.25eV gate work-function Figure 7 is showing the variation of sub-threshold current with different work-functions.

4.3. INFLUENCE OF TRANSISTOR'S WORK-FUNCTION ON ON/OFF RATIO

The On/Off ratio of current is the most important parameter to get the best performance device. The On/Off ratio of any MOSFET should be is in the range of e5 to

e6 which can be improved by increasing the work-function range. Different materials are used in the research labs nowadays to get the higher On/Off ratio. The variation of this current ratio with different work-function range is shown below in Figure 8.

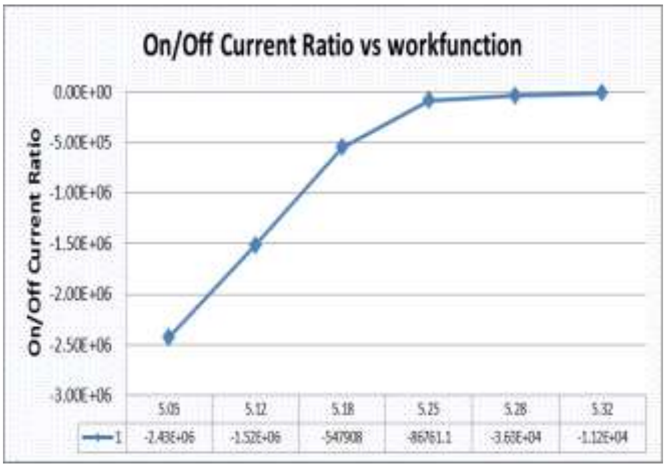

Fig. 8 On/Off Ratio curve

4.4. INFLUENCE OF GATE WORK-FUNCTION ON SS

The lesser sub-threshold slope illustrates the fast switching of the transistor in the sub-threshold region. The sub-threshold region is that region where the leakage current flows due to minority carriers present in the MOS which is not required. But it can be reduced by increasing gate work-function of the P-type device[15]. The drain characteristic in addition to sub-threshold current is given below.

$$I_D \propto \exp\left(\frac{V_{gs}}{n.V_T}\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

where $V_T = \frac{k.T}{q}$ k is the Boltzmann constant, T is the absolute temperature and q is the electron charge.

and $n = 1 + \frac{C_d}{C_m}$

The subthreshold slope is given by:

$$S_t = \left(\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right)^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right).(6)$$

where k is Boltzmann's constant and T is the temperature. The sub-threshold slope can be calculated by the known values of capacitances.

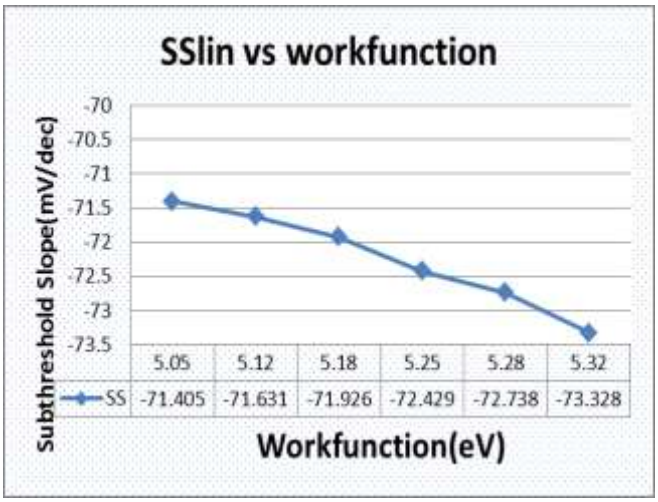

Fig. 9 Sub-threshold Slope Indicative Curve

The above Figure 9 shows that the decreased sub-threshold slope can be achieved with increased gate work-function of p-type MOSFET. The sub-threshold slope is the key parameter to achieve the fast switching and lesser leakage current in the sub-threshold regime.

5. CONCLUSION

The simulation-based analysis in this paper depicts the usefulness of work-function engineering for the regulation of various parameters in Nano-Scale devices. Also, with the increase of the transistor's work-function of the gate electrode, off-state leakage current of the device for lightly doped substrate decreases which is the necessary factor for low power applications. The On/Off current ratio increases and sub-threshold current decreases and sub-threshold behavior is also improved. After the exploration of all prerequisite parameters, it has been observed that by enhancing the threshold voltage, short channel effect decreases off state and the performance of the device increases. The sub-threshold leakage current and Sub-threshold slope are observed as 9.35nA/μm and 72.42mV/decade at a work-function of 5.25eV.

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