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LVCMOS IO Standard Based High Performance RAM Design on 28nm FPGA

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Abstract

In the work the energy efficient and thermal aware single-port RAM has been designed to make it more energy efficient using 28 nm Kintex-7 at ambient temperature of 25 ˚C design tool used is Xilinx 14.2 ISE. Frequency scaling approach has been taken to design energy and power efficient RAM. It is done by scaling frequencies from 50GHz to 200 GHz and calculating the Leakage Power, Quiescent Power as well as the Junction Temperature of Single–Port RAM. Leakage Power has been reduced to the range of 9.411% to 3.52%by Frequency Scaling technique, Quiescent Power Consumption in the range 9.33% to 4.00% and Junction Temperature range from 9.39% to 3.33%, IO Power consumption in range of 45.75% to 15.266% for 50GHz frequency and so on, which makes RAM Design energy efficient and thermal aware.

Keywords: *Single-port RAM in Read-first Mode,Low Power, Optimizing Frequency, Optimizing Voltage, Optimizing Power, FPGA*

1. Introduction

Frequency scaling is done to reduce energy consumption and cooling cost of lightly loaded RAM. The voltage selected (1.2v) is such that stable operation is achieved by the frequency at which the circuit is clocked. It has been concluded that increasing frequency or capacitance increases RAM power demand which in turn increases the temperature. RTL SCHEMATIC i.e. REGISTER TRANSFER LEVEL created after the HDL synthesis phase is as shown

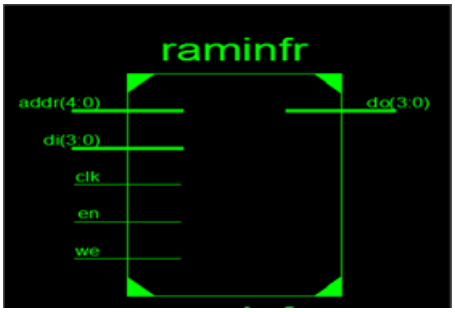

Figure 1. RTL Schematic

It's the pre-optimized design in form of generic symbol. It's basically a circuit abstract which models synchronous digital circuit and is used in verilog (hardware description level) in creating THE HIGH LEVEL circuit representation, from which low level

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representation or even wiring can be derived. This synchronous circuit is consisting of two elements:-

- Registers synchronized circuit's operation to edges, implemented flip flops and the only memory holding device in the circuit.
- Combinational logic consists of logic gates only in the circuit.

Now to attain the foresaid purpose,4 slice registers as flip flops,5 slice LUTs out of which one is used as logic gate and one to obtain OS output only,4 as memory and 4 as single port RAM have been used. With this design, memory is able to work at voltage as low as 0.7 volt, without reducing its performance.

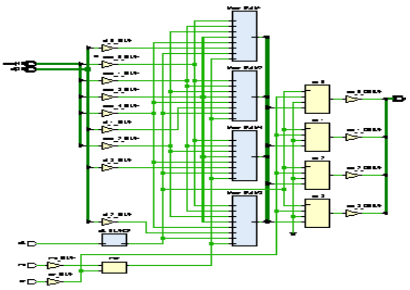


Figure 2. Floor Planning

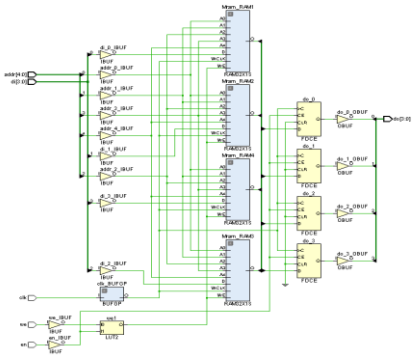


Figure 3. Detailed Structure

In section 2, the literature review is discussed; section 3 includes results of frequency scaling on 28nm Kintex-7 along with the results of optimization of the capacitance scaling over the range of 5 Pico farad to 20 Pico farad. Section 4, includes conclusion and last but not the least section 5 summarizes the future scope of the project.

2. Literature Review

Advancing the technology ranging from 40 nm to 28 nm [1]applies voltage optimization to trim down the dynamic power in both 28nm and 40nm technologies and concluded that 28nm Technology based FPGA is more power effective FPGA in comparison to 40nm technology based FPGA KINTEX7, PGA using IO standards LVCMOS. In [2] capacitance scaling has been designed on the basis of low power ROM design and on varying capacitance, variation in IO power is observed. In [3] Analysis of IO standards at different temperatures is done and several observations are mentioned. In [4] low power and high performance ROM has been designed on FPGA. In [5] a thermal as well as power aware RAM design on FPGA that is IoTs enabled is designed also in [5] author has focused on thermal awareness of RAM by testing its thermal stability at different ambient temperatures In [6] IoTs enable RAM was made to make it energy efficient and observed that using SSTL2_I instead of SSTL_II_DCI there was drastic reduction of 77.73 percent in I/O power at the operating frequency of 3GHz, a small reduction in leakage power i.e. 7.48% is also observed. In [7] lowering of power is done on 28nm FPGA using Xilinx 7. In [8] provides us with systematic trade off between power consumed and test time .The design has reached the level of high performance while simultaneously reducing the power. In [9] author has used Spartan-3, a 90 nm FPGA to assure the power reduction in memory design. In [10] 5 different members of SSTL IO standards family are compared to achieve the most energy efficient among them. In [11] author has used digitally controlled impedance IO standard in memory design to keep a check on power consumption. In this paper Kintex-7 FPGA is used to design high performance RAM so as to make it Energy efficient and thermal aware. Paper [12] is based on the maximum reduction that can be achieved on FPGA and also relates to the low power design of RAM. Paper [13] is basically a low power design based on not

only 90nm of FPGA but also on energy efficient i.e. designed on ultra-scale FPGA. In [14] this book contains the ideas about different gate arrays and their usage in our design. [15] Describes the dependency on different LVMOS standards on the circuit. Now in this work frequency scaling over the range of capacitance from 5 Pico farads to 20 Pico farads is being optimized to get the maximum reduction in Leakage Power, Quiescent Current and Quiescent Power.

3. Results of Frequency Scaling

Based on a 28nm technology Kintex7 is a Field Programmable Gate Array. On the whole Frequency Optimization has been used to observe reduction in effective IO power dissipation and junction temperature of target design. RAM is operated with different frequencies of 50 GHz, 100 GHz and 200GHz.Frequency Scaling optimization results are as follows:

3.1. Operating Frequency is 50 GHz

With 28nm Technology and 50 GHz operating frequency, there is 3.529412%, 7.058824% & 9.411765% reduction in Leakage power, reduction in IO Power 15.26627%, 30.4931% AND 45.75937%. Reduction in Junction Temperature 3.333333%, 6.363636% and 9.393939% when the range of capacitance 5pf-20 pf with step size of 1pf. as shown in Table 1 and Figure 4.

Table 1. Operating Frequency is 50 GHz on 28nm FPG

Capacitance (pf) (C)	Leakage Power (LP)	Quiescent Current (QC)	Quiescent Power (QP)
5	0.077	0.044	0.068
10	0.079	0.046	0.07
15	0.082	0.048	0.072
20	0.085	0.05	0.075

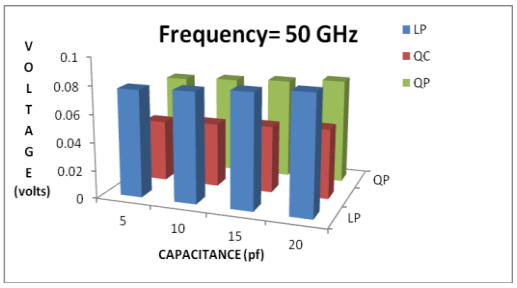


Figure 4. Power and Junction Temperature at Frequency 50 GHz

3.2. Operating Frequency is 100 GHz

When 100 GHz is operating frequency and FPGA is 28nm there is 6.481%, 12.0374%, 17.592% reduction in leakage power, 15.24%, 30.49%, 45.759% reduction in IO power 5.147%, 10.29%, 15.442% is reduction observed in junction temperature in range of 20 pf - 5 pf capacitance with subsequent increase of 1pf. as in Table:2 and Figure 5.

Table 2. Operating Frequency is 100 GHz on 28nm FPG

Capacitance (pf) (C)	Leakage Power (LP)	Quiescent Current (QC)	Quiescent Power (QP)
5	0.089	0.053	0.078
10	0.059	0.058	0.083
15	0.101	0.063	0.089
20	0.108	0.069	0.095

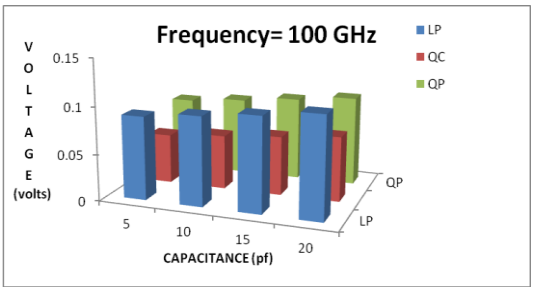


Figure 5. Power and Junction Temperature at Frequency 100GHz

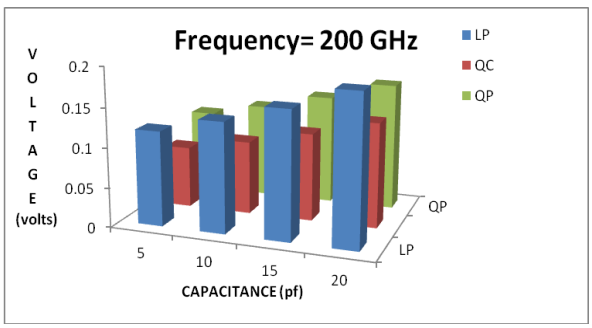
3.3. Operating Frequency of 200 GHz

On 200 GHz operating frequency and 28nm FPGA, there is 14.361%, 26.063%, 36.170% reduction in leakage power, 15.254%, 30.5098%, 45.764% reduction in IO power, 7.433%, 14.867%, 22.300%, is the reduction observed in junction temperature in range of 20-5pf capacitance with subsequent increase of 1pf as shown in Table 3 and Figure 6.

Table 3. Operating Frequency is 200 GHz on 28nm FPGA

Capacitance (pf) (C)	Leakage Power (LP)	Quiescent Current (QC)	Quiescent Power (QP)
5	0.12	0.078	0.105
10	0.139	0.093	0.12
15	0.161	0.111	0.139
20	0.188	0.132	0.161

Figure 6. Power and Junction Temperature at Frequency 200GHz



3.4. Optimizing the Junction Temperature

While scaling the frequency from 50 GHz to 200GHz and optimizing the junction temperature at different capacitances i.e. over a range of 5 Pico farad to 20 Pico farad it's observed that junction temperature increases with increase in frequency from 50 GHz to 200 GHz and also along with increase in capacitance at the same frequency junction temperature increases. Its figure has been observed to follow the characteristics as shown in Figure 7 with increase in capacitance and frequency

Table 4. Junction Temperature for Frequency Ranging From 50 to 200 Ghz

Junction Temperature			
	50	100	200
5	29.9	34.5	43.9
10	30.9	36.6	48.1
15	31.9	38.7	52.3
20	33	40.8	56.5

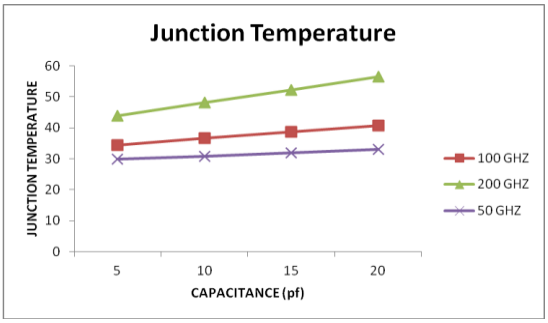


Figure 7. Junction Temperature at Different Capacitances

3.5. Optimizing the IO Power

While scaling the frequency from 50 GHz to 200GHz and optimizing the IO temperature at different capacitances i.e. over a range of 5 to 20 Pico farad it's observed that junction temperature increases with increase in frequency from 50 GHz to 200 GHz and also along with increase in capacitance at the same frequency junction temperature increases. Its figure follows the characteristics as shown in figure 8 with increase in capacitance and frequency.

Table 5. IO Power for Frequency Ranging from 50 to 200 GHz

IO power			
C	50 GHz	100 GHz	200 GHz
5	1.375	2.75	5.5
10	1.762	3.524	7.047
15	2.148	4.297	8.594
20	2.535	5.07	10.141

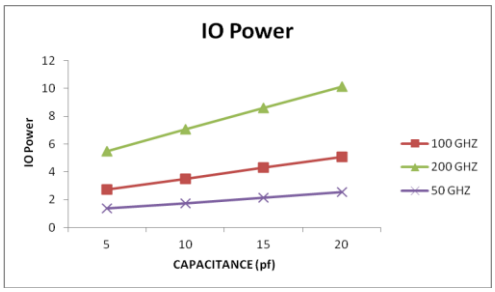


Figure 8. IO Power at Different Capacitances

4. Conclusion

28nm Technology based FPGA is power and energy efficient FPGA. With Frequency scaling, at the frequency of 50GHz and capacitance decreasing from 20-5 pf the maximum reduction is 9.411765% in Leakage power, 45.75937% in IO power and 9.393939% in junction temperature. With Frequency Scaling at 100 GHz the maximum reduction is 17.592% in leakage power, 45.759% in IO power and 15.442% in junction temperature and capacitance decreasing from 20-5 pf. With Frequency scaling, at the frequency of 200 GHz and capacitance decreasing from 20-5 pf the maximum reduction is 36.170% reduction in leakage power, 45.764% reduction in IO power and 22.300%, reduction in junction temperature. In a special optimization of junction temperature and IO power it has been inferred that junction temperature as well as IO power has increased at a range of frequencies of 50 GHz to 200 GHz and with increase in capacitance over the range of 5 pf to 200 pf.

5. Future Scope

There is a great scope in future to implement 16nm FPGA, IOT enable memory and not only can this be used in ICs but also it can be made more and more energy efficient in future. These details and observations can be used in future studies for implementing or formulating more and more results for higher technology.

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