International Journal of Control and Automation
Vol. 9, No. 9 (2016), pp.151-162
http//dx.doi.org/10.14257/ijca.2016.9.9.15

High Performance Energy Efficient Different Counters Design and Implementation on 28nm FPGA

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Abstract

In this paper, we have done analysis of ten different counters in term of frequency related to high performance and power dissipation related to energy efficiency. Conserving energy is now a days a very important aspect. In order to conserve energy consumption of our design, we are using dynamic frequency scaling with default LVCMOS18 IO Standard technique which plays a very important role in power saving. Our design is capable to operate with 1 THz frequency that deliver high performance in less time i.e. 1 pico second. Among 10 different counters, 8 bit simple up counter provide maximum reduction in total power that is 84.25% and 98.33% between a frequency range of 1GHz to 10GHz and 1 GHz to 100 GHz respectively.

Keywords*: Counter, Enable, Load, Reset, Energy Efficient, Gray, LFSR, One Hot, Divide by N Counter, Operating Frequency, FPGA*

1. Introduction

For making any device energy efficient [1-2], it is important that we should minimize power consumption of that device. By doing so, we not only save our money but also we are conserving energy for future use. There are different types of power dissipation as shown in Figure 1 such as clock power, logic power, signal power, IO power and leakage power. Counters can be both synchronous and asynchronous. In synchronous counters, the clock provide will be same and in asynchronous counters, the clock provided will be different. Power consumed by input and output terminals is the IO power. Power consumed by internal signal of counter is the signal power and the power consumed by operating the logic of any counter is the logic power. When charged capacitor connected to transistor used in counters losses energy is called the leakage power. In this paper we had done analysis of 10 different counters at different frequencies and observed the power reduction at different frequencies ranges between 1GHz-10GHz and 1GHz-100GHz. System is designed using FPGAs which are semiconductor devices that can be reprogrammed according to requirements of user [3]. FPGA [2, 4-5] consists of configurable logic blocks known as CLBs which are connected via interconnects that are programmable.

ISSN: 2005-4297 IJCA

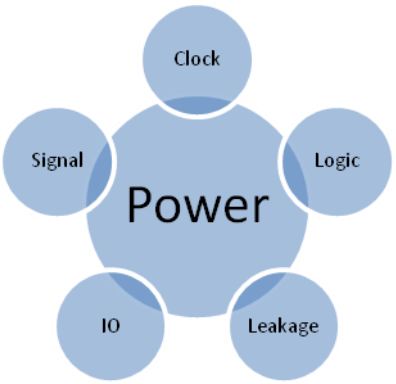

Figure 1. Power Dissipation

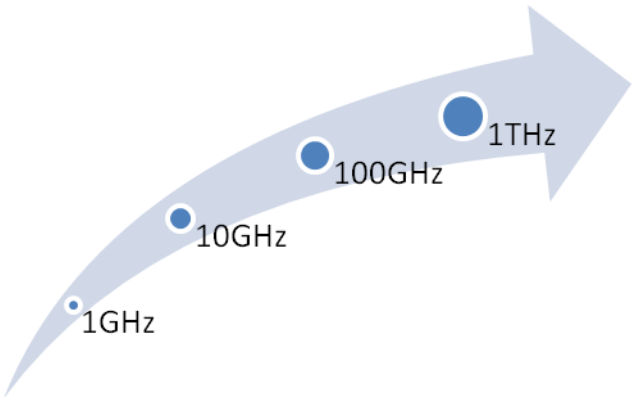

Figure 2. Frequency Dissipation

2. Schematics of Different Counters

A. 8-bit Simple up Counter

8 bit Up Counters are synchronous and presettable counters used in high-speed counting applications. Synchronous operation is done by having all flip-flops clocked simultaneously. These counters are fully programmable and can be preset to any number between 0 to 255 as shown in Figure 3.

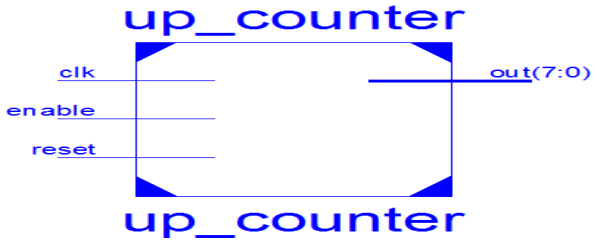

Figure 3. Simple Up Counter

B. Up Counter with Load

8 bit up counter with load is also a synchronous counter in which load pin is used to load the data from the input and enable pin is used to enable the data. After loading the data, data from the input delivered to the flip-flop and counter further processed and gives the output. The output can be seen from the out pin as shown in Figure 4.

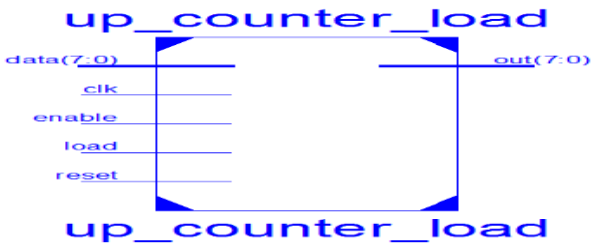

Figure 4. Up Counter with Load

C. Up Down Counter

Up down counter is a synchronous counter. Up down pin counts up when provided high input and counts down when provided low input. Reset pin is used for resetting the current value to initial value as shown in Figure 5. Up down modes have the same priority list and only one can be use at the same time.

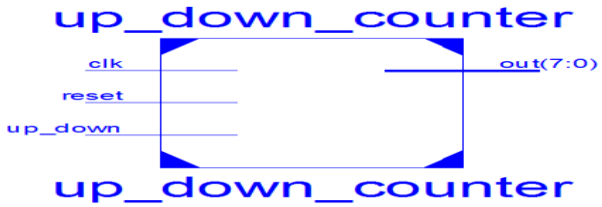

Figure 5. Up Down Counter

D. LFSR

Linear feedback shift register (LFSR) is a shift register in which there is a linear function between input bit and its previous state. LFSR counters operate at higher clock rate and have simple feedback logic. LFSR should not enter all zeros state as shown in Figure 6.

Figure 6. LFSR

E. LFSR Up Down

LFSR is a special kind of counter in which random sequence of counting takes place. LFSR up counter uses XOR gate and does not have all zero states where as LFSR down counter uses XNOR gate and does not have all ones states.

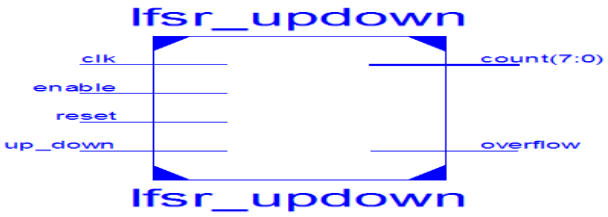

Figure 7. LFSR Up Down

F. Gray Counter

In gray code there is a difference of one bit between two successive values and it is a binary numeral system. Gray counters are used to detect errors in digital communication like in tv.

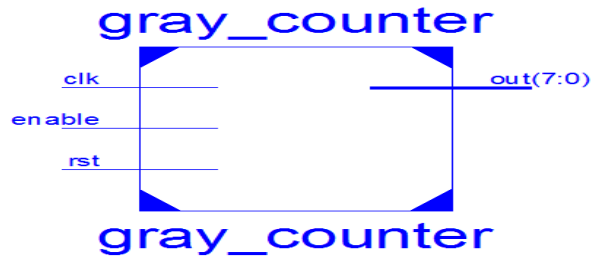

Figure 8. Gray Counter

G. One Hot Counter

One hot counter helps the state machine to run at a faster clock rate. Unlike Gray counter one hot counter does not require a decoder because when nth bit is high only then the state machine is in the nth state. Moreover one hot counter is easy to design and also helps in detection of illegal states.

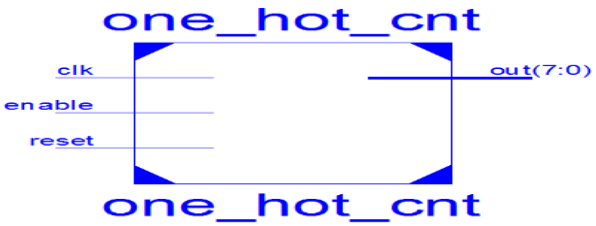

Figure 9. One Hot Counter

H. Divide By 2 Counter

In Divide by N counter, ratio between output signal and input frequency is 1:N. Here N is 2. Therefore output we get is the half of the input, that is, input divided by 2.

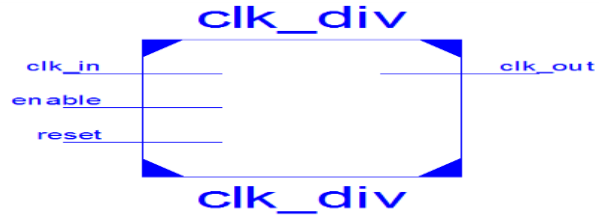

Figure 10. Divide By 2 Counter

I. Divide By 3 Counter

Divide by 3 counter can also be called as clock divider as in this output frequency will be one third of input frequency. e.g. If input frequency is 60 GHz then output frequency is 20 GHz.

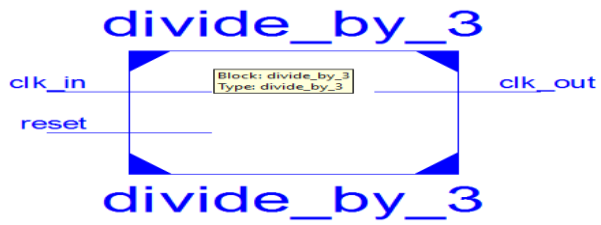

Figure 11. Divide By 3 Counter

J. Divide By 4.5 Counter

Divide by 4.5 counter can also be called as clock divider as in this output frequency will be one third of input frequency. e.g. If input frequency is 50 GHz then output frequency is 11.11 GHz.

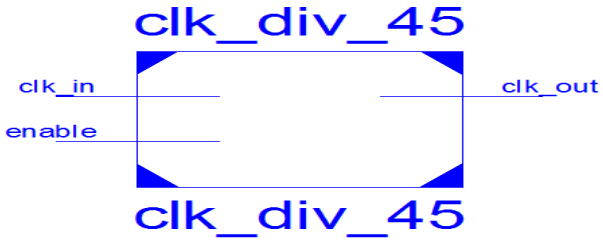

Figure 12. Divide By 4.5 Counter

2. Related Work

Mapping is energy efficient technique used in energy efficient counter design on FPGA [1]. There is only one counter discussed in [1]. Whereas, we are working on ten different counters. Mobile DDR IO standard is used in energy efficient design of ALU [2]. We are using frequency scaling for low power counter design. They have used techniques on Xilinx XC2V3000FPGA [3] while we have used Artix7.

3. Results

A. 8-bit Simple Up Counter

Table 1. Power Dissipation of 8-bit Simple Up Counter

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.001	0.056	0.043	0.105
10GHz	0.051	0.001	0.008	0.562	0.044	0.667
100GHz	0.513	0.012	0.077	5.623	0.066	6.291
1THz	5.136	0.115	0.767	56.234	0.773	63.020

If we use 8-bit simple up counter at frequency of 1GHz instead of 10GHz, 100GHz then total power reduction will be 84.25%, 98.33 % respectively and change in IO power will be 90.03%, 99% respectively and leakage power variation will be 2.27%, 34.84% as shown in Table 1 and Figure 13.

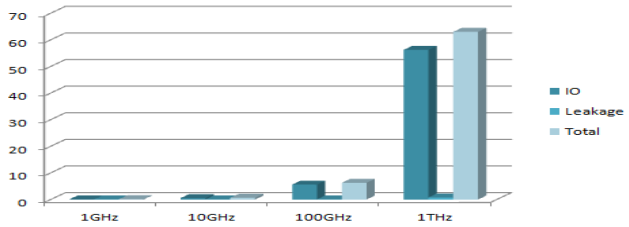

Figure 13. 8bit Simple Up Counter

B. Up Counter with Load

Table 2. Power Dissipation of Up Counter with Load

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.001	0.022	0.042	0.071
10GHz	0.050	0.002	0.007	0.221	0.043	0.323
100GHz	0.500	0.007	0.071	2.208	0.051	2.837
1THz	5.005	0.054	0.705	22.079	0.654	28.498

If we use Up Counter with load at the frequency of 1GHz instead of 10GHz, 100GHz then total power reduction will be 78.01% , 97.49% respectively and change in IO power will be 90.04%, 99% respectively and leakage power variation will be 2.32%, 17.64% as shown in Table 2 and Figure 14.

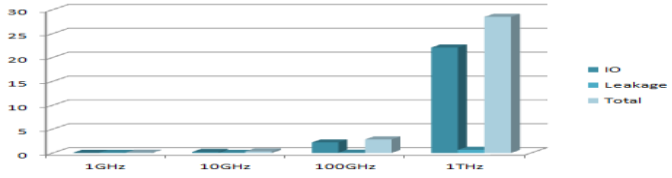

Figure 14. Up Counter with Load

C. Up Down Counter

Table 3. Power Dissipation of Up Down Counter

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.005	0.001	0.001	0.047	0.043	0.095
10GHz	0.051	0.002	0.008	0.465	0.004	0.571
100GHz	0.513	0.013	0.079	4.653	0.061	5.320
1THz	5.133	0.124	0.794	46.529	0.773	53.353

If we use Up Down Counter at the frequency of 1GHz instead of 10GHz, 100GHz then power reduction will be 83.36%, 98.21% respectively and change in IO power will be 89.89%, 98.98% respectively and leakage power variation will be 2.27%, 29.50% as shown in Table 3 and Figure 15.

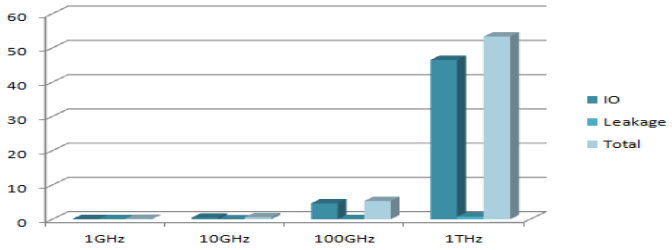

Figure 15. Up Down Counter

D.LFSR

Table 4. Power Dissipation of LFSR

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.001	0.055	0.043	0.103
10GHz	0.051	0.001	0.008	0.547	0.044	0.651
100GHz	0.513	0.005	0.083	5.469	0.065	6.136
1THz	5.130	0.046	0.830	54.695	0.773	61.474

If we use LFSR at the frequency of 1GHz instead of 10GHz, 100GHz then power reduction will be 84.17% ,98.32% respectively and change in IO power will be 89.94%, 98.99% respectively and leakage power variation will be 2.27%, 33.84% as shown in Table 4 and Figure 16.

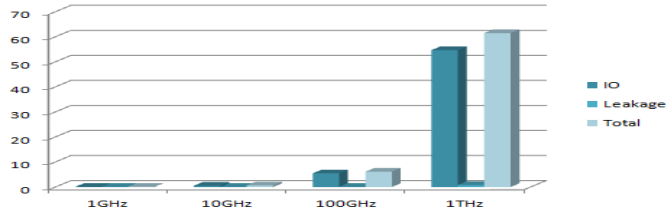

Figure 16. LFSR

E. LFSR Up Down

Table 5. Power Dissipation of LFSR Up Down Counter

Freq	Clock	Logic	Signal	IO	Leakage	Total
: 1GHz	0.006	0.001	0.001	0.054	0.043	0.104
10GHz	0.056	0.002	0.009	0.545	0.044	0.656
100GHz	0.560	0.011	0.093	5.449	0.066	6.180
1THz	5.603	0.099	0.928	54.493	0.773	61.896

If we use LFSR Up Down at the frequency of 1GHz instead of 10GHz, 100GHz then power reduction will be 84.14%, 98.31% respectively and change in IO power will be 90.09%, 99% respectively and leakage power variation will be 2.27%, 34.84% as shown in Table 5 and Figure 17.

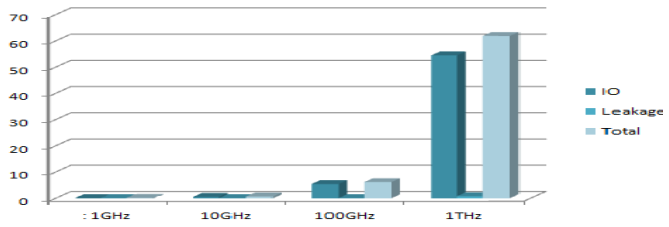

Figure 17. LFSR Up Down Counter

F. Gray Counter

Table 6. Power Dissipation of Gray Counter

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.001	0.047	0.043	0.096
10GHz	0.051	0.002	0.004	0.469	0.044	0.570
100GHz	0.513	0.025	0.028	4.686	0.061	5.303
1THz	5.130	0.140	0.260	46.855	0.773	53.160

If we use Gray Counter at the frequency of 1GHz instead of 10GHz, 100GHz then power reduction will be 83.15%, 98.18% respectively and change in IO power will be 89.97%, 98.99% respectively and leakage power variation will be 2.27%, 29.50% as shown in Table 6 and Figure 18.

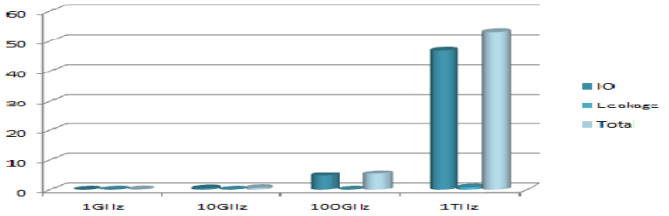

Figure 18. Gray Counter

G. One Hot Counter

Table 7. Power Dissipation of One Hot Counter

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.001	0.033	0.042	0.081
10GHz	0.051	0.000	0.005	0.330	0.043	0.430
100GHz	0.513	0.003	0.050	3.299	0.055	3.919
1THz	5.130	0.026	0.499	32.988	0.773	39.417

If we use One Hot Counter with at the frequency of 1GHz instead of 10GHz, 100GHz then power reduction will be 81.16%, 97.93% respectively and change in IO power will be 90%, 98.99% respectively and leakage power variation will be 2.32%, 23.63% as shown in Table 7 and Figure 19.

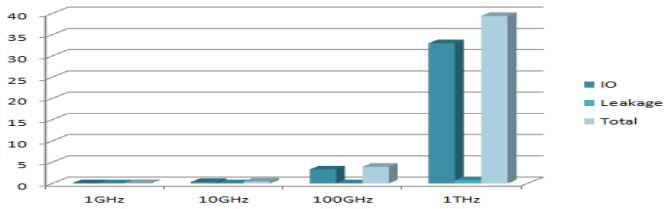

Figure 19. One Hot Counter

H. Divide By 2 Counter

Table 8. Power Dissipation of Divide By 2 Counter

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.000	0.029	0.042	0.077
10GHz	0.050	0.000	0.004	0.289	0.043	0.387
100GHz	0.497	0.003	0.041	2.895	0.053	3.489
1THz	4.973	0.028	0.406	28.950	0.773	35.130

If we use Divide By 2 Counter with at the frequency of 1GHz instead of 10GHz, 100GHz then power reduction will be 80.10%, 97.79% respectively and change in IO power will be 89.96%, 98.99% respectively and leakage power variation will be 2.32%, 20.75%as shown in Table 8 and Figure 20.

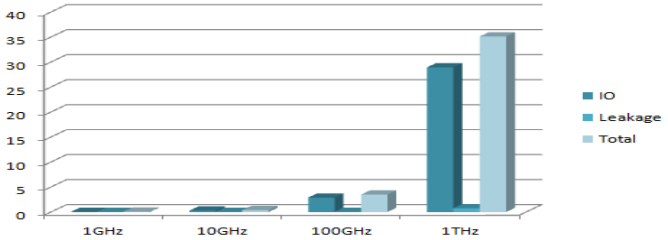

Figure 20. Divide By 2 Counter

I. Divide By 3 Counter

Table 9:Power Dissipation of Divide By 3 Counter

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.005	0.000	0.000	0.004	0.042	0.051
10GHz	0.050	0.000	0.001	0.036	0.013	0.130
100GHz	0.417	0.002	0.010	0.364	0.045	0.917
1THz	4.974	0.013	0.094	3.637	0.084	8.801

If we use Divide By 3 Counter with at the frequency of 1GHz instead of 10GHz, 100GHz then power reduction will be 60.76%, 94.4 % respectively and change in IO power will be 88.88%, 98.90% respectively and leakage power variation will be 2.32%, 6.66% as shown in Table 9 and Figure 21.

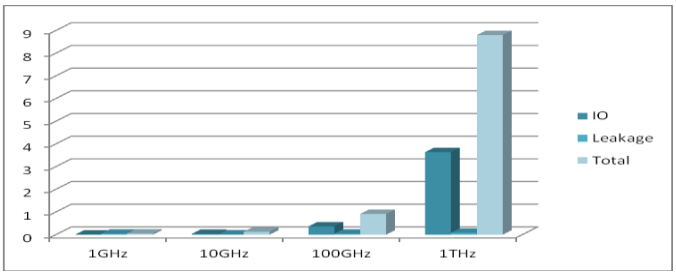

Figure 21. Divide By 3 Counter

J. Divide by 4.5 Counter

Table 10. Power Dissipation of Divide by 4.5 Counter

Freq	Clock	Logic	Signal	IO	Leakage	Total
1GHz	0.006	0.001	0.001	0.005	0.042	0.055
10GHz	0.100	0.005	0.013	0.048	0.043	0.209
100GHz	1.004	0.027	0.126	0.477	0.047	1.679
1THz	10.035	0.245	1.191	4.766	0.188	16.425

If we use Divide By 4.5 Counter with at the frequency of 1GHz instead of 10GHz, 100GHz then power reduction will be 73.68%, 96.72% respectively and change in IO power will be 89.58%, 98.95% respectively and leakage power variation will be 2.32%, 10.63%as shown in Table 10 and Figure 22.

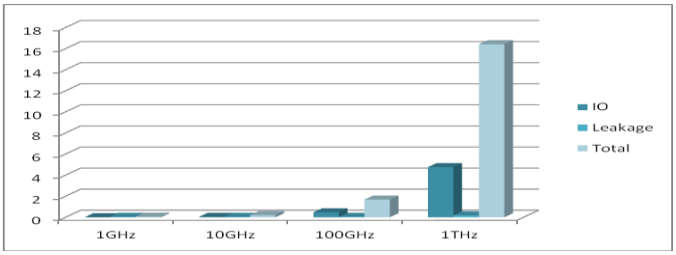

Figure 22. Divide By 4.5 Counter

4. Conclusion

After doing analysis of all the counters discussed above we can conclude that of all the counters, 8 bit simple up counter is the counter in which there is maximum reduction of total power occurs that is 84.25% and 98.33% between a frequency range of 1GHz to 10GHz and 1 GHz to 100 GHz respectively and of all the counters, divide by 3 counter is the counter in which minimum reduction of power takes place that is 60.76% and 94.4% between a frequency range of 1GHz to 10GHz and 1 GHz to 100 GHz respectively. Thus, 8 bit simple up counter is more energy efficient of all the counters mentioned above.

5. Future Scope

In this work, we are using 28nm FPGA technique but in future we can also work on 20nm FPGA, 15nm FPGA, and 7nm FPGA technology. We can also go for SoCs (system on chip) and ultra scale FPGA. This technique can be used in other electronic components

such as ALU, processors, sensors, ICs, and many more in order to make them energy efficient.

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Authors

Daizy Gupta, She is an awardee of young scientist-2016 for her contribution toward research and welfare of humanity. She is an undergraduate student in engineering and covers the basic problem of counting and its implementation for VLSI, electronics, Information Technology and computer science in perspectives of low power and energy efficiency.