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Buffer, Extraction and Style based RAM Design on 28nm Field Programmable Gate Array

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Abstract

In this work, we report a detailed analysis on a low power memory circuit using buffer, extraction and style based RAM design on 28nm Field Programmable Gate Array (FPGA).The designing of this memory circuit is done by Verilog as HDL, Xilinx ISE 14.6 simulator with kintex-7 FPGA. Different RAM styles and RAM extracts are compared on basis of power consumption and reduction. Auto RAM style is the default RAM style and it consumes minimum power as compared to block RAM. The RTL schematic shows I/O ports, nets and primitives. Bufgdll also consumes less power and power reduction is also maximum for bufdll and auto RAM as compared to block RAM, ibufg and RAM extract yes. Auto RAM at 10GHz frequency can be used in designing various applications like in radio astronomy, microwave devices and communications, wireless LAN, most modem radars, communications satellites, satellite television broadcasting.

Keywords*: Memory, Power Efficient, Low Power, RAM, FPGA*

1. Introduction

RAM being a volatile memory thus information written to it can be accessed as long as power is on. In our research, we have used three different types of RAM. This includes RAM style, BRAM and RAM extraction. It is a hardware device that allows information to be stored and retrieved on a computer. Further, this design also allows us to randomly access the data stored in it. Being directly accessed by CPU, data in ram can be read and write very quickly. In our design our design is implemented on 28nm kintex-7 FPGA using different RAM styles. Various families of IO standards like SSTL, HSTL, LVCMOS and LVDCI are supported by Kintex-7 FPGA. Our analysis aims on design an energy optimized system that is more eco-friendly and cost-effective. Moreover, Kintex-7 FPGA requires very less power and results into very high performing circuit. Kintex-7 is a modish class of FPGA; it provides 50% less power consumption than the previous devices. Different types of RAM constraints are shown in Figure 1.

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Figure 1. Different Types of RAM Constraints

We have used two different RAM styles and they are SRAM and DRAM. SRAM (Static RAM) and DRAM (Dynamic RAM) both holds data but in different manner. In DRAM, to retain the data, the data has to be refreshed periodically whereas, in SRAM we need not to refresh the data because the transistors would continue to retain the data in memory as long as the power supply is not turned off. This behavior leads to some advantages, not the least of which is the much faster speed that data can be written and read.

2. Literature Review

In area of energy efficient memory design there is already work going on in ROM design using SSTL IO standards [1]. We are designing RAM in place of ROM. We are designing RAM on 28nm FPGA, while the work have been done on 65nm FPGA [2]. Our memory design is on LVCMOS and the work is already going on HSTL family [3]. The work is going on design of counter, however our energy efficient memory circuit can be used to design counters used in radio astronomy, radars [4]. The frequency range for which our memory circuit design is compatible can also be used for design of Unicode reader with better power efficiency [5].

3. Block Diagram

For our analysis, Random Access Memory (RAM) circuit of 16-bit with different constraints on FPGA of 28nm is been used so as to make it a most power efficient circuit. RAM has the competence of reading data from memory and writing to it. Figure 2 shows RTL schematic of RAM, which has 16 data input pins out of which 6 are address lines and 16 data output pins. It has 3 scalar ports that include clock, enable and write.

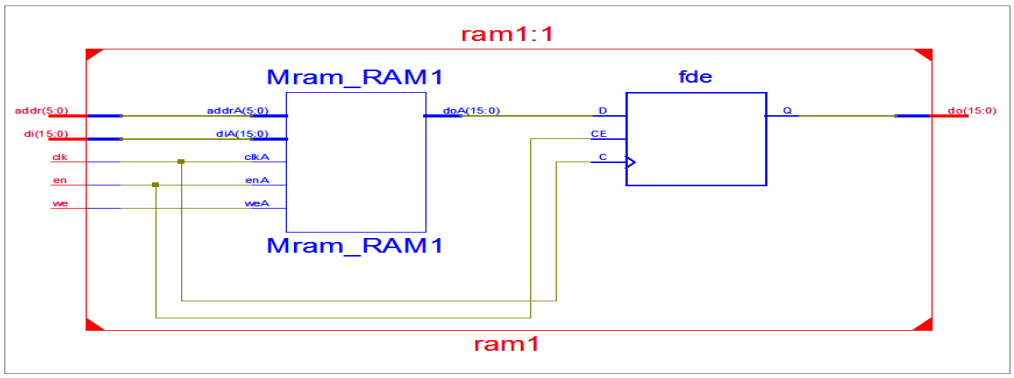

Figure 1. Schematic of Memory Chip from the Design using RTL

Register Transfer Language is abbreviated as RTL. The above schematic shows implementation logic of the circuit. The flowing of data in and out in the circuit can also be studied from above schematics. The Figure 3 shows 16 bit memory package pins of RAM. It has 41 ports, 60 nets and 5 primitives.

Below, a Memory Package with all the pins is shown from Top View.

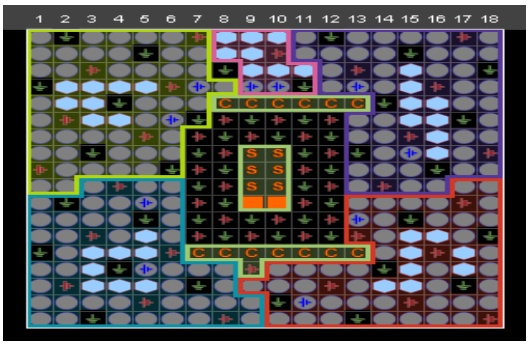

Figure 2. Verilog HDL Design of a 16-bit Memory Package Pins

4. Power Consumption in a 16-bit Memory Circuit

In our research, we focused to minimize the consumption of power in a memory and make our entity cost-effective and power efficient memory circuit. Power is further categorized into two types and they are Static and Dynamic Power Consumption.

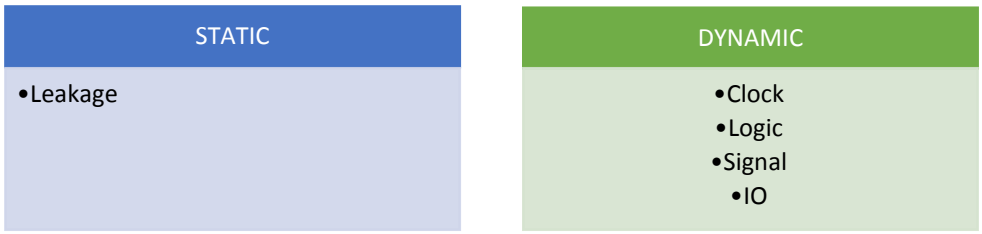

Figure 3. Categories of Power

As presented above in Figure 4, Leakage power is static power, whereas Clock, Logic, Signal and I/O powers are Dynamic Powers. According to analysis, Table 1 below shows us the variations in leakage power at different frequencies.

Table 1. Analysis of Power (W) at Different Frequencies for RAM Styles

Frequency (GHz)	Auto	Block
10	0.706	0.831
1.2	0.197	0.226
2.3	0.279	0.324
3.5	0.344	0.401
4.5	0.122	0.137

Table 1 shows maximum power consumption 0.831W by block RAM at 10 GHz frequencies while minimum power consumption 0.122W is by auto RAM at 4.5 GHz frequencies. Thus it can be observed that auto RAM style at 4.5 GHz frequencies can be used in the design of Wi-max.

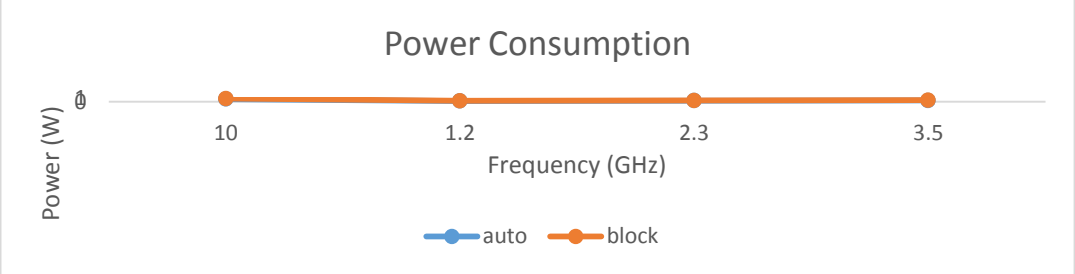

Figure 5. Power Consumption for Ram Styles at Different Frequencies

Table 2. Analysis of Power (W) for BRAM Utilization (Buffer type)

Frequency (GHz)	Bufgdll	Ibufg
10	0.706	0.831
1.2	0.197	0.226
2.3	0.279	0.324
3.5	0.344	0.401
4.5	0.122	0.137

As shown in Table 2, power consumption in case of ibufg is maximum *i.e.* 0.831W at 10GHz frequency while it is minimum in bufgdll *i.e*. 0.122W at 4.5 GHz frequency.

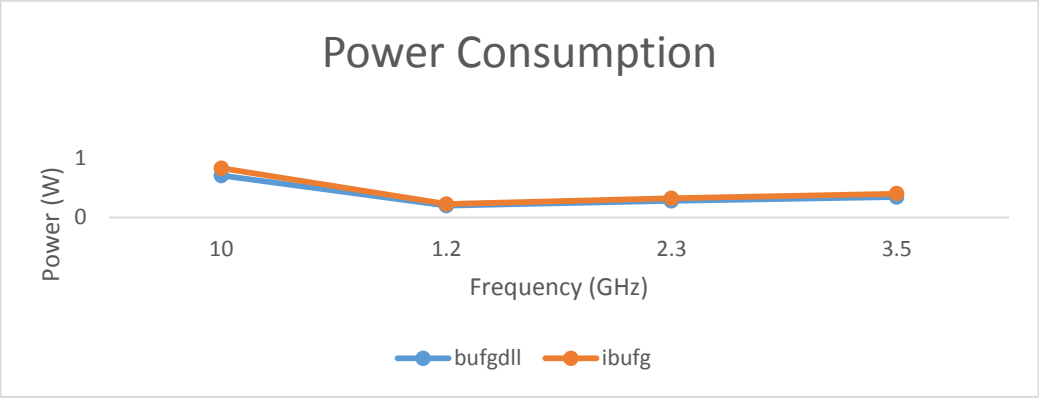

Figure 6. Power Consumption for Buffer Type at Different Frequencies

Table 3. Analysis of Power (W) at Different Frequencies oor RAM Extract

Frequency (GHz)	Yes	No
10	0.706	0.566
1.2	0.197	0.164
2.3	0.279	0.282
3.5	0.344	0.229
4.5	0.122	0.108

As shown in Table 3, power consumption is maximum for RAM extracts yes *i.e*. 0.706W at 10 GHz frequency while power consumption is minimum for RAM extract no *i.e*. 0.108W at 4.5 GHz frequency.

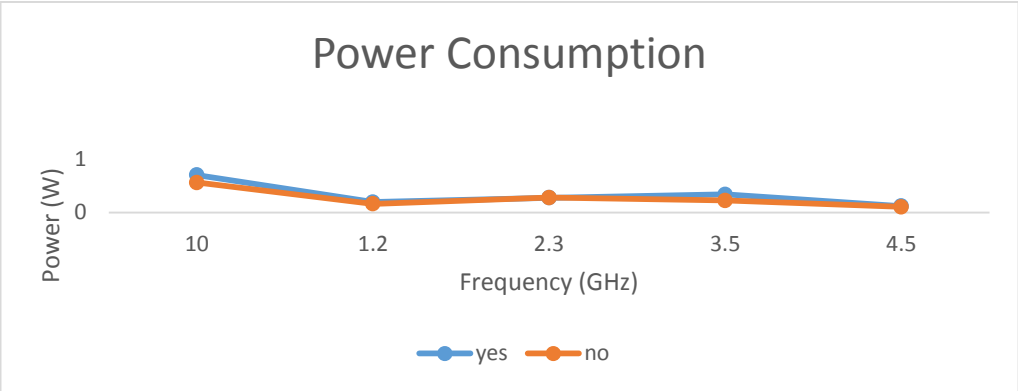

Figure 7.Power Consumption for Ram Extract at Different Frequencies

Table 4. Reduction of Power at 10 Ghz Frequencies as Compared to RAM Extract

	Power Reduction (%)
Auto(RAM style)	24.73%
Block(RAM style)	46.81%
Bufgdll(BRAM)	24.73%
Ibufg(BRAM)	46.81%
Yes(RAM extract)	24.73%

shows minimum power reduction

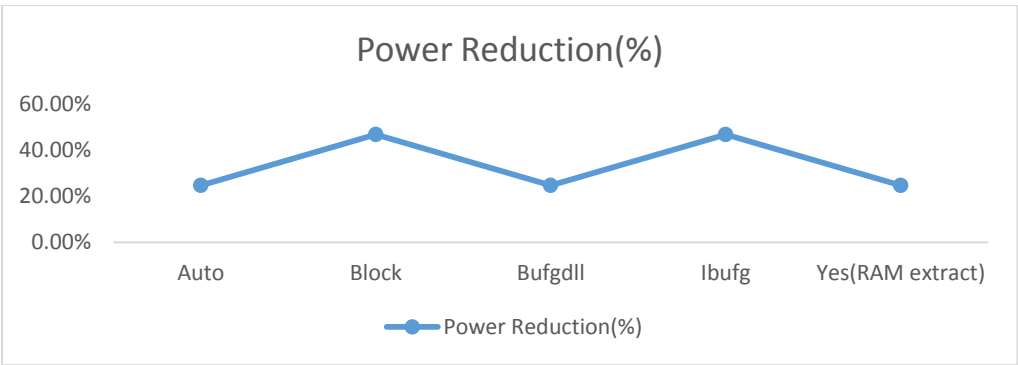

Figure 8. Power Reduction at 10 Ghz as Compared to RAM Extract

Table 5. Power Reduction at 2.3 Ghz Frequency as Compared to RAM Extract

	Power Reduction (%)
Auto(RAM style)	20.12%
Block(RAM style)	37.80%
Bufgdll(BRAM)	20.12%
Ibufg(BRAM)	37.80%
Yes(RAM extract)	20.12%

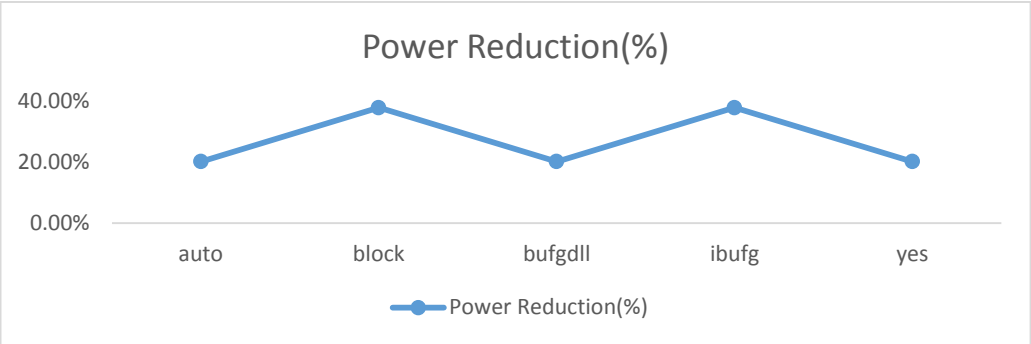

Figure 9. Power Reduction at 2.3 Ghz Frequencies as Compared to RAM Extract

Table 6. Power Reduction at 1.2 Ghz Frequency as Compared to RAM Extract

	Power Reduction (%)
Auto (RAM style)	20.12%
Block (RAM style)	37.80%
Bufgdll(BRAM)	20.12%
Ibufg(BRAM)	37.80%
Yes(RAM extract)	20.12%

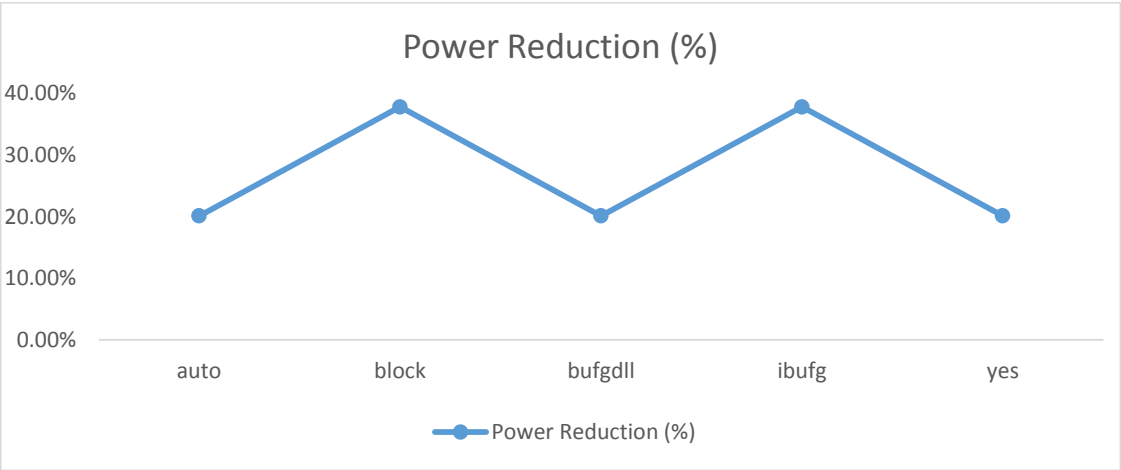

Figure 10. Power Reduction at 1.2 Ghz as Compared to RAM Extract

5. Conclusion

It is proved that auto RAM and bufgdll consumes less power and power reduction is also maximum for bufdll and auto RAM as compared to block RAM, ibufg and RAM extract yes. Power Reduction means to optimize the design to consume as little power as possible. Macro processing decisions are made to implement functions in a manner than uses minimal power. Although power is allowed in both area and speed modes, it may negatively impact the final overall area and speed of the design.

6. Future Scopes

Auto RAM at 10GHz frequency can be used in designing various applications like in radio astronomy, microwave devices and communications, wireless LAN, most modem radars, communications satellites, satellite television broadcasting. As power onsumption is very less in auto RAM, it is very efficient to use in radio astronomy.

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