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Frequency Based Energy Efficient Motley RAM Design on 40nm FPGA Technology

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Abstract

This paper incorporates the most efficient layout of the RAM in terms of the power consumption. Various RAM styles have been thoroughly analyzed. Frequency analysis has been done for RAM on 40nm FPGA. The main focus has been on studying the various power consumption parameters (total power, I/O power, signal power and the clock power) at different frequencies for the different layouts. We focus highly to find out the optimum conditions at which the RAM behaves the best. Frequency variations and its effect on the RAM technologies is basically the main point of concern. Lesser the power consumption, more efficiently would the circuit behave because the improvidence in terms of power consumption is reduced. The analysis has been done using the Verilog VHDL language and XILINX 12.1. We lead to a conclusion that the distributed style is the most preferred one and that too at a lower value of frequency. This research would open up many avenues in the field of electronics and communication regarding the design of various energy efficient RAM designs on the FPGA.

Keywords*: Frequency, energy efficient, Motley, RAM design, 40nm, FPGA, Technology*

1. Introduction

RAM stands for the Random Access Memory. It is a means to store the data. The most striking feature about the RAM is its volatility. It loses its data as soon as the power is turned off. We have perused the RAM with various styles and have focused highly on its response with respect to diverse frequency values.We have taken into consideration the pipelining style precisely called the pipe_distributed style. It is a concept which works on the principle of parallelism. A register is inserted between each of the adjoining blocks. Accordingly, many registers get inserted into the whole system. Also, the number of registers inserted are directly proportional to the frequency of the entire system. Output of one of the blocks is the input for the next block. The main advantage of the system is that the instructions as well as the data is incessantly imparted from one of the blocks to the succeeding blocks. Also, we have evaluated the auto methodology as one of the RAM style. This is a raw style in which the data is interpreted regardless of any form of modification.The best possible design parameters are selected for the process. This is the default mode in which the analysis is done forthe various frequency values and the results are analyzed accordingly. Another technique of analysis is the distributed style.This a form of communication system in which the entire system coordinates by advancing the messages [1]. In the process, the whole program is divided intosmaller fragments or modules that aid the communication process of the entire system. In this system, each processor has a private memory and the information is passed by the means of sharing and

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distribution. This process of apportioning makes the system all the effective.We have taken the RAM extract to be no. this means no data is inferred from the RAM. When it was taken to be yes, the results were similar to those that were produced when the mode was auto. Assigning a "yes" to the RAM extract would have meant enabling the RAM extract. This is equivalent to using the RAM block in a mode in which it can inherit certain properties from the other RAM block. RAM extract no would mean using only the properties of the primary RAM block without any extraction from the other RAMs. This infers to the absolute usage of only a single RAM and no secondary RAMs. If and when the RAM extraction is enabled, two RAM blocks can function together to produce a more beneficial result.

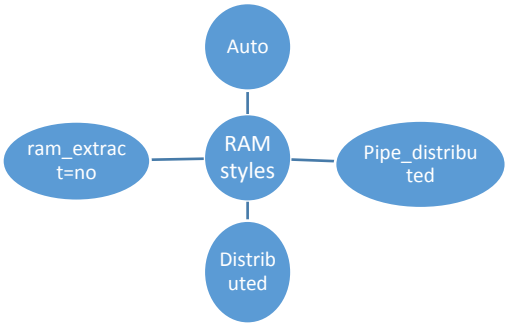

Figure 1. Variegated Analyzed RAM Styles

As depicted by the tables below, the power consumption in a mode where there is no RAM extract is far higher than the contrary case. The results for these different RAM styles have been observed at different Frequency values of 1, 10, 60, 100 GHz and 1 THz. The technology of FPGA used for this purpose is the 40 nm technology or the Virtex-6 technology. This a recent technology that consumes a smaller chip size and takes up lesser power to produce the most desirable results. The comparative analysis is done for various styles of RAM and frequency values to get the most viable conditions of operation for the RAM.

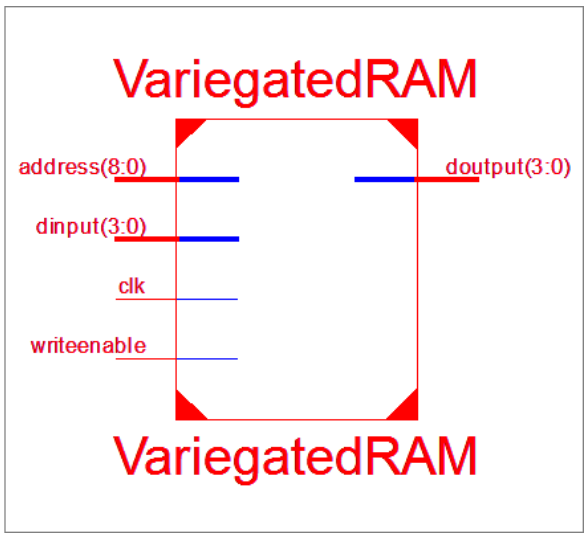

Figure 2. Block Diagram for Motley RAM

2. Related Work

A researcher had focused on realizing the energy efficient FPGA and reconfigurable Digital Filter however we aim at analyzing the variegated RAM styles at different frequencies [2].A researcher had developed an energy aware engineering based on the algorithmic approach whereas we focus on analyzing a RAM structure which consumes the minimum power. We have minutely calculated the values for the power at various frequency values and RAM styles [3]. Also another researcher had been determined to figure out an energy efficient on chip available memory design using the spin torque RAM however our main intent of the research is to study the functioning of the various RAM styles on different frequency values [4]. Also an analyst had been researching on developing a methodology aimed at developing a highly durable, less energy consuming spin torque transfer RAM arrays for different technologies however, we have grossly focused on studying RAM styles at different frequency values [5].

3. Objective

The major intent of the research is to figure out which layout of the RAM is most energy efficient and at what conditions does the RAM with the 40 nm FPGA technology behave the best. We have analyzed the RAM at different frequencies and have drawn various conclusions with respect to the different RAM styles. The total power consumption has been meticulously studied (cited in tables 1-5). Every form of power and energy dissemination in this universe is a form of wastage. It should be reduced to as low a value as possible for the most optimum use of the energy resources. This would in turn automatically reduce the consumption of power. The total power dissipation varies between 12.16% and 87.82%. It has the least values for the distributed styles.The Signal Power, the I/O Power and the Clock Power consumption is the least for the distributed style as well. They vary between 33.33% and 47.82%, 27.08% and 27.80%, 23.52% and 18.40% respectively. At a lower value of frequency the RAM behaves to be the best. This is because at 1GHz the power is least consumed when compared to the ones consumed at 10GHz or for any higher values of frequencies. Also, the distributed style is thought to be the best out of all these styles. It would produce the most optimum results for a similar consumption of power parameters. This combination would prevent the prodigal power consumption and would in turn produce the best results in terms of the efficiency factor.

4. Results

4.1 When Device is Operating at 1 GHz

Table 1. Total Power Observed with Different RAM Styles

RAM styles	Signal	I/Os	Leakage	Total	Clocks
Auto	0.001	0.048	0.713	0.785	0.013
Distributed	0.002	0.035	0.713	0.768	0.017
Pipe_distributed	0.003	0.035	0.713	0.767	0.017
ram_extract =”no”	0.067	0.007	0.716	0.905	0.115

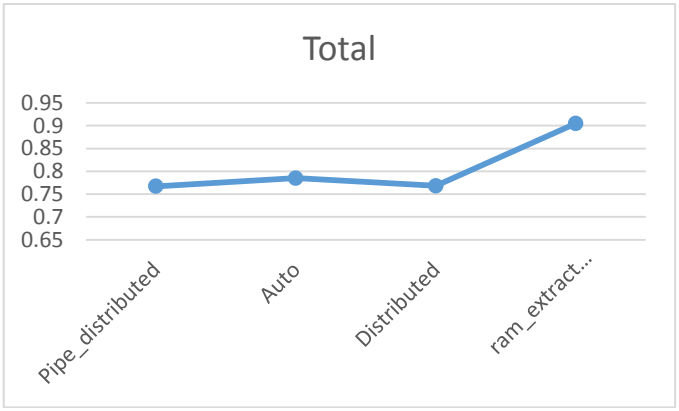

Figure 2. Total Power Plotted with Different RAM Styles at 1 Ghz

The total power decreases by 2.16%, 2.29% for distributed style and pipe_distributed style respectively but increases by 13.25% when there is no ram extract as compared to the automatic style at 1GHz frequency. The signal power increases by 50%, 33.33%, 95.52%, the clock power variegates by 23.52%, 23.52%, 88.69% if the style is varied from auto to distributed, pipe_distributed and ram_extract=no respectively. The I/O power decreases by 27.08% for both distributed and pipe distributed styles and by 85.41% when there is no ram extract as shown in Table 1 and Figure 3.

4.2. When Device is Operating at 10 GHz

Table 2. Total Power Observed with Different RAM styles

RAM styles	Signal	I/Os	Leakage	Total	Clocks
Auto	0.012	0.482	0.729	1.447	0.134
Distributed	0.023	0.348	0.724	1.261	0.165
Pipe_distributed	0.027	0.354	0.724	1.265	0..158
ram_extract =”no”	0.672	0.069	0.756	2.612	1.112

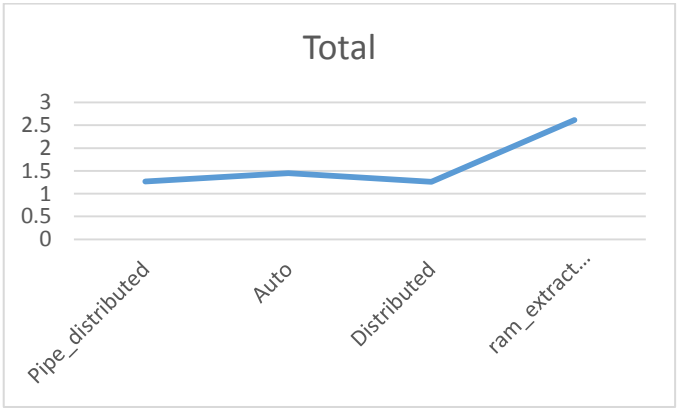

Figure 4. Total Power Plotted with Different RAM Styles at 10 Ghz

The total power decreases by 12.85%, 12.57% for distributed style and pipe_distributed style respectively but increases by 44.60% when there is no ram extract as compared to the automatic style at 1GHz frequency. The signal power increases by 47.82%, 55.55%, 98.21%, the clock power variegates by 18.78%, 15.18%, 87.98% if the style is varied from auto to distributed, pipe_distributed and ram_extract=no respectively. The I/O power decreases by 27.80% for distributed styles, by 26.55% for pipe distributed styles and by 85.68% when there is no ram extract as shown in Table 2 and Figure 4.

4.3. When Device is Operating at 60 GHz

Table 3. Total Power Observed with Different RAM Styles

RAM styles	Signal	I/Os	Leakage	Total	Clocks
Auto	0.073	2.891	0.822	5.133	0.806
Distributed	0.130	2.090	0.792	4.004	0.988
Pipe_distributed	0.155	2.127	0.724	4.024	0.945
ram_extract ="no"	3.685	0.413	1.024	11.694	6.571

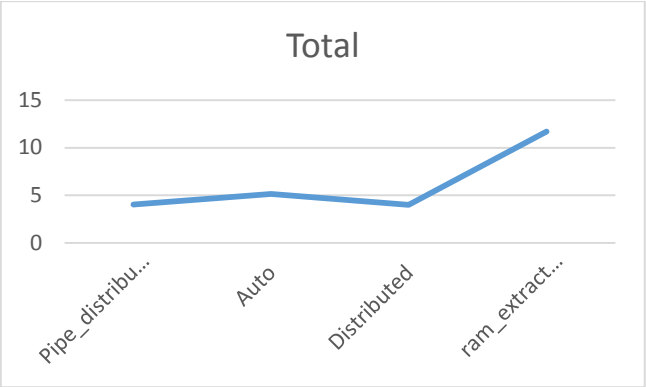

Figure 5. Total Power Plotted With Different RAM Styles at 60 Ghz

The total power decreases by 21.99%, 21.6% for distributed style and pipe_distributed style respectively but increases by 56.10% when there is no ram extract as compared to the automatic style at 1GHz frequency. The signal power increases by 43.84%, 52.90%, 98.01%, the clock power variegates by 18.42%, 14.70%, 87.73% if the style is varied from auto to distributed, pipe_distributed and ram_extract=no respectively. The I/O power decreases by 27.70% for distributed styles, by 26.42% for pipe distributed styles and by 85.71% when there is no ram extract as shown in Table 3 and Figure 5.

4.4. When Device is Operating at 100 GHz

Table 4. Total Power Observed with Different RAM Styles

RAM styles	Signal	I/Os	Leakage	Total	Clocks
Auto	0.121	4.818	0.907	8.092	1.343
Distributed	0.217	3.483	0.852	6.204	1.646
Pipe_distributed	0.256	3.545	0.853	6.236	1.575
ram_extract ="no"	6.005	0.688	1.029	18.675	10.952

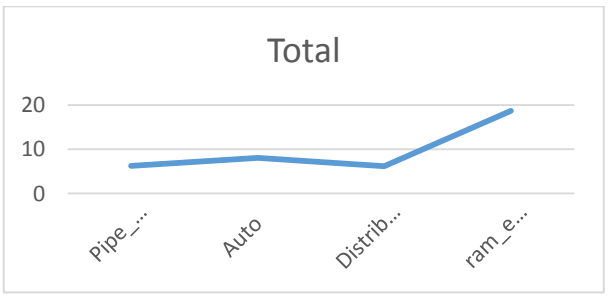

Figure 6. Total Power Plotted with Different RAM Styles at 100 Ghz

The total power decreases by 23.33%, 22.93% for distributed style and pipe_distributed style respectively but increases by 56.66% when there is no ram extract as compared to the automatic style at 1GHz frequency. The signal power increases by 44.24%, 52.73%, 97.98%, the clock power variegates by 18.40%, 17.27%, 87.73% if the style is varied from auto to distributed, pipe_distributed and ram_extract=no respectively. The I/O power decreases by 27.70% for distributed styles, by 26.42% for pipe distributed styles and by 85.72% when there is no ram extract as shown in Table 4 and Figure 6.

4.5. When Device is Operating at 1 THz

Table 5. Total Power Observed with Different RAM Styles

RAM styles	Signal	I/Os	Leakage	Total	Clocks
Auto	1.215	48.177	1.029	72.882	13.431
Distributed	2.155	34.833	1.029	54.534	16.460
Pipe_distributed	2.544	35.447	1.029	54.835	15.752
ram_extract =”no”	59.51	6.878	1.029	177.748	110.327

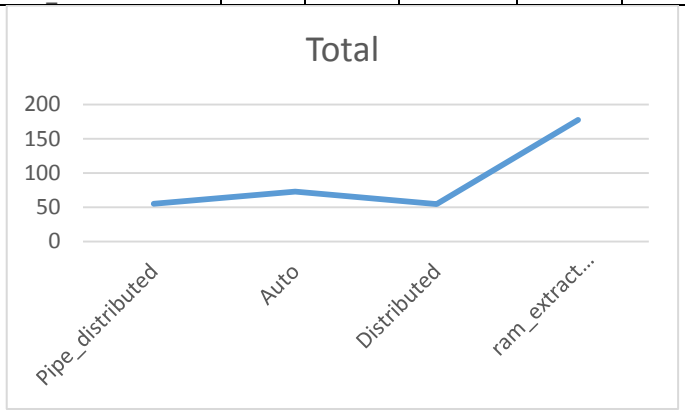

Figure 7. Total Power Plotted with Different RAM Styles at 1 Thz

The total power decreases by 25.17%, 24.76% for distributed style and pipe_distributed style respectively but increases by 58.99% when there is no ram extract as compared to the automatic style at 1GHz frequency. The signal power increases by 43.61%, 52.24%, 97.95%, the clock power variegates by 18.40%, 17.28%, 87.82% if the style is varied from auto to distributed, pipe_distributed and ram_extract=no respectively. The I/O power decreases by 27.69% for distributed styles, by 26.42% for pipe distributed styles and by 85.72% when there is no ram extract as shown in Table 5 and Figure 7.

5. Conclusion

All the research leads us to a conclusion that out of the four styles observed the distributed style is the most preferred at lower values of frequencies. This is because it consumes the least power when compared to the other three styles at value of frequency as low as possible. Therefore, it is the best layout since it cuts down the power wastage to a higher extent thereby proving to be a boon in the field of electronics and communication. Therefore, if the RAM is designed using this style, we are expected to face the least power consumption. Therefore, the use of this style should be greatly entertained in the designing of RAM.

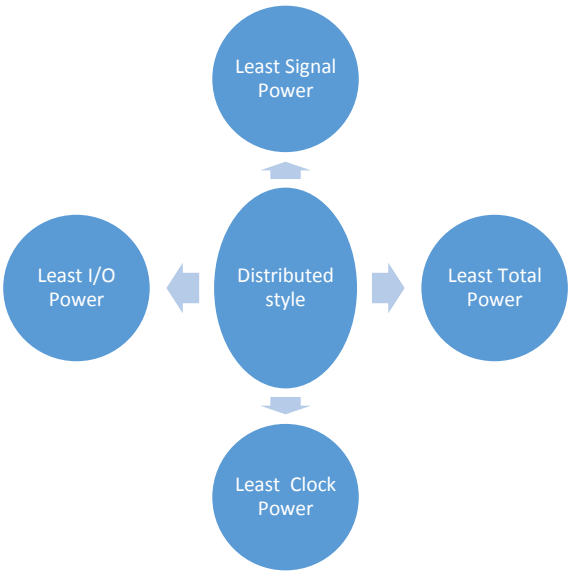

Figure 8. The Style That Consumes the Least Power

6. Future Scopes

In this particular research we have performed the Frequency analysis. However, analysis could also be done taking the time factor into consideration as well. Also, we have performed the analysis for a few forms of RAM. However, similar research work could be accomplished for other layouts as well. We have been concentrated on RAM throughout our research. Similar probe could be carried out for the ROM or any form of memory. Also, at this juncture we have used the FPGA which is a 2 dimensional IC. Further researches could be carried out on the 3D ICs. Here, we have used the simple RAM and the major intent of the research has been to find out that condition where the FPGA behaves to be the most energy efficient. However, further advancements in this field would lead to a detailed study on the memories like EPROM, EEPROM, FRAM *etc*. For this analysis, we have used the 40nm technology. However, with the advancements in science, 28nm has already come into existence and has been proven to be more energy efficient as compared to the 40nm technology. With the further amelioration in technology, the upcoming era would witness a furthermore reduction in size making the memory structure more energy efficient.

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