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An External Capacitor-Less High PSRR Low-Dropout Regulator with Enhanced Transient Response

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Abstract

This paper describes a capacitor-less high PSRR low-dropout (LDO) linear regulator with transition enhancement technique. The proposed LDO uses a 2-stage error amplifier for high PSRR. To maintain high stability without a big external capacitor, cascode compensation technique and current buffer compensation technique are adopted with the small internal capacitance of 1.15pF for local compensation, while the nested Miller compensation technique is used for global compensation. Also, an additional voltage-spike detection circuit improves the load transient response. The LDO operates with an input voltage of 3.3V and provides the output voltage of 1.8V. Simulated line and load regulation are 0.26mV/V and 1.8uV/mA, respectively. The power supply rejection ratio (PSRR) is -90dB and –30dB at DC and 1MHz, respectively. The chip area is 240μm x 110μm.

Keywords*: LDO, Regulator, PSRR, Fast Transition, On-Chip System*

1. Introduction

Low-dropout (LDO) regulators are widely used in SoC to supply clean voltage to the noise-sensitive IP blocks, and also to provide power management for low power consumption. An output capacitor-less LDO regulator is needed to reduce the pad in chip and also to reduce the form factor in printed-circuit-board. However, the removing of output filtering capacitor will lead to severe output voltage changes during fast load current transients [1], [4], [5], [6]. Since the external capacitor provides stability in conventional approach, an extra compensation technique in capacitor-less LDO is needed for stable operation for on-chip application. In addition, to provide a clean voltage to the noise sensitive analog/RF blocks, high power supply rejection ratio (PSRR) is required [2]. In this paper, by using small internal compensation capacitors, high PSRR capacitor-less LDO with transition enhancement circuits is presented.

2. Architecture of the proposed LDO

Figure 1 shows the block diagram of the proposed LDO. The proposed LDO has a 2-stage error amplifier (A1 and A2), and hence a total 3-stage configuration including power transistor (Ap) to achieve a high PSRR. Also, external capacitor is removed. Two zero compensation techniques are locally applied to the 3-stage amplifier with gm-C_{C0} and gm-$C_{C1,}$ and nested Miller compensation technique is also globally applied to the 3-stage amplifier configuration. These compensation techniques guarantee a stable operation without a big external capacitor. In addition, to provide insensitive output voltage changes during fast load current transients, transition

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enhancement circuits (HPF & capacitive coupling) are also equipped on the proposed LDO [4].

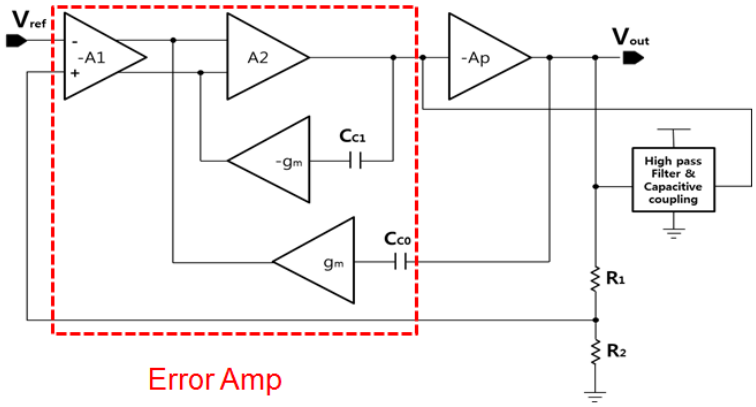

Figure 1. Block Diagram of Proposed LDO

3. Proposed LDO Circuits

The proposed LDO consists of three gain stages as shown in Figure 2 [3]. The first gain stage is a differential-to-single ended amplifier with cascode configuration of input transistor pair; that is, the original input transistor is separated with divided length as M_{A3} and M_{A5} (or M_{A4} and M_{A6}). These cascode designs of input transistors are for the zero compensation that will be explained later. The second gain stage is a current mirror type high gain amplifier to achieve high PSRR. The third gain stage is a driving stage with the power transistor of Mp. For stable operation, the proposed LDO adopted the cascode compensation technique with C_{C0} and M_{A4} and current buffer compensation technique with C_{C1} and M_{A1} within the nested Miller compensation. The compensation capacitor C_{C0} and C_{C1} can be implemented with small internal capacitors [3]. The proposed output capacitor-less, zero-compensated LDO guarantees stability with a total internal capacitor of 1.15pF.

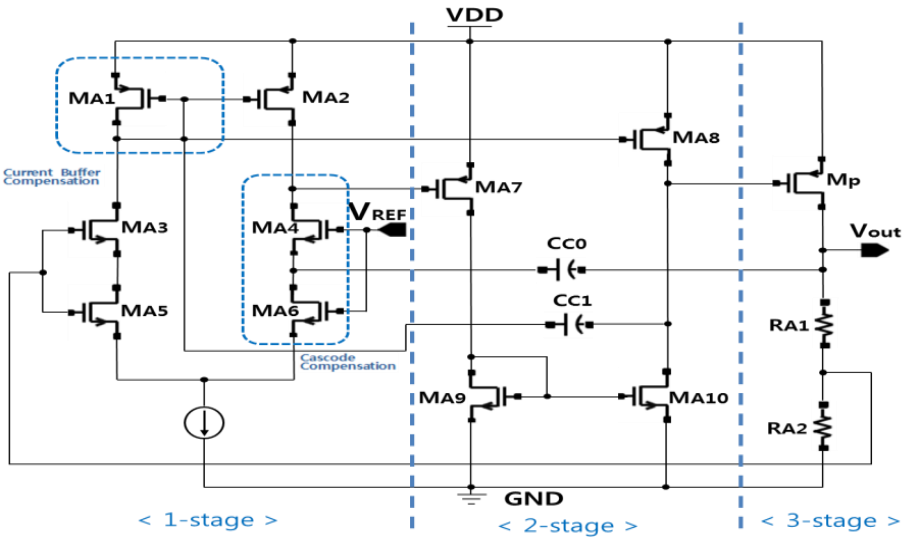

Figure 2. Proposed LDO Circuits

3.1. Cascode Compensation

Figure 3 shows the conceptual diagram of cascode compensation. The trans-conductance of common gate amplifier M_{CG}, g_{mCG}, and capacitor Cc can be used to provide a left-half-plane (LHP) zero as indicated in the equation in Figure 3. The cascode compensation of the proposed LDO has been implemented by the source input impedance of M_{A4} ($1/g_{mA4}$) and C_{C0} in Figure 2

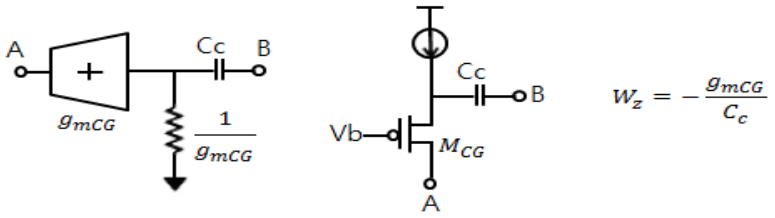

Figure 3. Cascode Compensation

3.2. Current Buffer Compensation

Figure 4 shows the concept of current buffer compensation. Inverting current buffer can be used in series with compensation capacitor to generate another LHP zero. Current buffer compensation of the proposed LDO has been implemented by the impedance of transistor M_{A1} and C_{C1} in Figure 2, and this compensation creates the second left half plane zero. Miller compensation network can appear with a current mirror of unity current gain.

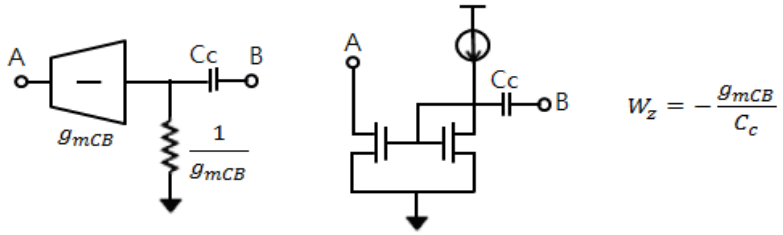

Figure 4. Current Buffer Compensation

3.3. Transition Enhancement Circuits

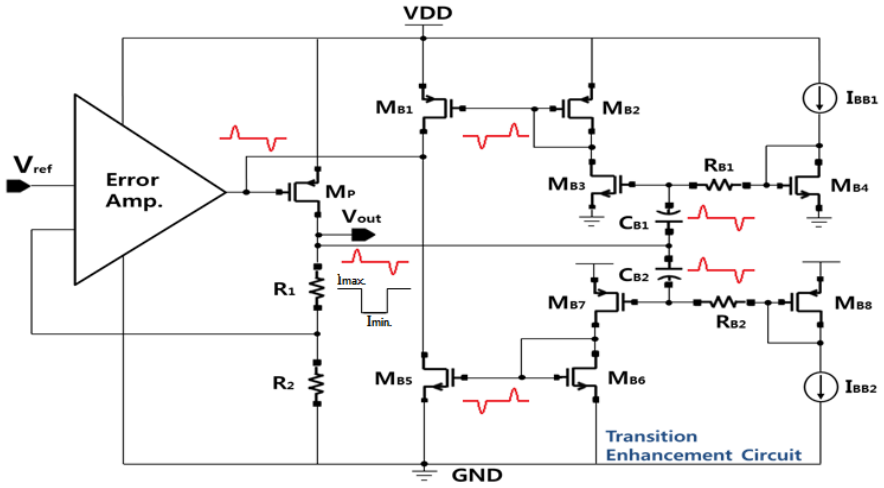

Figure 5. LDO with Transition Enhancement Circuits

The proposed LDO adopted the transition enhancement circuits. Figure 5 shows the operation of transition enhancement circuits when a voltage spike is detected at the output, while the load current is rapidly changing. As shown in Figure 5, resistors (R_{B1}, R_{B2}) and capacitors (C_{B1}, C_{B2}) construct the high-pass filter (HPF) network. This HPF can detect the voltage spike generated at the output (Vout) when a large load current transition occurs. Since the total transient enhancement circuits produce a low-pass filter (LPF) with the HPF in feedback network, this network reduces spike voltages. If Vout is lowered due to the abrupt increase of the load current, the gate voltages of M_{B3} and M_{B7} also will be lowered. This in turn lowers the gate voltage of driver transistor M_P. This lowered gate voltage of M_P makes the output voltage of Vout increase. As a result, we can achieve the regulation with this negative feedback loop in this circuit. The same operation is also achieved in the case of higher Vout due to the abrupt negative change of load current. Since the transition enhancement circuit has no high impedance nodes in the loop, it shows higher bandwidth than LDO loop; hence the fast removal of voltage spike is achieved.

4. Simulation Results and Performance Summary

The proposed LDO was implemented with the 0.18μm high voltage CMOS technology. Figure 6 shows the AC simulation results of the proposed external capacitor-less LDO with the load current of 10μA and 30mA respectively. The first LHP zero, Z_1, was generated by the cascode compensation and is located just behind the second pole. The second LHP zero, Z_2, was generated by the current buffer compensation and is located between the first zero and the unit-gain-frequency.

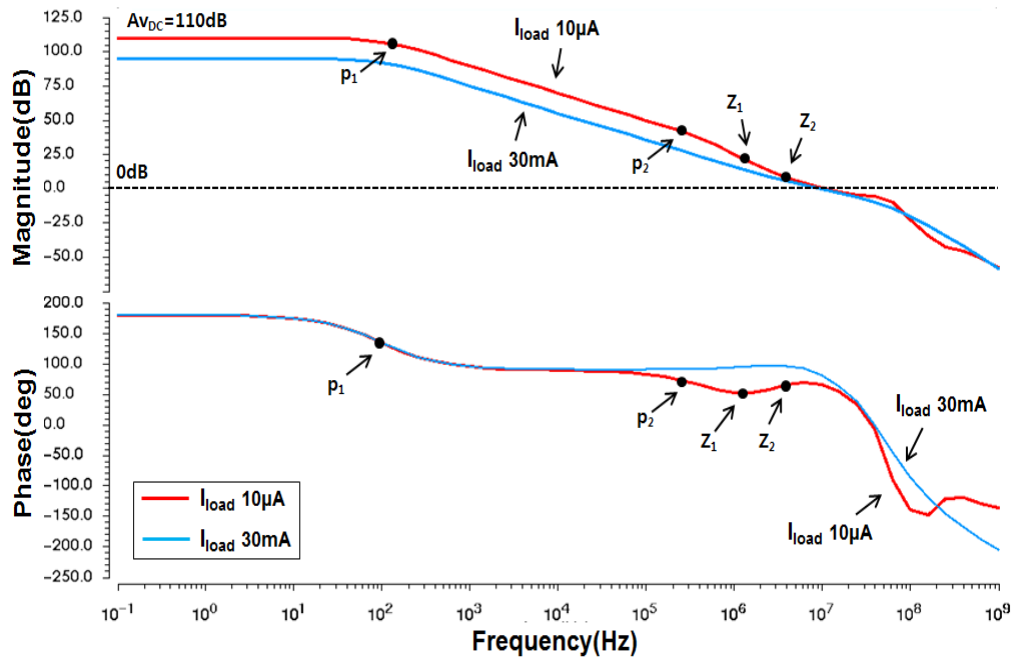

Figure 6. AC Simulation Results of Proposed LDO

As shown in Figure 6, these two compensation techniques improve the phase margin and guarantee frequency stability. The proposed LDO has DC gain of 110dB and phase margin of 62°. The simulated results of PSR are over -90dB and -34dB at

DC and 1MHz with the load current of 10μA and 30mA, respectively, as shown in Figure 7. Figure 8 shows the load transient simulation results when the output load current has the change of 30mA with rising time of 500ns. With these transition enhancement circuits, undershoot and overshoot of output voltage are reduced from 400mV to 50mV and from 1100mV to 100mV, respectively. The layout size of the proposed LDO with bandgap reference is 0.026mm^2 as shown in Figure 9. The performance summary is presented in Table 1.

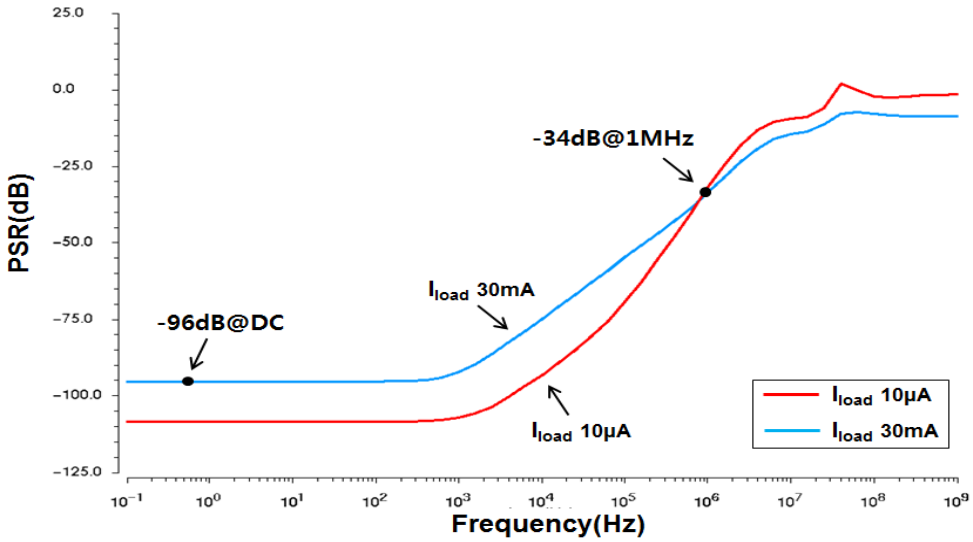

Figure 7. PSR Simulation Results

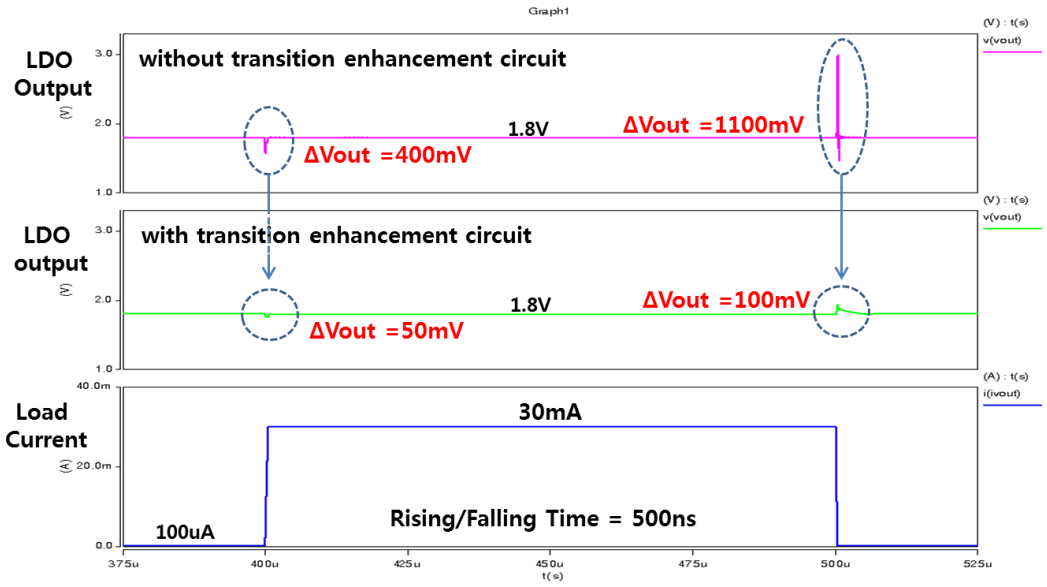

Figure 8. Load Transient Simulation Results

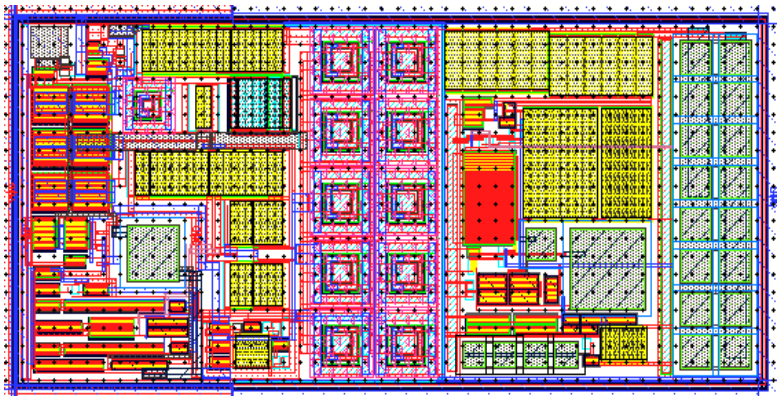

Figure 9. Layout(240μm x 110μm)

Table 1. Performance Comparisons

Parameter	[2]	[6]	This Work
V_{in}(V)/V_{out}(V)	3.3/1.3	1.5/1.3	3.3/1.8
Io, Max(mA)	10	50	30
On-Chip Capacitance(pF)	3	NA	1.15
PSRR(dB)@Hz	-56dB@DC -10dB@1MHz	NA	-90dB@DC -30dB@1MHz
Current consumption(μA)	39	29	40
Chip Area(mm^2)	NA	0.252	0.026

5. Conclusion

The output capacitor-free high PSRR LDO was designed with a voltage spike reduction technique. To achieve high PSRR, a 2-stage error amplifier was adopted. The stability of the proposed LDO was guaranteed by using the cascode compensation technique and also by using the current buffer compensation technique. To reduce the output voltage change from the load current transition, a spike cancellation circuit was adopted.

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