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Low Power Squarer Design Using Ekadhikena Purvena on 28nm FPGA

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Abstract

EkadhikenaPurvena is a Sanskrit name which means "one more than the previous". This technique is used for squaring any big number but the condition is it should end with digit "5". Vedic mathematical formulas are used to solve tedious and cumbersome arithmetic operations. Tool is Xilinx ISE Design Suite 14.2 and Kintex-7. We have taken different frequencies and calculated its power. Today's demand forces us to design the low power energy efficient devices which takes lesser time for its execution. In our design there are 2 inputs and 1 output. The inputs are clocked and the number whose square we are supposed to calculate is 8 bits wide and the output is 14 bits wide (squared number). Many researchers have performed research on Vedic mathematics to solve DSP operations using Urdhava-Triyagbhayam multiplication sutra. We have done power analysis by varying frequency at different temperatures to make our Vedic squarer energy efficient. Temperatures taken in view are 56.7, 53.5, 40, 21 degree Celsius and Airflow is 250 LFM (Linear Feet Per Minute). Analysis results shows that the maximum power consumption is at 2.2 Billion Hertz and minimum power consumption is at 1400 Million Hertz. In respect to temperature maximum power is consumed at 56^{o}C and minimum at 21^{o}C.

Keywords*: EkadhikenaPurvena, Vedic mathematics, FGPA, energy efficient, Vedic squarer*

1. Introduction

Ancient mathematics is also called Vedic mathematics [1-2]. Vedic mathematics taken from four Vedas (books of wisdom) [3]. Vedic mathematics deals with various Vedic mathematical formulae and their applications to carry out tedious and cumbersome arithmetic operations [4]. It save time in mathematical calculations, even when there were no computers [5]. DSP operations based on ancient Vedic Urdhava-Triyagbhayam [6], 8-bits fixed point Vedic DSP processor [7] and 4*4 multiplier based Urdhva-Tiryakbhyam [8], and division using Vedic technique `Dhwajam' [9] are getting attention of researcher. In our paper we have designed a Vedic squarer using Vedic mathematical technique "EkadhikenaPurvena" meaning "one more than the previous". This technique is used for squaring any big number but the condition is it should end with digit "5". Tool is Xilinx ISE Design Suite 14.2 and 28nm Kintex-7. We have taken different frequencies and calculated its power. Frequencies of different mobile sets are taken which can be seen in table 1. Ambient temperature is changing every time we have taken 4 temperatures on which we have tested our design. Temperatures taken in view are 56.7, 53.5, 40.0, 21.0 degree Celsius and Airflow is 250 LFM. Vedic squarer is shown in Figure 1. For example if the input number is 5 so it is written in the form 8'b00000101 and the square of this number is 25 (14'b00000000011001). Our paper deal with "EkadhikenaPurvena" this is a

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Sanskrit work meaning "one more than the previous". In this technique we have to square the last digit and multiply the remaining digits with one more than that number and then concatenate both the results. All this process takes place in our Vedic squarer. In [10] a generalized squarer is designed to square any binary number. In paper [7] an efficient vedic multiplier is designed using Urdhva - tiryagbhyam, NikhilamNavatashcaramamDastaha, Ekadhikena Purvena, Ekanyunena Purvena, Anurupyena, AntyayorDasakepi sutras. LVCMOS IO standard is used to design FPGA based Thermal Aware Energy Efficient Vedic Multiplier based on UrdhvaTiryagbhyam [11]. In order to achieve performance with energy efficiency, HSTL IO standard is also used along with LVCMOS for design of energy efficient Vedic multiplier based on UrdhvaTiryagbhyam [12]. Frequency scaling is one of the best energy efficient technique for FPGA based VLSI design [13-18]. Here we are going to utilize the benefit of frequency scaling for this Vedic Squarer based on Vedic formula of EkadhikenaPurvena. Table 1 shows the set of frequencies taken in consideration along with its corresponding mobile set. We can vary the temperature range according to our convenience.

Table 1. Maximum Operating Frequency of Cellular Device

Operating Frequency	Cellular Device
1400 Million Hertz	Nokia Lumia 710
1.2 Billion Hertz	Samsung Galaxy Core
2100 Million Hertz	I phone6
1700 Million Hertz	HTC/T
1800 Million Hertz	Micromax X091
2.2 Billion Hertz	Sony Xperia Z1

This Vedic squarer design is based on 28nm FPGA, Verilog code, XC7K160T Kintex-7 FPGA, FBG676 package and -3 speed grade. Table 2 shows different parameters available in Kintex-7 FPGA.

Table2. Characteristic Features of Kintex-7 FPGA

Input/Output (I/O) pins	676
Look Up Table (LUT)	101400
Flip Flop	202800
BRAM	325
GTXE2 Transceiver	8
PCI Buses	1.1
MMCMS	8
Minimum operating temperature (OT)	273.15 Kelvin
Reference OT	358.15 Kelvin
Maximum OT	358.15 Kelvin
Minimum voltage (V)	0.97 Volt
Reference voltage (V)	0.97 Volt
Maximum voltage (V)	1.03 Volt

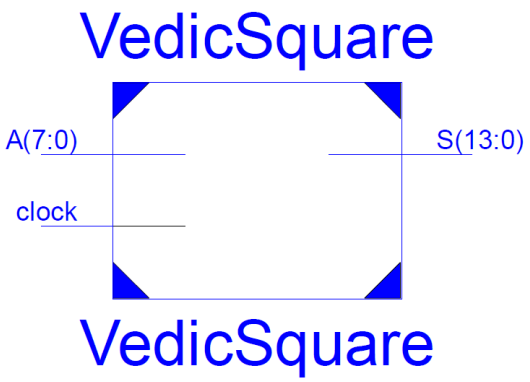

Figure 1. Symbol of EkadhikenaPurvena

2. Power Analysis

A. Power Analysis at 56.7 degree Celsius

Table 3. Power Analysis at 56.7°Celsius

FREQUENCY	**Total Power**
1400 Million Hertz	0.224
1.2 Billion Hertz	0.238
2100 Million Hertz	0.236
1700 Million Hertz	0.229
1800 Million Hertz	0.231
2.2 Billion Hertz	0.238

There is 5.88% reduction in power consumption with 28nm FPGA and temperature is 56.7 degree Celsius and frequency is varied for example 1400 Million Hertz, 1.2 Billion Hertz, 2100 Million Hertz, 1700 Million Hertz, 1800 Million Hertz, 2.2 Billion Hertz as visible in Table 3 and Figure 2.

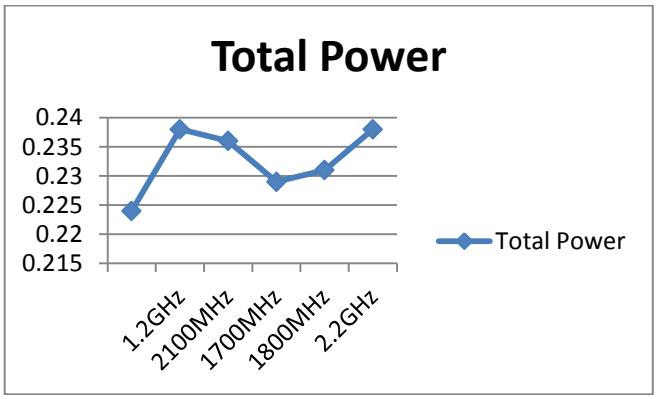

Figure 2. Power Dissipation at 56.7°Celsius Temperature for 1 Billion Hertz

B. Power Analysis at 53.5 degree Celsius

Table 4. Power Analysis at 53.5°Celsius

FREQUENCY	**Total Power**
1400Million Hertz	0.202
1.2Billion Hertz	0.216
2100Million Hertz	0.214
1700Million Hertz	0.207
1800Million Hertz	0.209
2.2Billion Hertz	0.216

There is 6.48% reduction in power consumption with 28nm FPGA and temperature is 53.5 degree Celsius and frequency is varied for example 1400 Million Hertz,1.2 Billion Hertz, 2100 Million Hertz, 1700 Million Hertz, 1800 Million Hertz, 2.2 Billion Hertz as

visible in Table 4 and Figure 3.

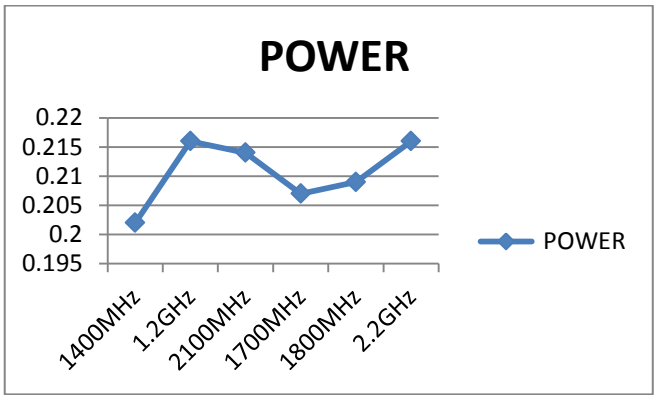

Figure 3. Power Dissipation at 53.5°Celsius Temperature for 10 Billion Hertz

C. Power Analysis at 40 degree Celsius

Table 5. Power Analysis at 40°Celsius

FREQUENCY	**Total Power**
1400 Million Hertz	0.136
1.2 Billion Hertz	0.149
2100 Million Hertz	0.147
1700 Million Hertz	0.141
1800 Million Hertz	0.142
2.2 Billion Hertz	0.149

There is 8.72% reduction in power consumption with 28nm FPGA and temperature is 40 degree Celsius and frequency is varied for example 1400 Million Hertz, 1.2 Billion Hertz, 2100 Million Hertz, 1700 Million Hertz, 1800 Million Hertz, 2.2 Billion Hertz as visible inTable 5 and Figure 4.

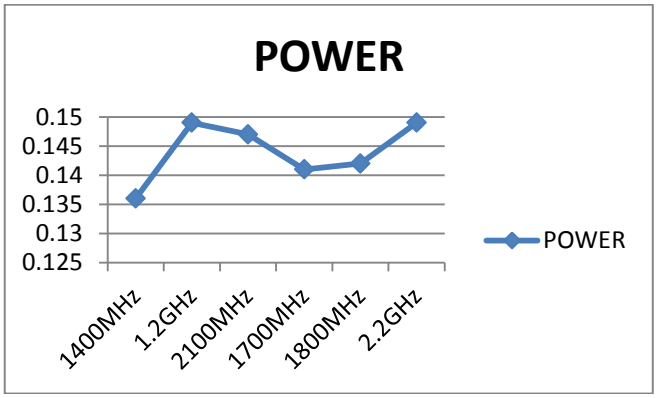

Figure 4. Power Dissipation at 40°Celsius Temperature for 6 Million Hertz

D. Power Analysis at 21 degree Celsius

Table 6. Power Analysis at 21°Celsius

FREQUENCY	**Total Power**
1400 Million Hertz	0.089
1.2 Billion Hertz	0.102
2100 Million Hertz	0.101
1700 Million Hertz	0.094
1800 Million Hertz	0.096
2.2 Billion Hertz	0.102

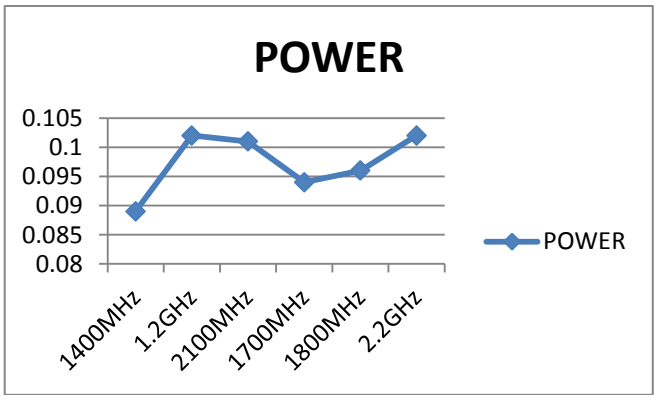

Figure 5. Power Dissipation at 21°Celsius Temperature for 10 Billion Hertz

There is 12.74% reduction in power consumption with 28nm FPGA and temperature is 21 degree Celsius and frequency is varied for example 1400 Million Hertz, 1.2 Billion Hertz, 2100 Million Hertz, 1700 Million Hertz, 1800 Million Hertz, 2.2 Billion Hertz as visible in Table 6 and Figure 5.

E. Power Consumption at Different Frequencies at Different Temperatures

Table 7. IO Power Analysis for Different Frequencies at Different Temperatures

Frequency	56.7°C	53.5°C	40°C	21°C
1400Million Hertz	0.224	0.202	0.136	0.089
1.2Billion Hertz	0.238	0.216	0.149	0.102
2100Million Hertz	0.236	0.214	0.147	0.101
1700Million Hertz	0.229	0.207	0.141	0.094
1800Million Hertz	0.231	0.209	0.142	0.096
2.2Billion Hertz	0.238	0.216	0.149	0.102

From Table no. 7 and Figure no. 6 we can conclude that the maximum power consumption is at 1.2 Billion Hertz and 2.2 Billion Hertz and minimum power consumption is at 1400 Million Hertz. In respect to temperature maximum power is consumed at 56°C and minimum is consumed at 21°C.

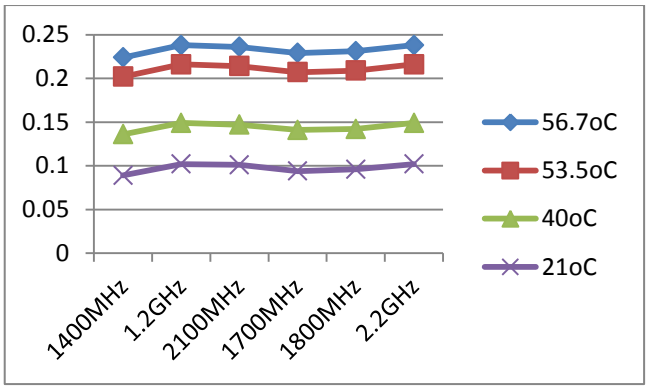

Figure 6. IO Power Analysis for Different Frequencies at Different Temperatures

3. Conclusion

The design is low power energy efficient and the code has been developed in Verilog and results were verified on 28nm FPGA platform. This Vedic squarer consists of 2 inputs that are clocked pulse and input 8 bits number to be squared and one 14 bits output. The design is tested by varying frequency at different temperatures. We can conclude that the maximum power consumption is at 1.2 Billion Hertz and 2.2 Billion Hertz and minimum power consumption is at 1400 Million Hertz. In respect to temperature, maximum power is consumed at 56^{o}C and minimum power is consumed at 21^{o}C.

4. Future Scope

As future is continuously becoming the present, no line can be drawn between present and future. Here, we find Ekadhiken Purven is the fastest method to compute square of some natural number. In future, we can find the any other method that gives more faster result than this. Here our frequency is in limit of 1.2-2.2 Billion Hertz. There is always open door for this research that we can migrate our same research in Tera Herts domain with the latest three dimenstional integrated circuits. Whole work is done in Xilinx ISE Design Suite 14.2 with Verilog. In future, we can go for Vivado System edition that also supports System Verilog.

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